"POLITEHNICA" UNIVERSITY of BUCHAREST
ELECTRICAL ENGINEERING DOCTORAL SCHOOL

DOCTORAL THESIS ABSTRACT

RESEARCH ON THE ANALYSIS OF ANALOG CIRCUITS WITH MEMRISTORS

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CHAPTER 1
INTRODUCTION

1.1. CURRENT ISSUES

The new circuit element, called the *memristor*, was first postulated in 1971 by Professor Leon Chua of the University of California - Berkeley and defines a nonlinear, passive, two-terminal electrical component that establishes a relationship between electrical charge and magnetic flux.

Some of the current interest topics refer to the construction of circuits with memristive logic gates, the construction of memory blocks with the help of memristors, the use of memristors in neuromorphic circuits or read-out integrated circuits ('ROIC'), etc.

Research on memristors continues today, mainly due to the fact that they have gone beyond the concept stage, but the main problem remains the fact that despite the promising features of memristors, they have not yet found their place in the electronics industry.

1.2. THESIS OBJECTIVES

The purpose of this paper is to outline an overview of the memristor's main aspects and includes in a first part the memristor's fundamental notions, its mathematical model and its physical model.

The second part of the paper presents memristive analog circuits from the main possible areas of applicability of this innovative circuit element: using memristors in order to ensure the switching phenomenon in circuits with logic gates; using memristors to model brain synapses according to the neuronal model proposed by researchers Hodgkin and Huxley, by replacing active ion channels with memristive channels, respectively; adding the memristor within the Chua oscillator circuit to improve the chaotic character of the circuit and to study the effects, respectively the dynamics of the proposed memristive circuit.

1.3. THESIS CONTENT AND STRUCTURE

The thesis "Research on the Analysis of Analog Circuits with Memristors" is structured in 6 chapters as follows:

In ***Chapter 1 - Introduction***, general aspects related to the current issues encountered in this research are presented, followed by the objectives pursued in this paper.

Chapter 2, entitled ***Analysis of analog circuits with memristors*** is an introductory and explanatory one, which outlines a general analysis of the basic concepts of memristors. The memristor's mathematical model defined by Leon Chua is presented, followed by the physical model of memristors with nonlinear dopant drift proposed by the *Hewlett-Packard* company.

Chapter 3, entitled ***Simulation of memristive nonlinear circuits***, presents examples of nonlinear electrical circuits analysis starting from the LT Spice model of HP memristor proposed by Zdeněk BIOLEK, followed by an analysis of memristive logic gates circuits.

Chapter 4 entitled ***Neural modeling using the Hodgkin-Huxley principle*** studies the electrophysiological neural model introduced by researchers Hodgkin and Huxley. In this chapter being reproduced this behavior by means of passive and non-volatile memristors, by a detailed study and a characterization of two biological memristors with sodium and potassium ion channels, by studying their equivalent electrical circuits and specific waveforms.

Chapter 5 entitled ***Implementing a chaotic oscillator using the HP memristor*** presents a chaotic circuit based on the traditional model of Chua's oscillator, but which combines the use of a traditional nonlinear resistor with the addition of a memristor, respectively the model made in HP laboratories.

The circuits proposed in this paper start from the techniques used so far to model the nonlinear element in the Chua oscillator circuit, either with the help of two diodes and resistors (Matsumoto model), or with operational amplifiers and six resistors (Kennedy model), to which I added the HP memristor model.

Chapter 6 - Conclusions and Original Contributions presents the final conclusions of the scientific activity carried out during the doctoral thesis preparation, the author's original contributions made in the thesis and a series of future research directions.

CHAPTER 2
ANALYSIS OF ANALOG CIRCUITS WITH MEMRISTORS

2.1. MEMRISTOR - THEORY

The notion of memristor was first recorded by Professor Leon Chua in 1971 announcing the existence of a new passive circuit element with two terminals, along with resistor, coil and capacitor.

Starting from the idea of obtaining a symmetry of the equations that define the fundamental passive circuit elements (figure 2.1), Chua assumed that there must be a connection between the magnetic flux and the electric charge, in addition to those already existing between voltage and electrical current, magnetic flux and electrical current, voltage and electric charge respectively.

The nonlinear dependence relationship between the electric charge *q(t)* and the magnetic flux *φ(t)* in Figure 2.1 is thus ensured by the fourth passive terminal element with two terminals which is characterized by the property called self-resistance ***M***, measured in ohms [Ω] [1], [12].

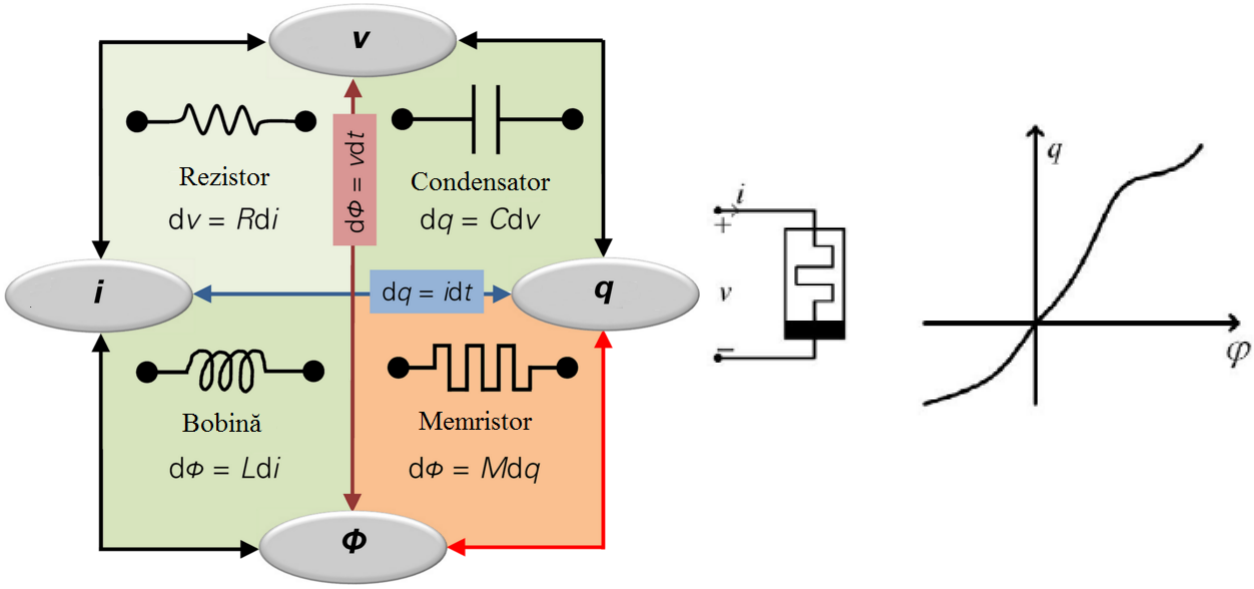


Figure 2.1 Passive circuit elements with two terminals [3]

Memristor's symbol and *φ*-*q* characteristic [1]

2.2. PHISICAL MODEL OF MEMRISTORS

The physical implementation of the memristors was initially developed by Hewlett-Packard (HP) laboratories in 2008, by positioning two layers of titanium dioxide between two platinum electrodes (figure 2.2). The first layer is partially doped with oxygen gaps and behaves like a semiconductor, and the second layer of pure titanium dioxide acts as an insulating layer [3].

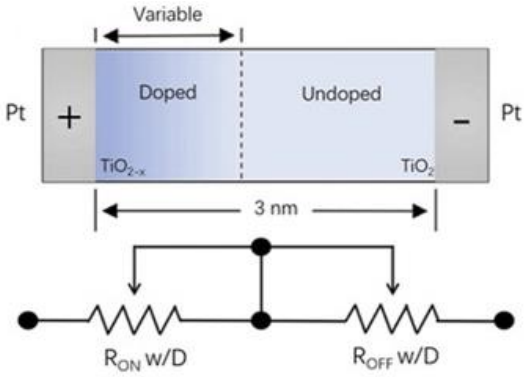


Figure 2.2 Internal structure of a memristor (w - variable width of the doped layer, D - total width of the memristor - 3nm for HP model) [3]

When a positive voltage is applied to the memristor's terminals, the gaps in the doped layer migrate to the right, moving the boundary in the same direction and decreasing the resistance of the undoped layer. At the end of the potential, the gaps remain immobilized and the total resistance of the memory remains constant, thus noting the characteristic of storing the resistance value even in the absence of a power signal.

Another fingerprint of the HP memristor is the $M(q) = V(t)/I(t)$ characteristic. This is a current-voltage curve of an odd hysteresis loop, symmetrical around the origin that describes the current phase shift depending on the polarity of the voltage applied to the terminals of the semiconductor element [3], [12].

The I-V characteristic illustrated in figure 2.3 highlights a switching between different resistance values. It reaches positive values when the voltage applied to the memory resistor terminals increases, respectively negative when the voltage decreases. The characteristic can be restricted to a straight line for high frequencies, in which case the memristor behaves like a classical resistor [38].

2.3. THE MATHEMATICAL MODEL OF MEMRISTORS

This paper studies the model of a memristor with nonlinear dopant drift presented by HP. Starting from the series connection of the two layers of titanium dioxide and applying Ohm's law, we can express the mathematical model of the memristor by the following relations [5], [12]:

$$v(t) = \left[R_{on} \frac{w(t)}{D} + R_{off} \left(1 - \frac{w(t)}{D} \right) \right] i(t) \tag{2.13}$$

Where $w(t)$ represents the width of the doped layer, R_{on} is the minimum resistance of the memristor, and R_{off} is the maximum resistance of the memristor.

Variation of memristence over time [5], [12]:

$$M_q(t) = R_{off} \left(1 - \frac{\mu_v R_{on}}{D^2} q(t) \right) = R_{off} \left(1 - \frac{q(t)}{Q_d} \right), \tag{2.17}$$

where $Q_d = \dfrac{D^2}{\mu_v R_{on}}$.

Considering $\Delta R = R_{off} - R_{on} \cong R_{off} \cong M_0$, then the electric charge through the memristor can be expressed as follows [5], [12]:

$$q(t) = Q_d \left(1 - \sqrt{1 - \frac{2}{Q_d R_{off}} \varphi(t)} \right), \tag{2.18}$$

By differentiating the above relation we can obtain the equation of current intensity as a result of the displacement of the electric charge through the memristor, in which the ratio between R_{off} and R_{on} was noted with r [5], [12]:

$$i(t) = \frac{v(t)}{R_{off} \sqrt{1 - \dfrac{2\mu_d}{rD^2} \displaystyle\int_0^t v(t)dt}} \tag{2.19}$$

CHAPTER 3
SIMULATION OF MEMRISTIVE NONLINEAR CIRCUITS

3.1. INTRODUCTION

This chapter presents methods for simulating memristive circuits. Their analysis is based on the memristor with nonlinear dopant drift developed in HP laboratories, respectively on the model proposed by Zdeněk BIOLEK and developed in the LT Spice program, followed by the analysis of memristive logic gates circuits.

The modeling of a nonlinear memristor using LTspice program is performed starting from the equivalent electrical circuit of such a device, being implemented using a 'netlist' file, attached in APPENDIX1, which defines the electrical subcircuit's topology, the mathematical model and the values used for its parameters at the initial time t_0.

3.2. LTSPICE ANALYSIS OF MEMRISTORS

The LTspice program is used as it allows easy simulation of analog circuits by defining the topology of the electrical circuit (figure 3.2) and analyzing the waveforms described by it. The memristor is added to the LTSpice program library as a new circuit element with two terminals (*plus, minus*), being characterized by the properties described in the *MEMRISTOR.subckt* file in APPENDIX1.

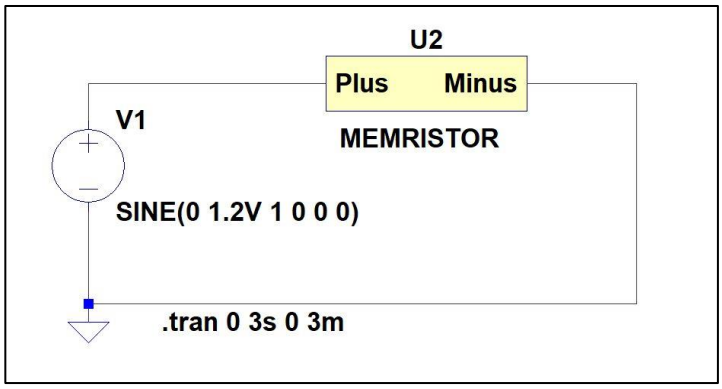


Figure 3.2 LTSpice analysis of a memristor

The memristor model is then loaded into LT Spice using a 'netlist' file that defines the topology of the electrical subcircuit in Figure 3.2, the mathematical model and the values used for the memristor's parameters at the initial time t_0. The memristor is supplied with a sinusoidal voltage of 1.2V amplitude and a transient analysis is performed by studying the time variation of the supply voltage, the current absorbed by the memristor and the hysteresis curve characteristic of memory devices.

3.3. ANALYSIS OF MEMRISTIVE LOGIC GATES

Possible digital applications based on memristive systems seem to open up great opportunities and challenges to today's researchers. One of the topics of current interest refers to the construction of circuits with logic gates using memristors. Memristive devices are used in this case only to ensure the switching phenomenon and not to store logic states, similar to already existing circuits based on CMOS logic. The implementation of memristive logic gates is realised by connecting in series two memristors of opposite polarities (figure 3.5) [15]. Thus, the input signals are provided by the free terminals of each memristor, while the output signal is obtained through the common terminal of the two serial devices [7].

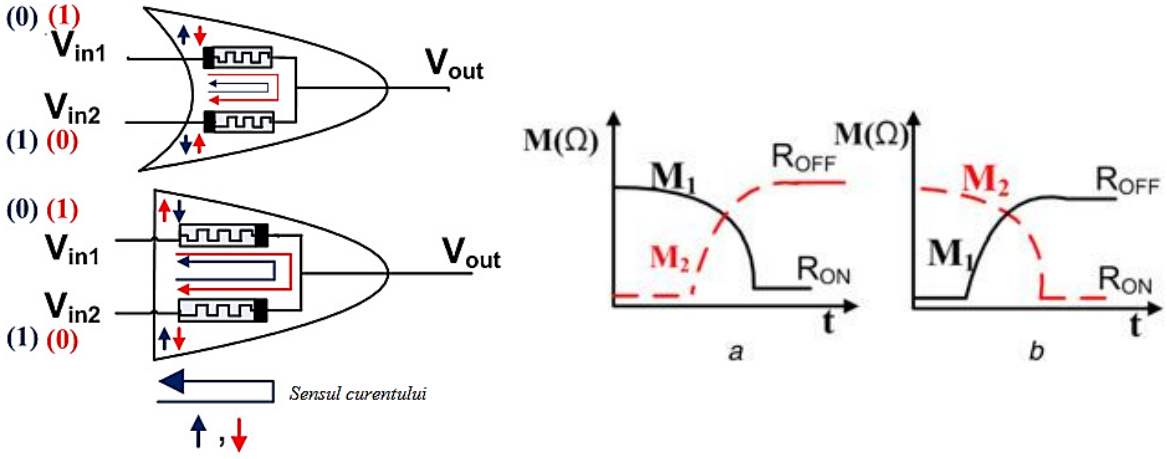


Figure 3.5 Logic gates with memristors. Memristence variation for *OR* (a), *AND* (b) logic gates [7]

Switching phenomena for such devices can be tracked by implementing logic gate circuits using the LTspice program. The modeling of the memristive element is performed using the same netlist file defined in APPENDIX 1, modifying the values of the initial parameters as presented in the subcircuits in APPENDIX 2.

CHAPTER 4

NEURONAL MODELING WITH THE HODGKIN-HUXLEY PRINCIPLE

4.1. INTRODUCTION

Researchers Hodgkin and Huxley discovered the existence of charging channels with sodium and ions distributed along the entire length of the axons, along with a so-called discharge channel, shown in Figure 4.1 [17].

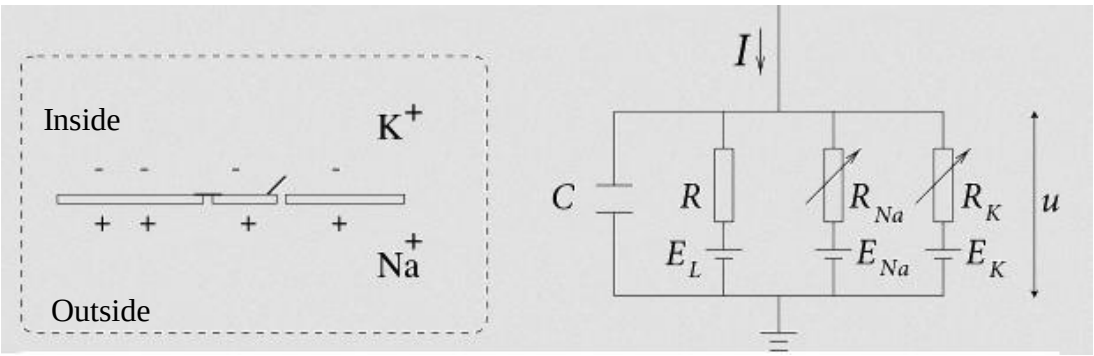


Figure 4.1 Electrical circuit of the Hodgkin Huxley model [19]

In the initial model described by Hodgkin and Huxley there are only 3 types of ion channels: sodium channels, illustrated by branch *(Na+)*, potassium channels, by branch *(K+)* and an unspecified draining channel modeled by branch *(R)* [17].

Ionic channels are described using the conductances g_{Na} for the sodium ion-channel, g_K for the potassium ion-channel, g_L for the draining channel, and through the gate variables *n* for potassium and *m* and *h* for sodium, respectively.

The present paper emphasizes that these ion channels presented in Chapter 4 are in fact active local memristors. Hence, the sodium and potassium ion channels in the brain have all the characteristics of memristors [22], [23] including the characteristic of Lissajous hysteresis loop that varies with the change in the frequency of the excitation signal [16], [4].

4.2. MEMRISTIVE MODEL OF HODGKIN-HUXLEY AXON

The purpose of this subchapter is to carry out a detailed study based on the model of the giant octopus axon (Hodgkin-Huxley) presented above and to highlight that it consists of two active memristors, more precisely contains a memristor for each ion channels, potassium respectively sodium.

4.2.1. POTASSIUN ION-CHANNEL MEMRISTOR

Leon Chua describes the memristive conductance of the G_K potassium ion channels in the Hodgkin-Huxley model as in fact 1st order memristors. The hysteresis characteristic presented by the memristors for potassium ion channels are analyzed in LT Spice according to the circuit described in APPENDIX 3, by applying periodic sinusoidal signals, the first of which is with an amplitude of 50mV and a frequency of 100Hz. The electrical subcircuit of the memristors related to the potassium ion channels has a symmetrical hysteresis characteristic around the origin illustrated in the i_K-v_K plane in figure 4.4, alongside the variation of the G_K memconductance versus the supply voltage v_K.

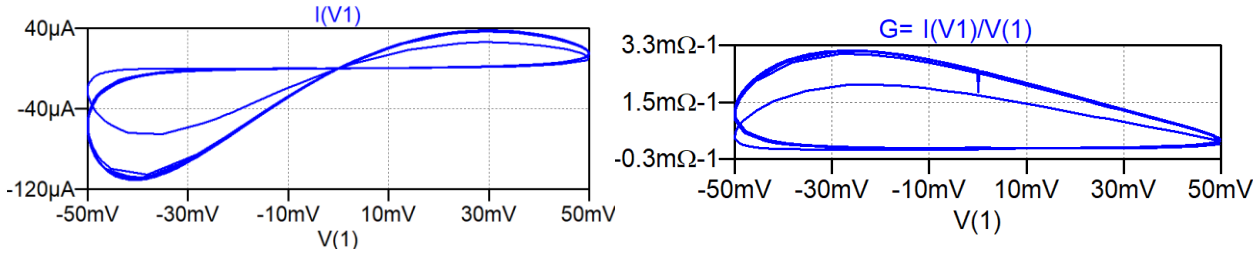


Figure 4.4 Hystrerezis loop $I_k=f(V_k)$. Memconductance variance G_K vs. the supply voltage v_K.

It was further considered a memristor for potassium ion channels, powered by a signal composed of a sinusoidal signal $A\sin(2\pi ft)$ and its N-order harmonic of amplitude B and phase shift Φ, so that $v_K(t) = A\sin(2\pi ft) + B\sin(2\pi Nft + \Phi)$, where N = 1,3,5 and represents the order of the original signal's harmonic, f is the 100Hz frequency, the signal's aplitude is A=B=50mV and phase shift is Φ=π/3.

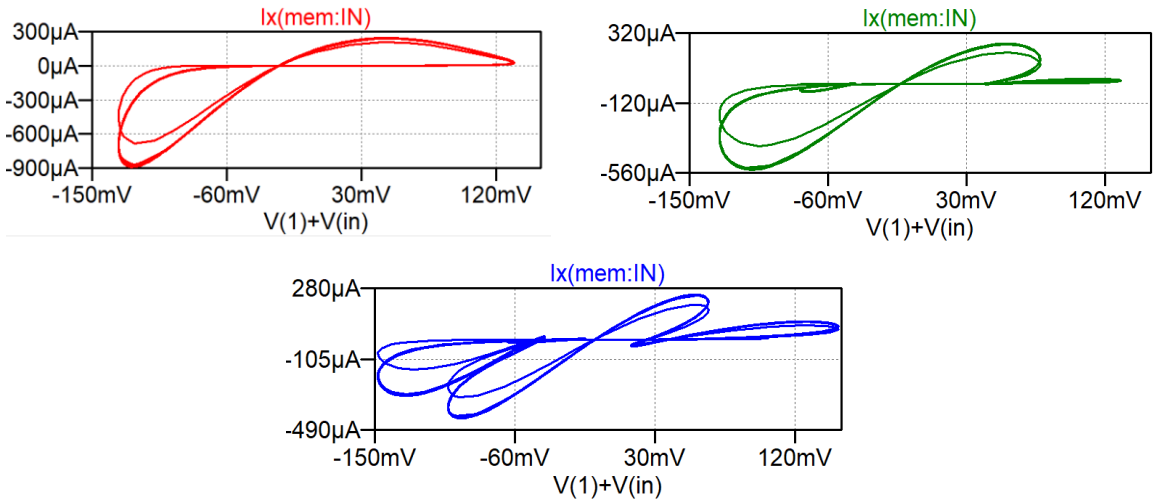


Figure 4.5. Hysteresis loop $I_k=f(V_k)$ for N = 1, 3, 5.

In a last step was considered a memristor for potassium ion channels powered by a signal composed of a sinusoidal signal $v_K(t) = A\sin(2\pi ft) + B\sin(2\pi Nft + \Phi)$, where N = 1,5,10,20 and and represents the order of the original signal's harmonic, f is the 100Hz frequency, the signal's aplitudes are A= 50mV, B=10mV and phase shift is $\Phi=\pi/3$.

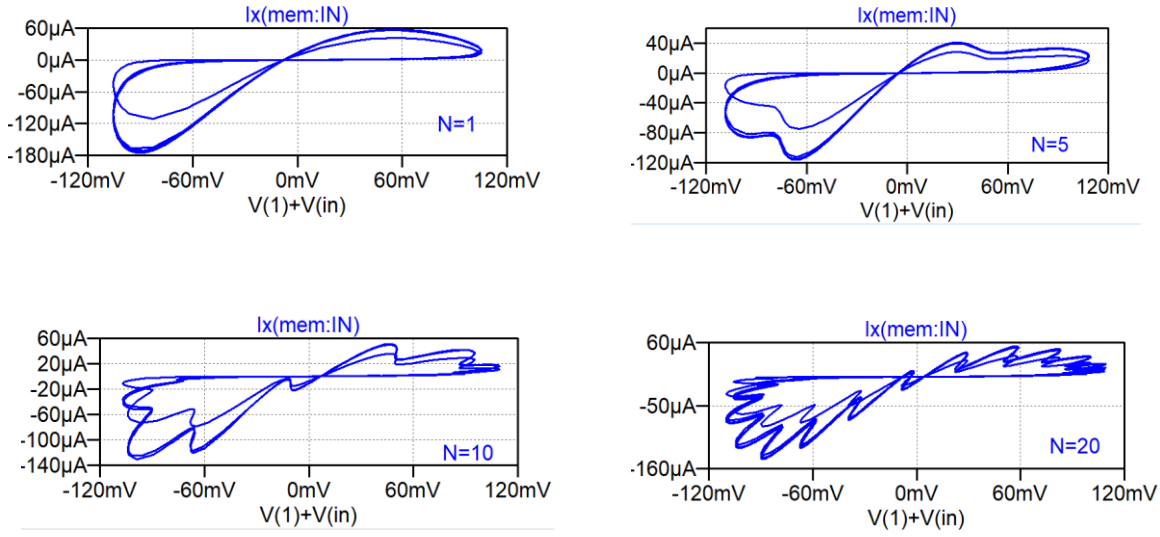


Figure 4.6 Hysteresis loop $I_k=f(V_k)$ for A=50mV, B=10mV, N=1,5,10,20

4.2.2. SODIUM ION-CHANNEL MEMRISTOR

In the same way, the equation that defines the model of sodium ion channels in the Hodgkin-Huxley model are in fact 2nd order memristors according to Leon Chua. The hysteresis characteristic presented by the sodium ion channel switches is analyzed in LT Spice according to APPENDIX 4 by applying periodic sinusoidal signals.

The first signal applied is a sinusoidal shape $v_{Na}(t) = A\sin(2\pi ft)$ of 120mV amplitude and 200Hz frequency, having the following initial values of the gate variables *m(0)=0, h(0)=0.003*. It was further considered a memristor for sodium ion channels, powered by a signal composed of a sinusoidal signal. $A\sin(2\pi ft)$ and its *N*-order harmonic of amplitude *B* and phase shift Φ so $v_{Na}(t) = A\sin(2\pi ft) + B\sin(2\pi Nft + \Phi)$, where N = 1,3,5 and represents the order of the original signal's harmonic, f is the 500Hz frequency, the signal's aplitude is *A*=*B*=50mV and phase shift is $\Phi=\pi/3$.

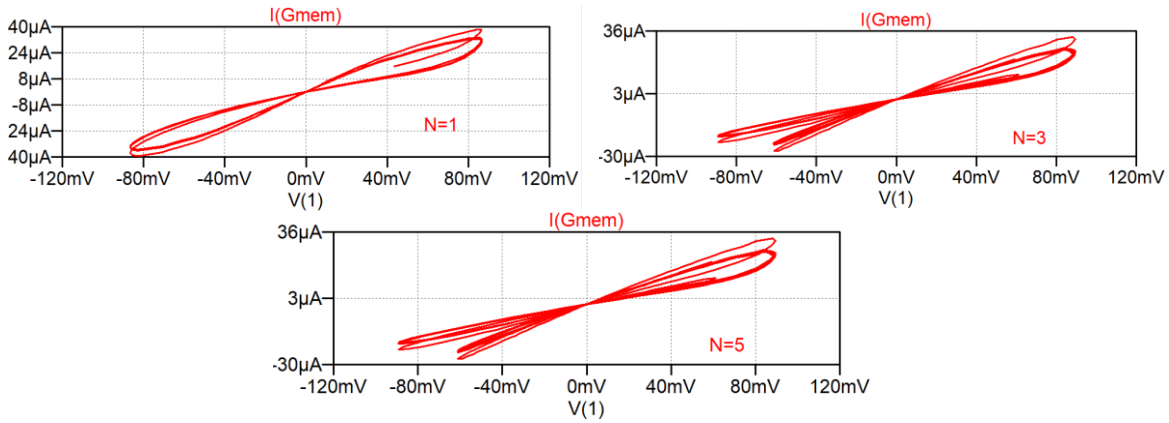


Figure 4.8 Hysteresis loop $I_{Na}=f(V_{Na})$ for *A*=*B*=50mV, *N*=1,3,5, $\Phi=\pi/3$

In a last step it was considered a memristor for sodium ion channels, powered by a signal composed of a sinusoidal signal $A\sin(2\pi ft)$ its *N*-order harmonic of amplitude *B* and phase shift Φ so $v_{Na}(t) = A\sin(2\pi ft) + B\sin(2\pi Nft + \Phi)$, where N = 1,5,10,20 and represents the order of the original signal's harmonic, *f* is the 500Hz frequency, the signal's aplitudes are *A*=50mV, *B*=15mV and phase shift is $\Phi=\pi/3$.

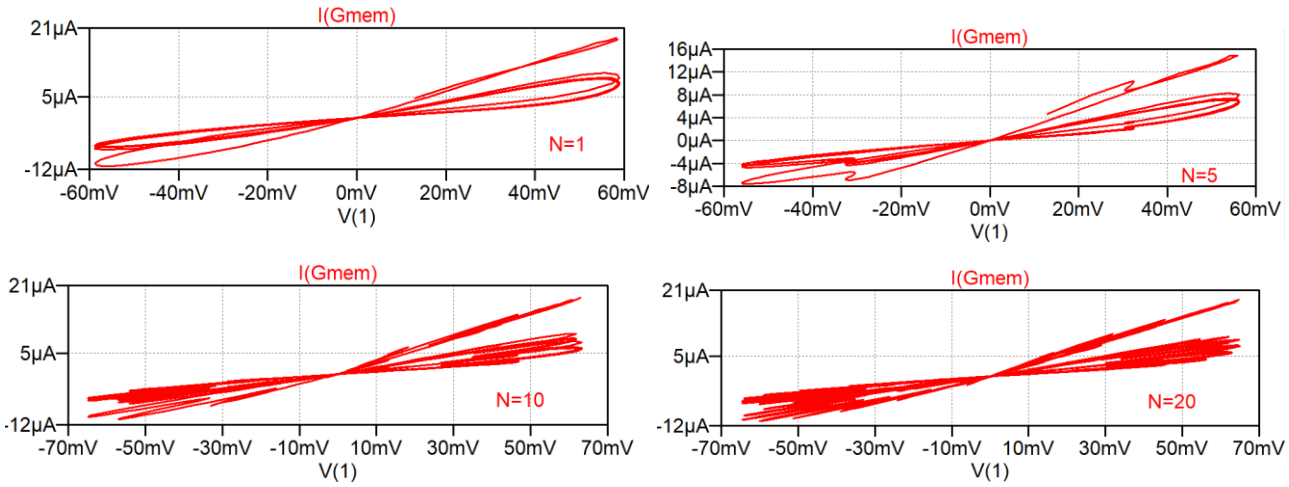


Figure 4.9 Hysteresis loop $I_{Na}=f(V_{Na})$ for A=50mV, B=15mV, N=1,5,10,20, $\Phi=\pi/3$

4.2.3. COMPUTATION OF HYSTERESIS LOOP AREA

This dependence of the hysteresis curve on the input signal's frequency is another property specific to memristors [25],it is detailed in this subchapter by applying a periodic input signal to a memristor, using LT Spice program, so that the two loops of $I = f(V)$ characteristic be obtained in 1 and 3 quadrants. Hence it illustrates the hysteresis curve orientation of potassium ion channel and sodium ion channel memristors for a periodic input signal using in LT Spice, according to the subcircuits in APPENDIX 3 and 4.

In the case of potassium ion channel memristor, the area A_{r+} has positive values for $t=T/2$, while A_{r-} has negative values, so that the orientation of the hysteresis loop is clockwise for $t<T/2$, counterclockwise respectively for $t>T/2$.

In the case of sodium ion channel memristor, the hysteresis loop's area in the 1st quadran, over the period $0<t<T/4$ varies from zero to positive values, so that a sub-loop with clockwise orientation is obtained, while for $T/4<t<T/2$ another sub-loop oriented counterclockwise is obtained because the area of the hysteresis loop migrates towards negative values. The hysteresis loop's area during $T/2<t<T$ takes only positive values and clearly illustrates the clockwise direction for the quadran 3 hysterezis loop.

4.3. MEMRISTIVE HODGKIN-HUXLEY MODEL

The purpose of this paragraph is to conduct a detailed study based on the entire model of the giant octopus axon and to highlight that it can be composed of two memristors related to potassium and sodium ion channels, presented in previous chapters.

A detailed study and characterization of this model are presented below through the equivalent electrical circuit and its specific waveforms [18]. To analyze the memristive's ion channels behavior, LT Spice program is used as it allows the simulation of topology illustrated in Figure 4.14 by defining the mathematical models of memristors with sodium and potassium ion channels.

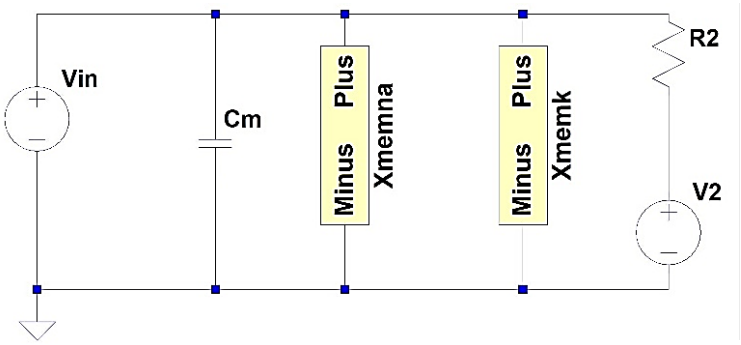


Figure 4.14 LTSpice topology of memristive Hodgkin-Huxley model

The two memristors $Xmem_{Na}$ și $Xmem_{K}$ where implemented by a .netlist attached in APPENDIX 3 and 4, alongside the entire Hodgkin-Huxley memristive model from ANEXA 5.

The circuit is supplied with a step voltage of 50mV amplitude and a transient analysis simulation is performed in order to study the time variation of supply voltage, ion currents and ionic conductances g_K, g_{Na}.

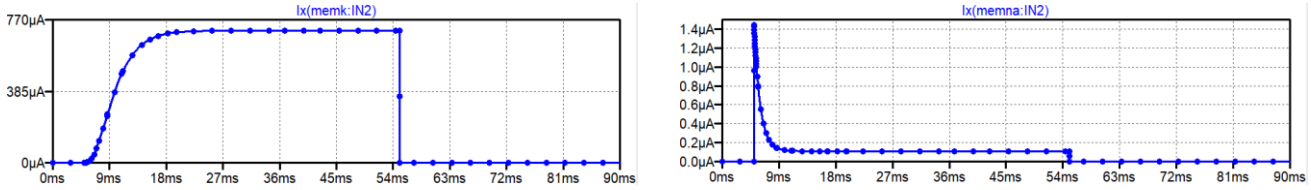


Figure 4.15 Electrical current for potassium and sodium ion-channel memristors

Subsequently, a sinusoidal supply voltage of amplitude 50mV with a frequency of 50Hz is applied and a transient analysis simulation is performed in order to study the memristors's characteristics.

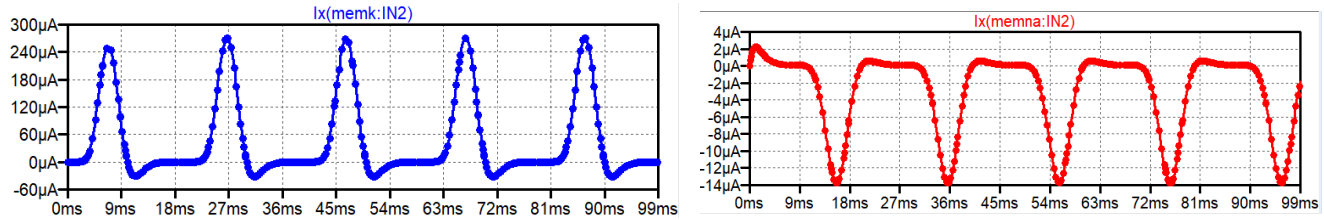


Figure 4.16 Electrical current for potassium and sodium ion-channel memristors

As can be seen from Figure 4.16, appling a sinusoidal input signal to the memristive system generates the absorption of a narrow pulses current during the period when the memristive elements are driven by a sinusoidal action potential of positive alternation.

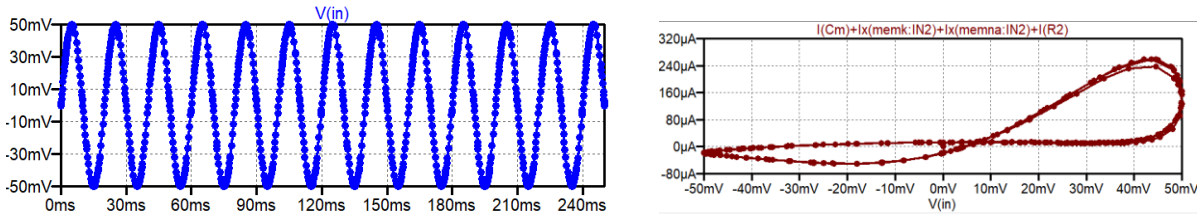


Figure 4.18 Supply voltage waveform and hysteresis loop of the memristive system $I_m = f(V_{in})$

CHAPTER 5

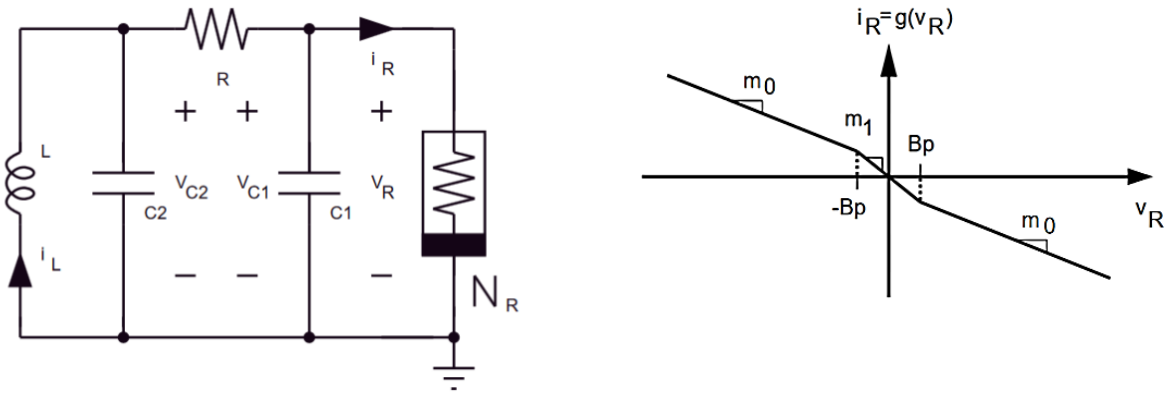
LTSPICE IMPLEMENTATION OF A MEMRISTIVE CHAOTIC OSCILLATOR

5.1. INTRODUCTION

Among the few electrical structures with chaotic behavior deliberately induced by the human factor is the Chua circuit, named after the engineer Leon Chua [32]. The Chua circuit is in this case an oscillator with a complex behavior, characterized by bifurcations of state and tendency to chaotic behavior. It consists of a coil, two capacitors, a resistor and a nonlinear element known as a "*Chua diode*" [20]. This chapter presents a chaotic circuit based on the traditional model of Chua's oscillator, but which combines the use of a traditional nonlinear resistor with the addition of a memristor made in HP laboratories (the memristive model presented in previous chapters). Therefore, the proposed mixed implementation links the old research papers that focused on diodes or operational amplifiers, with the current research papers that focus on memristors.

5.2. CHUA'S CHAOTIC OSCILLATOR

The Chua oscillator shown in Figure 5.1a is composed of an coil of inductance *L*, with internal resistance *r*, two capacitors with capacities *C1* and *C2*, a linear resistance resistor *R* and a nonlinear element N_R [21], [29].



a. b.

Figure 5.1 a Chua's chaotic oscillator. b. *I-V* nonlinear characteristic of N_R circuit element [21]

Following the simulations performed in the research published so far, it was observed that this circuit has an attractor with a particular form of "Double Scroll Atractor" that illustrates the phenomenon of state bifurcation.

The output of any circuit based on the Chua oscillator should meet two conditions to be recognized as chaotic [28], [32]:

1. Circuit variables (current and voltage) measured at any node of the circuit should be chaotic and random.
2. Chaotic attractors (voltage variation on one of the capacitors versus voltage on the other capacitor / coil current) should show the bifurcation phenomenon or approach it.

The only circuit element to be implemented is the nonlinear resistor N_R. There are several techniques that have been used in practical circuits, it can be synthesized using an operational amplifier with two bipolar transistors, two diodes and resistors (Matsumoto et al. 1986) [28] or two operational amplifiers and six resistors (Kennedy 1993) [29], [32].

In this paper I started from the LTSpice implementation of the circuit made by Matsumoto decribed by the topology shown in figure 5.2 and APPENDIX6 respectively.

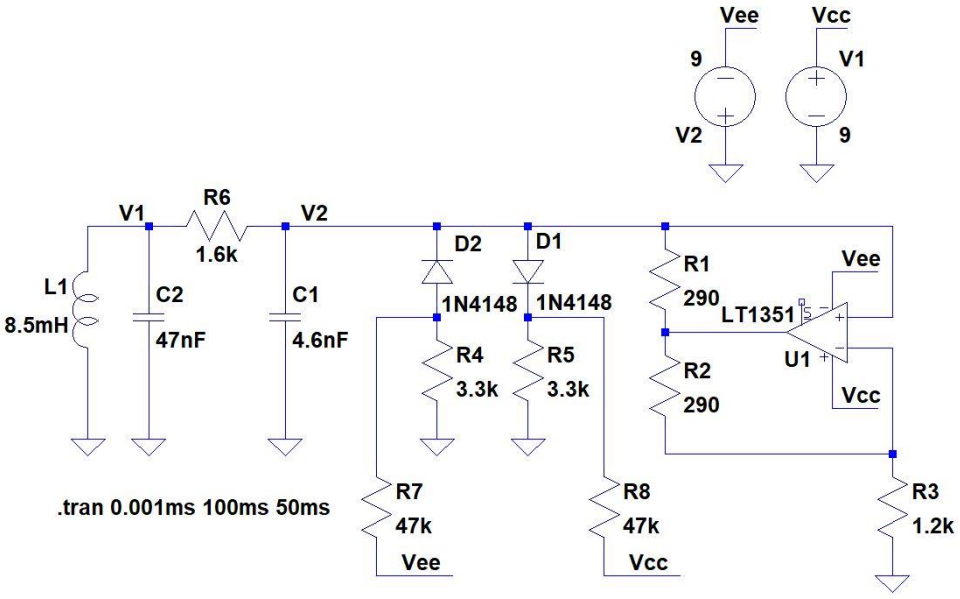


Figure 5.2 LTSpice Chua's oscillator topology

The circuit is being controled by a conductance related to the R6 resistor and as its value increases, the occurrence of of period doubling or bifurcation phenomenon of is noticed. By changing the resistance R6 in the range of values [0-2kΩ] it was found that for a value of 1.6K the circuit behaves like a periodic oscillator, Chua's double-scroll attractor is presented in figure 5.3.

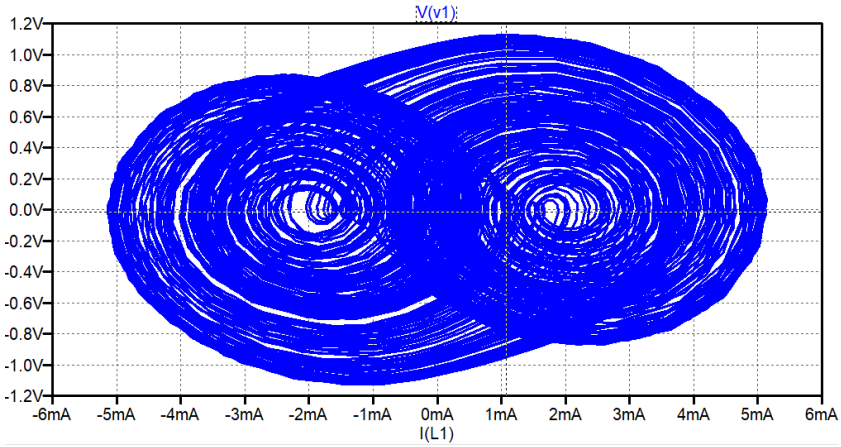


Figure 5.3 Bifurcation phenomenon for $R6 = 1.6k\Omega$

5.3. LTSPICE IMPLEMENTATION OF A MEMRISTIVE OSCILLATOR

The innovative element of this analysis is the addition of a non-linear memristive element within Chua'S oscillating circuit according to the topology presented in Figure 5.4 (Matsumoto model).

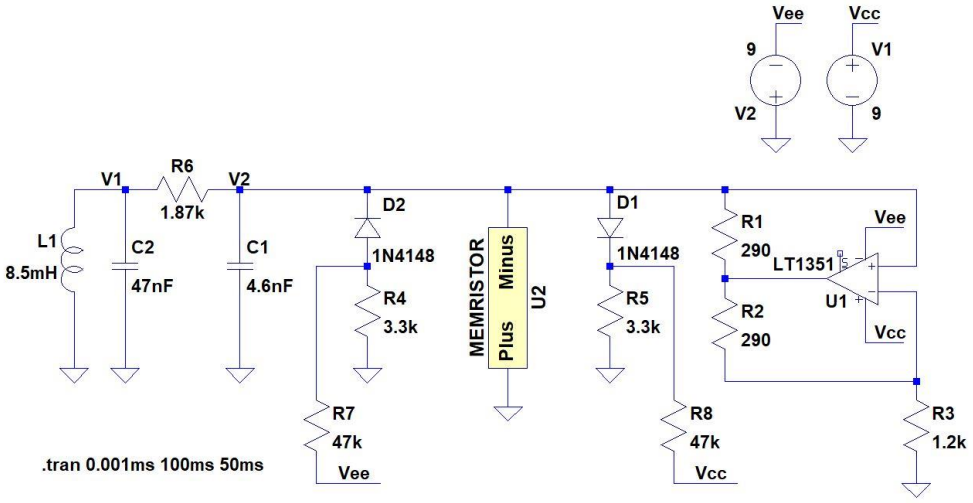


Figure 5.4 LTSpice topology of memristive oscillator

The output signal is analyzed by the voltage drop on capacitor *C2* and it can be seen that it is really chaotic and random, because it behaves like a very noisy signal, without any predetermined model thus fulfilling the first necessary condition for a chaotic system.

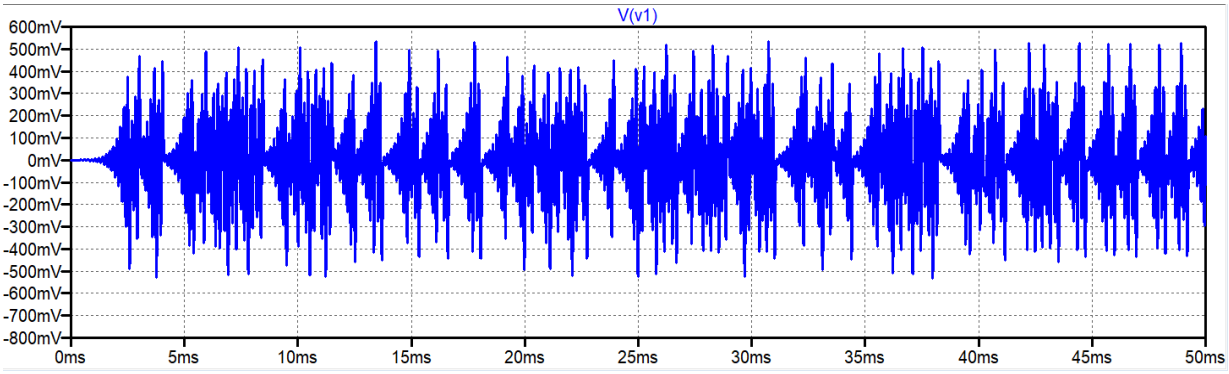


Figure 5.6 Output signal measured as the voltage drop on capacitor *C2*

The next checkpoint was to illustrate the chaotic attractor for the memristive system. The chaotic attractor is represented as a variable of the circuit in relation to another, in this case, the current in the inductor *L1* related tothe voltage at the terminals of the capacitor *C2*. The obtained graph is illustrated in figure 5.7 and the form of double scroll attractor can be observed, which satisfies the second condition for a chaotic system as it presents the bifurcation phenomenon.

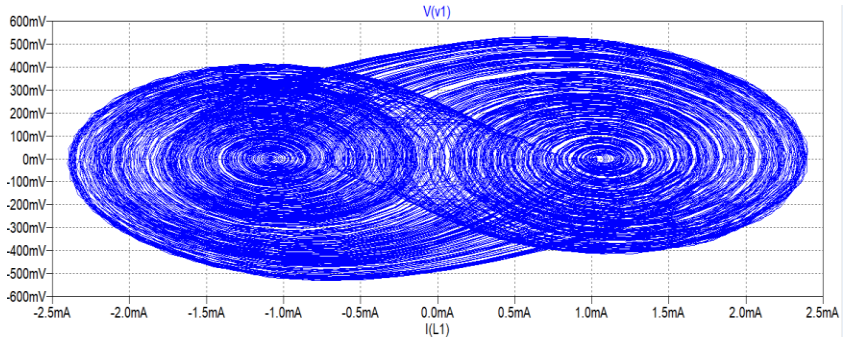


Figure 5.7 Double scroll attractor *I =f(V)* for the memristyve oscillator

By decreasing the R6 resistor's value from 2kΩ to 1.4kΩ, the memristive circuit transitions from the period bifurcation phenomenon (figure 5.8.a and b), to Chua's Spiral attractor (figure 5.8.c), followed by the double-scroll attractor (figure 5.8.d) and finally at the occurrence boundary crisis phenomenon (figure 5.8.e).

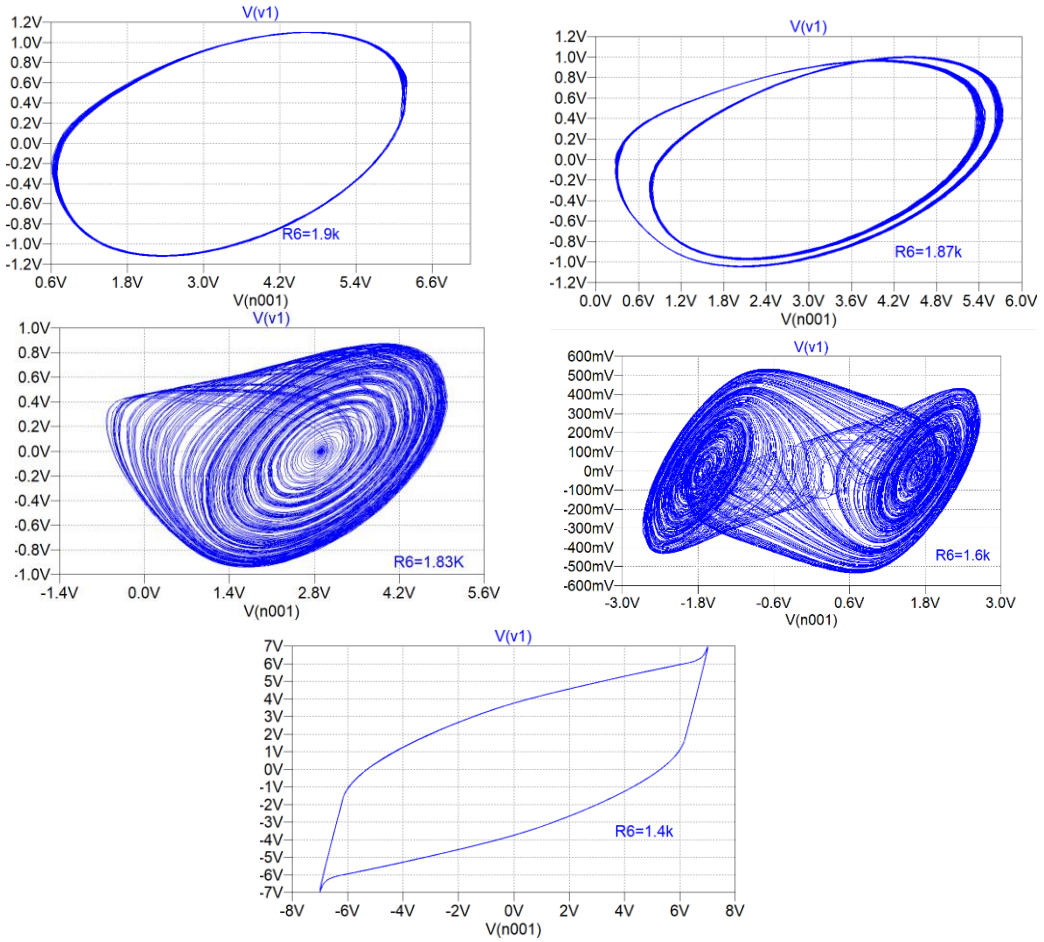


Figure 5.8 Typical bifurcation sequences encountered (horizontal axis *V2*, vertical axis *V1)*: (a) *R6* = 1.9 kΩ *period-1*, (b) *R6* = 1.87 kΩ *period-2*, (c) *R6* = 1.83 kΩ Chua's spiral attractor, (d) *R6* = 1.6 kΩ double-scroll attractor, (e) *R6* = 1.4 kΩ boundary crisis phenomenon.

Finally, to ensure that this random characteristic of the electrical current comes from both diodes and memristor, the currents of each component are shown in Figure 5.9 and it can be clearly seen that each component of the total current contributes equally to the randomness of the circuit.

Figure 5.9 a) Electrical current for *D1*, *D2*, Memristor components
b) Electrical current for *L1* coil

Another common implementation for the nonlinear resistor N_R, with *I-V* characteristic shown in figure 6.5 is achieved by connecting in parallel two negative resistance converters (Kennedy model) [37], [39] as shown in Figure 5.10.

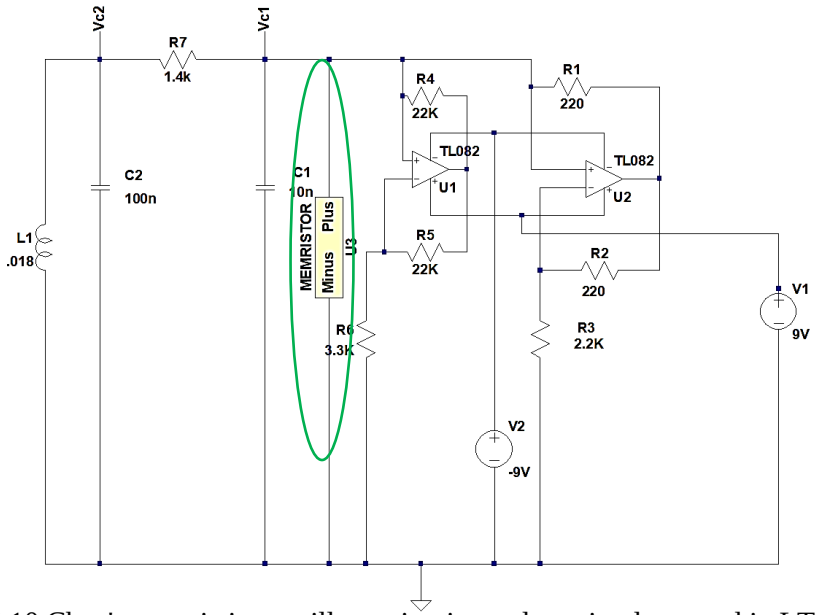


Figure 5.10 Chua's memristive oscillator circuit topology, implemented in LTSpice

The circuit dynamics is studied in the same way presented in the previous paragraph, by changing the R7 value of the resistor from 0 to 2kΩ. As expected, as its resistance increases, the period doubling phenomenon is obtained leading to chaotic behavior as illustrated in the sequences in Figure 5.11. Another interesting phenomenon observed is that a change in control resistance's values also causes a change in size for each attractor obtained. Therefore, the orbit of period - 1 is large, that of period - 2 is smaller, that of period - 4 even smaller, and in the end it decreases visibly before disappearing completely [32], [40].

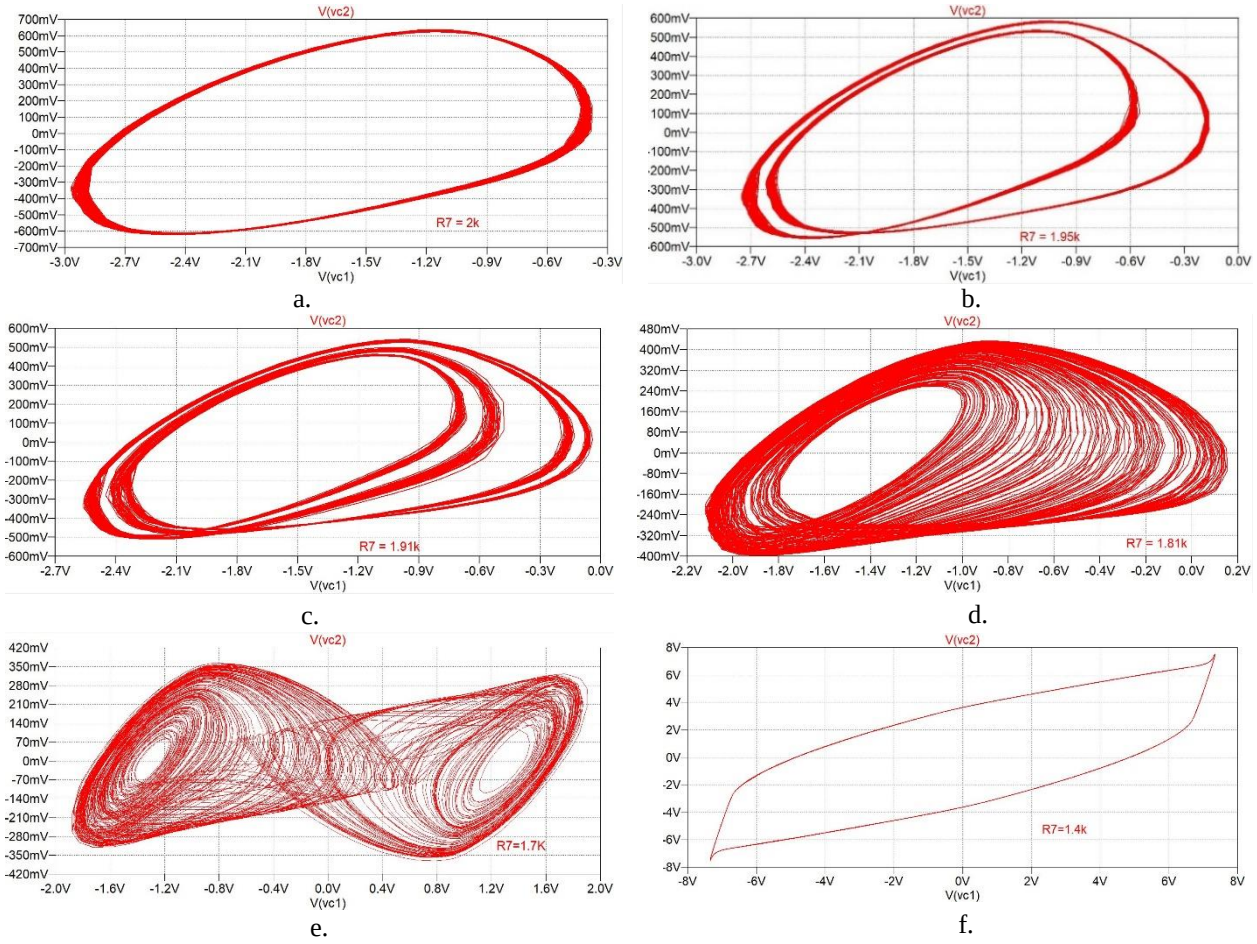


Figura 5.11. Typical bifurcation sequences encountered (horizontal axis *V2*, vertical axis *V1*): (a) *R7*= 2 kΩ *period-1*, (b) *R7* = 1.95kΩ *period -2*, (c) *R7* = 1.83kΩ *period -4*, (d) *R7* = 1.72 kΩ Chua's spiral attractor, (e) *R7*= 1.6 kΩ double scroll attractor, (f) *R7* = 1.4 kΩ boundary crisis phenomenon.

CHAPTER 6
CONCLUSIONS

6.1 GENERAL CONCLUSIONS

The SPICE model analyzed in Chapter 3 is represented by a subcircuit with two terminals whose parameters can be easily defined when using the memristive device in any electrical circuit. The possibility of using these emerging devices in logic gates was also considered.

Following the analysis of sodium and potassium ion memristive channels presented in Chapter 4 of this paper, symmetrical hysteresis characteristics were obtained, characteristic that narrows as the frequency of the supply signal increases, unique characteristics of memristors. Therefore, the use of memristive systems to manufacture artificial neural networks of dimensions comparable to the human brain could become possible.

In Chapter 5, I proposed a new way of implementing a chaotic oscillator using an HP memristor integrated into the well-known Chua circuit, starting from the models defined by Matsumoto and Kennedy. The simulations of the proposed electrical circuits show that the proposed memristive systems managed to maintain the chaos and randomness presented by the traditional Chua circuit.

6.2 CONTRIBUTIONS

Below are briefly presented the original personal contributions that this thesis brings in the field studied addressing the following issues:

- ✓ Main models of memristors from the literature are presented, alongside the numerous attempts to use them in complex memristive circuits from different areas of applicability. It identifies the methods of analysis, modeling, simulation and design of memristive analog circuits and illustrates the benefits of using the LTSpice program in their analysis.
- ✓ Adding a memristor to the LTSpice library, based on the mathematical model and the equivalent electrical circuit described in a *netlist* file, and modeling the behavior characteristic of "memory".

- ✓ Identifying the memristor's definition parameters at time t_0 for which the hysteresis curve specific to memory devices is obtained and highlighting its degeneration at a straight line, in which case it behaves like a normal resistor.
- ✓ Outlining the possibility of using the memristor defined in LTSpice to ensure the switching phenomenon within memristive logic gates, thus benefiting from reduced circuit dimensions and lower power consumption.
- ✓ Carrying out the study of the neural model proposed by Hodgkin and Huxley and analyzing the possibility of modeling ion channels through memristive channels with sodium and potassium ions in LTSpice.
- ✓ The proposal of adding a memristor within the subcircuit of the nonlinear element in Chua's oscillator and the analysis of the circuit dynamics using LTSpice program, starting from two topologies often encountered in scientific papers.
- ✓ Determining the optimal values of memristor's initial parameters and of the control resistance that ensures the chaotic behavior of the proposed circuit as well as highlighting the specific attractors.

6.3 FUTURE DIRECTIONS

Regarding the future development perspectives related to the models studied in this paper, the SPICE model presented in this paper could be improved in a later study by adding a second active layer in order to obtain a better response to frequency variation.

At the same time, memristors have all the necessary characteristics to emulate a network of electronic neurons capable of learning, adapting, making decisions and can represent in the future a solid basis in building intelligent, conscious computers, like an electronic brain. A future research suggestion that combines the studies conducted in previous chapters with the current one is the use of memristors to synchronize a network of two neurons.

In the case of proposed chaotic circuits, in order to further study their dynamics, bifurcation diagrams should be constructed, which also helps to determine at what exact values the circuit becomes chaotic. Synchronizing chaotic circuits may be another point of future study.

This paper allows a broad comparison of memristive models because all topologies can be easily implemented in a single program, LTSpice, and used in further studies.

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APPENDIX

APPENDIX 1 – Modelarea memristorului în LT Spice

APPENDIX 2 - Circuite porți logice memristive ȘI, SAU

APPENDIX 3 – Modelarea memristorului pentru canalul cu ioni de potasiu alimentat de un semnal sinusoidal

APPENDIX 4 - Modelarea memristorului pentru canalul cu ioni de sodiu alimentat de un semnal sinusoidal

APPENDIX 5 - Modelarea sistemului memristiv Hodgkin-Huxley

APPENDIX 6 – Modelarea oscilatorului lui Chua (topologie Matsumoto fără memristor**)**

APPENDIX 7 - Modelarea oscilatorului Chua (topologie Matsumoto cu memristoare)

APPENDIX 8 - Modelarea oscilatorului Chua cu (topologie Kennedy cu memristor)