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Summary of PhD Thesis

COMPLEX INTEGRATED CIRCUITS IN THE RADIATION ENVIRONMENT AT THE LHCB HIGH ENERGY PHYSICS EXPERIMENT AND EXTRAPOLATION TO THE CASE OF SPACE-BASED EXPERIMENTS

PhD Candidate: **Eng. Vlad-Mihai PLĂCINTĂ**

DOCTORAL COMMITTEE

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Scientific Coordinator	**Cristian RAVARIU, PhD**	from	**University POLITEHNICA of Bucharest**
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List of abbreviations

ADC – Analog-to-Digital Converter

ASIC – Application Specific Integrated Circuit

BiCMOS – Bipolar Complementary MOSFET

BJT – Bipolar Junction Transistor

BRAM – Block RAM

C-Cell – Combinational Cell

CERN – European Organization for Nuclear Research

CHARM – CERN High Energy Accelerator Mixed Field Facility

CL – Confidence Level

CMOS – Complementary MOSFET

CRAM – Configuration RAM

DAC – Digital-to-Analog Converter

DAQ – Data Acquisition

DD – Displacement damage

DUT – Device Under Test

FF – Flip-Flop

FPGA – Field Programmable Gate Array

GUI – Graphical User Interface

HDMI – High-Definition Multimedia Interface

HEP – High Energy Physics

HfO_2 – Hafnium Dioxide

ISS – International Space Station

JEM-EUSO – Joint Experiment Missions for Extreme Universe Space Observatory

JTAG – Joint Test Action Group

LET – Linear Energy Transfer

LHC – Large Hadron Collider

LHCb – Large Hadron Collider beauty

LUT – Look-up Table

LVDS – Low Voltage Differential Signaling

MaPMT – Multi-Anode Photomultiplier Tube

MBU – Multi Bit Upset

NIEL – Non-Ionizing Energy Loss

NMOS – N-channel MOSFET

PCB – Printed Circuit Board

PDMDB – Photodetection Module Digital Board

PMOS – P-channel MOSFET

R-Cell – Register Cell

RAM – Random Access Memory

SCR – Silicon Controlled Rectifier

SE – Single Ended

SEE – Single Event Effects

SEL – Single Event Latch-up

SBU – Single Bit Upset

SEU – Single Event Upset

Si – Silicon

SiGe – Silicon Germanium Technology

SiO_2 – Silicon Dioxide

SPACIROC – Spatial Photomultiplier Array Counting and Integrating Readout Chip

SRAM – Static Random-Access Memory

TCP/IP – Transmission Control Protocol/Internet Protocol

TID – Total Ionizing dose

TSMC – Taiwan Semiconductor Manufacturing Company

UART – Universal Asynchronous Receiver-Transmitter

UHECR – Ultra-High Energy Cosmic Rays

Chapter 1
Introduction

The semiconductor devices with strong reliability represent a constant demand for safety-critical applications that include experiments in the area of nuclear engineering, e.g. accelerator and aero-space experiments. By their nature, such experiments involve harsh environments with radiation background, and this represent a permanent threat to the operation of their electronics.

1.1 PhD Thesis Domain

Commercial-grade components are sometimes suitable to use in such harsh environments with radiation background. However, the reliability issues due to radiation may generate very serious electronics – and sensors, though not discussed here - design challenges.

When such components are considered to be used in a radiation environment, they have to be tested and qualified before in an equivalent radiation environment. However, such qualification procedure is a very complex activity that involves test facilities and specialized human resources for the design of an irradiation setup to control and monitor the tested circuit under radiation. Further, the data analysis and interpretation are important to understand how the radiation interact with the investigated device semiconductor structure. The only straightforward solution is to exposure the circuit to a charged particle beam and measure its response. The measured results can be extrapolated to the experiment radiation environment.

1.2 PhD Thesis Purpose

Scheduled during 2019-2020, the second long shutdown of the LHC accelerator gives the time window for the first upgrade of the Large Hadron Collider beauty (LHCb) experiment [1] at CERN.

The purpose of the present PhD thesis is focused on the radiation hardness qualification for three complex electronic integrated circuits: one ASIC and two commercial-grade FPGA

technologies. The ASIC was designed to operate in cosmic space, within the JEM-EUSO experiment [2] and onboard at the ISS. The FPGA circuits were proposed to be used in the digital readout of the LHCb-RICH sub-detectors during the first phase of its 2019 - 2021 upgrade program.

1.3 PhD Thesis Content

The first chapter provides an introduction that includes the purpose and motivation of this work, and a general description of the radiation environments especially those from cosmic space and within the high energy physics experiments from CERN. Also, the LHCb experiment and its RICH subdetectors are described.

The second chapter describes how radiation interacts with matter (e.g. semiconductor layers) and provides a better description of how the radiation may induce failures into the electronic integrated circuits.

The third chapter presents the radiation testing of the SPACIROC2 ASIC done with different particle beams: ions, protons, and X-Rays. Several methodologies and strategies are proposed and described to detect, measure and mitigate the radiation effects. The test beam results and the conclusions are given at the end of the chapter.

The fourth chapter presents the irradiation campaign carried out on a SRAM-based FPGA from Xilinx KINTEX-7 family. The FPGA was exposed to different particle beams: protons, ions, X-Rays and mixed fields. Various testing procedures and methodologies to detect, measure and to mitigate the radiation-induced failures are proposed and described. Based on the measured results, conclusions are established, and extrapolated to the LHCb-RICH environment.

The fifth chapter presents the radiation testing of the Axcelerator antifuse FPGA from Microsemi (now Microchip) with proton and X-ray particle beams. Several testing methodologies are proposed and described in this chapter. Based on the irradiation results, conclusions are drawn and the results are extrapolated to the LHCb-RICH environment.

The last chapter provides the overall conclusions of the extensive irradiation campaign considering the results, the original contributions, as well as the conference/workshop/school participations and the scientific papers published by the author and which are relevant to this PhD thesis. The plans for future are also outlined following the next phase of the LHCb Upgrade, the phase II beyond 2030.

Chapter 2
Radiation Damage in Semiconductor Devices

2.1 Specific Parameters for Radiation Effects in Electronic Devices

The radiation effects in semiconductor devices are triggered through the following mechanisms: *ionization* and *displacement damage*. Following these effects, the electrical parameters of the devices are altered in a way that may cause either parametric or functional failure. They are classified in cumulative and single event effects (SEEs) as shown in fig. 2.1.

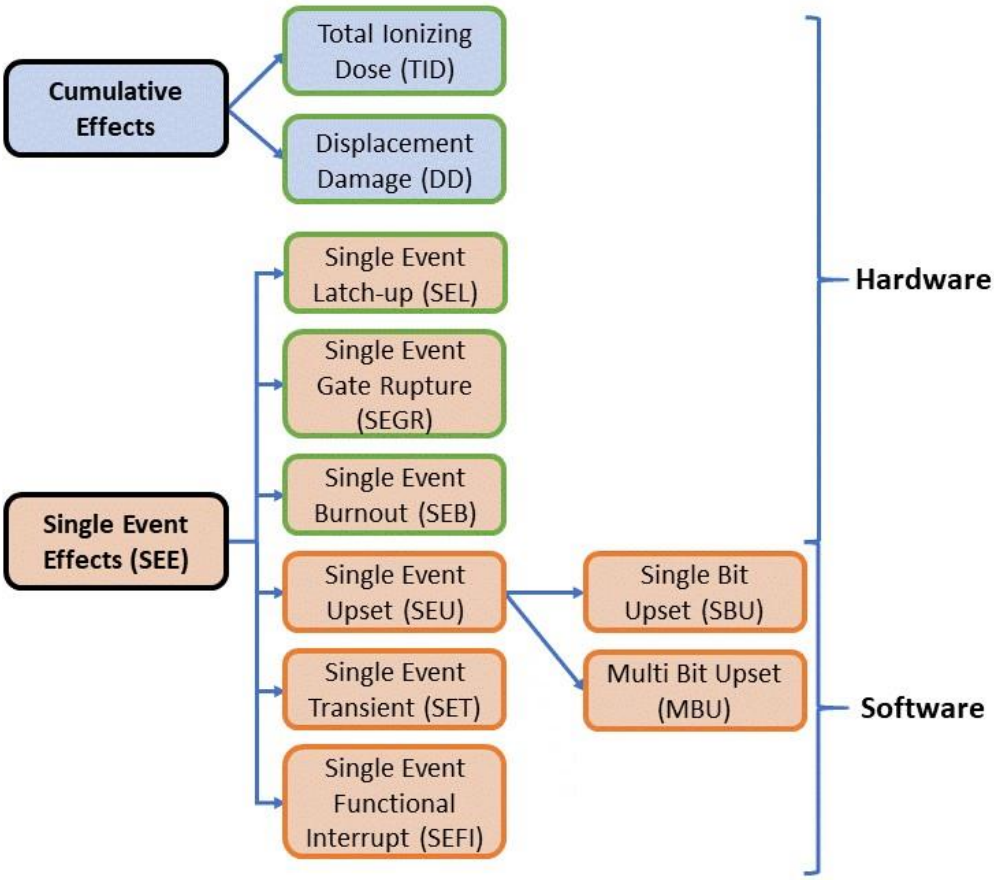

Fig. 2.1 *Classification of radiation effects in semiconductor devices*

2.2 Cumulative Physical Effects in Solid-State Devices

Cumulative effects [3] are due to accumulation of charges or defects into circuit layers during the exposure time of a given electronic device to a radiation environment. They are subclassified in two categories: Total Ionizing Dose (TID) and Displacement Damage (DD) effects.

2.2.1 Total Ionizing Dose

The performance of electronic devices may be degraded by the dose accumulated in the oxide dielectric layers, which usually are SiO_2 or HfO_2 (as gate dielectric) in modern CMOS electronics [4]. Through ionization, electron-hole (e-h) pairs are generated, and they can be separated in local electric fields. Trapped holes in the insulator layer or acceptors/donors at the Si-SiO_2 interface are possible mechanisms for the production of localized charges. These lead to aging and improper operation of the electronic devices.

TID effects in electronic devices depend on the technology type. Bipolar technologies manifest increased leakage currents and gain degradation due to radiation [5]. CMOS technologies are also affected by TID effects and are manifesting various failures like: decrease of transconductance, increased noise, increase in leakage currents and threshold voltage shifts [6].

In this thesis, *the TID-induced leakage current* is defined as a global excess of the current consumption within the integrated circuits under radiation exposure [7].

2.2.2 Displacement Damage

The particle/nucleus non-ionizing energy loss (NIEL) in Si leads to dislodging of atoms from their semiconductor lattice, leading to morphological changes within the semiconductor structure known as displacement damage, which is further highlighted in degradation of the electrical characteristics. The displacement damage is a gradual effect and is usually given as function of the number of 1 MeV equivalent neutrons per given area, **1 MeV neq. /cm^2.** However, it is also (approximately) proportional to the NEIL, and it is expressed in **MeV · cm^2/g** [8].

2.3 Single Event Effects and Functional Failures in Integrated Circuits

2.3.1 Single Event Effects – Physical Mechanisms

Single event effects (SEEs) are generally due to the path of a single high energetic and high-Z (Z > 2) particle passing through the device semiconductor layers while losing its energy through ionization. Following ionization process, a very localized charge is deposited in the semiconductor material, and if it is higher than a given threshold value, known as the critical charge (Q_c) [9], then the SEE probability of production is high. The critical charge is generated by particle energy deposition in a critical volume within the device. The region where the charge collection mechanism takes place, and where the SEE is created, is known as the sensitive volume.

Depending on how they may be affecting the integrated circuits, the SEEs can produce various software and hardware functional failures that may be temporary, quasi-permanent or permanent. High energy hadrons like GeV proton and pion particles could cause nuclear reactions and ions could result with keV to MeV energies, which in turn generate SEE - an indirect SEE production.

2.3.2 Single Event Transient

Transient effects may occur due to a single particle strike into the semiconductor layer and manifest as a temporary perturbation that may be propagated forward into the circuit leading in certain cases to malfunction of the device. These are known as single event transients (SETs) and are present as a glitch or a parasitic-induced pulse that is described by the shape, width/duration and amplitude [10].

2.3.3 Single Event Upset

Localized charge depositions into the semiconductor layer due to particle strikes may also lead to software errors like bit-flips within digital circuits. The bit changes are possible in memory cells, Flip-Flops (FF), look-up tables (LUT) or other digital logic resources. These

are known as single event upsets (SEUs) and are non-destructive radiation-induced effects. Depending on how many bits are changed by a single particle strike, the SEUs are classified in: Single Bit Upset (SBU) and Multi bit Upset (MBU).

2.3.4 Single Event Functional Interrupt

The single event functional interrupt (SEFI) is another software SEE that manifests as a temporary non-functional state of a device. Usually, in modern circuits, such as FPGAs, SEFI manifest as: induced restart/reset while under operation, complete freezing, partially or fully data loss of the program/configuration or by an unknown state of operation. SEFIs are mitigated only when an external operation is performed: either full power cycle or sometimes through a reconfiguration, if the procedure itself is accessible [11].

2.3.5 Single Event Latch-up

Single event latch-ups (SELs) are hardware failures that are manifesting as high current states between the power lines in a CMOS structure as consequence of a particle strike [12]. In a CMOS inverter there are inherently two parasitic bipolar transistors, which in normal operating conditions function as PMOS and NMOS transistors. Yet, this two-transistor configuration forms a p-n-p-n structure that might under certain condition function as thyristor or silicon-controlled rectifier (SCR). If the deposited charge is large enough, it can enable the bias for either one of the parasitic transistors, which cause the SCR structure to be activated, hence a short-circuit between the power lines is enabled. It can be recovered only through a power cycle, or an induced an localized voltage reduction on the specific power line.

2.3.6 Single Event Gate Rupture and Single Event Burnout

Two destructive and permanent radiation-induced SEEs can be triggered by a particle strike causing a permanent conductive path: single event gate rupture (SEGR) and single event burnout (SEB). SEGR is a catastrophic failure affecting only power MOSFETs, while SEB is possible in all power devices (MOS and BJT transistors, diodes) when they are in the “off” state.

Chapter 3
Characterization of the SPACIROC2 ASIC Under Radiation Exposure

The **S**patial **P**hotomultiplier **A**rray **C**ounting and **I**ntegrating **R**eadout **C**hip (SPACIROC) [13] family is a mixed signal and full readout front-end ASIC family designed to fulfill the readout of photomultiplier tube signals, while being optimized for 64-channel MaPMTs. It was designed to cope with the requirements of the **J**oint **E**xperiment **M**issions for **E**xtreme **U**niverse **S**pace **O**bservatory (JEM-EUSO) in terms of photodetector front-end readout.

3.1 SPACIROC2 ASIC Description

The SPACIROC2 ASIC was designed by Omega MICRO group in close collaboration with JEM-EUSO group. It was fabricated in a 0.35 μm SiGe BiCMOS technology node with an active area of ~19 mm^2 (4.6 mm x 4.1 mm).

The ASIC has 64 inputs with negative polarity that are compliant with the MaPMT readout requirements. It provides close to 100 % trigger efficiency for a measured charge higher than 50 fC, which corresponds to one third of photoelectron charge (1/3 p.e.).

3.2 Experimental Setup and Testing Routines

An experimental setup in compliance with various radiation testing standards was proposed and designed to power, monitor and characterize the SPACIROC2 ASIC – named the DUT from now on within this chapter – while performing laboratory tests as well as under ionizing radiation conditions [14]. Its architecture is shown in fig. 3.4. The setup is composed from the following parts: power supply block, the DAQ system, the DUT test board, an arbitrary wave generator as a pulser, and two personal computers (PC).

The DUT test board embeds the ASIC, and it has all the required components to ensure full operation. The pulser was used to generate a test pulse to be injected into the test board in order to simulate a 1 p.e. signal needed for trigger efficiency measurements.

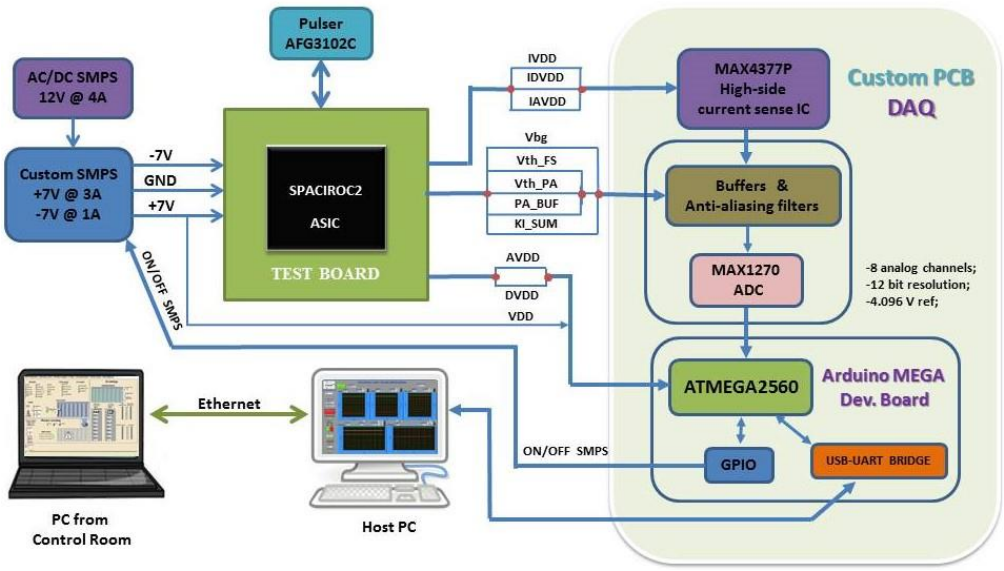

Fig. 3.4 *The experimental setup architecture designed to characterize the SPACIROC2 -self citation [14]*

The power supply block ensures the power requirements for powering the DUT test board by providing two independent voltages of +/- 7 V with respect to the ground.

The DAQ system is designed around a commercial development board that embeds the ATMEGA2560 8-bit microcontroller [15]. It provides power management and monitoring on both the analog and digital cores as well as monitoring of other internal signals (e.g. analog probes, voltage references etc.). The system is connected through an UART communication to a LabVIEW GUI. The GUI ensures full control of the experimental setup and the measured data are displayed on graphs and saved in computer files for later analysis.

The monitoring strategy as well as the testing routines used before, during and irradiation were established together with the DUT design team. In this way a compressive set of electrical parameters and characteristics were measured. Therefore, based on data collected while the DUT was irradiated as well as after the irradiation, the cumulative effects measurements and SEE rates were highlighted in user display and recorded on the hard-disk.

3.3 Test Beam Results and Analysis

The SPACIROC2 circuits were tested in radiation by using ions, protons and X-rays particle beams from the following facilities:

- Ions at SIRAD [16] facility from Legnaro National Laboratories in Italy;

- 200 MeV protons at the proton irradiation facility (PIF) [17] at the Paul Scherer Institute in Switzerland;
- 35 MeV protons at the 2.88 GeV Cooler Synchrotron COSY-Jülich [18] at Juelich Research Center in Germany (Julic cyclotron pre-accelerator);
- X-rays at the X-ray radiation facility [19] from Padova University in Italy.

3.3.1 Ion Irradiation

Two types of ions, ^{16}O and ^{20}Si, with an LET of about (2.85 +/- 0.29) MeV cm^2/mg and about (8.59 +/- 0.86) MeV cm^2/mg, respectively, were used to test the DUT and to measure SEEs rates with different inclination angles and with a fluence up to (1.5 +/- 0.3) $\cdot 10^7$ ions/cm^2. Two SEU cross-section values function of effective LET – upsets in the configuration registers - were measured (with a CL of 95 %): between 0.13 $\cdot 10^{-6}$ cm^2/DUT and 9.5 $\cdot 10^{-6}$ cm^2/DUT for a LET of about (8.59 +/- 0.86) MeV cm^2/mg and between 1.4 $\cdot 10^{-6}$ cm^2/DUT and 20 $\cdot 10^{-6}$ cm^2/DUT for a LET of about (11.15 +/-1.1) MeV $\cdot$ cm^2/mg. No SEL was observed. The observed SEUs were corrected by a full reconfiguration of the DUT.

3.3.2 35 MeV Proton Irradiation

One DUT test board was tested with 35 MeV protons beam at different dose rates and up to (150 +/- 7.5) krad (Si) TID that corresponds to a fluence of (7 +/- 0.35) $\cdot 10^{11}$ protons/cm^2. At these very high and unrealistic dose-rates, functional failures were observed in various build-in blocks, especially the DACs.

An increase of leakage currents, mostly visible in the digital core of the ASIC, was observed due TID effects, see fig. 3.32. However, a very fast room-temperature recovery process was visible in absence of the beam.

For these TID rates, the build-in DACs start to lose their monotonicity at a TID threshold between 80 and 100 krad (Si). After 100 krad (Si) the DACs suffer complete failure. In fig. 3.34 it can be observed the linearity measurements for 2 embedded DACs, during the proton irradiation runs as well as after a 10-h room-temperature recovery process over 10 hours.

The DUT recovered completely after a few days of recovery in unbiased off-state mode, with no permanent or residual failures observed, compared with the state before irradiation. No SEEs were observed during irradiation with 35 MeV protons.

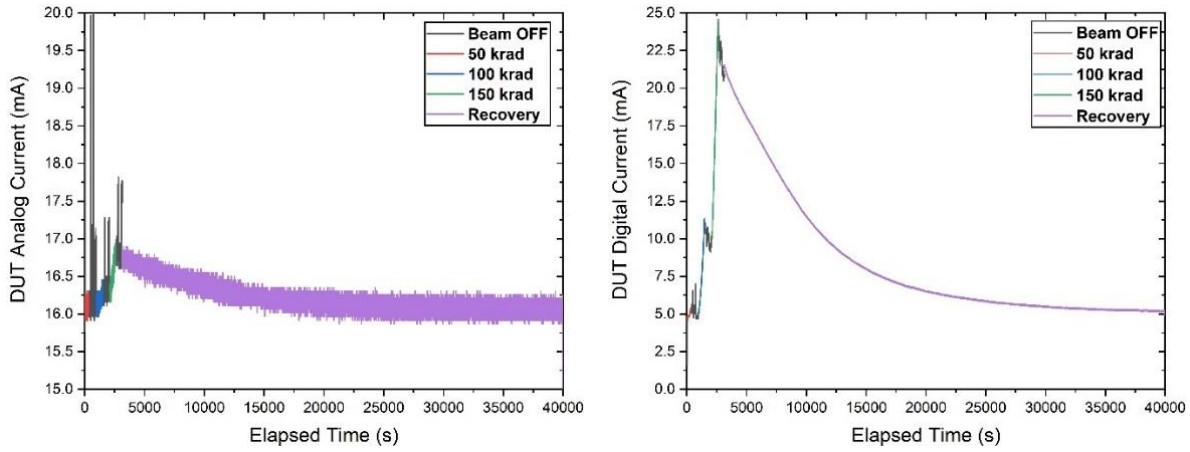

Fig. 3.12 *DUT power consumption on the analog block (left side) and digital block (right side) after three runs of 50 krad (Si) each, plus room-temperature recovery measurements*

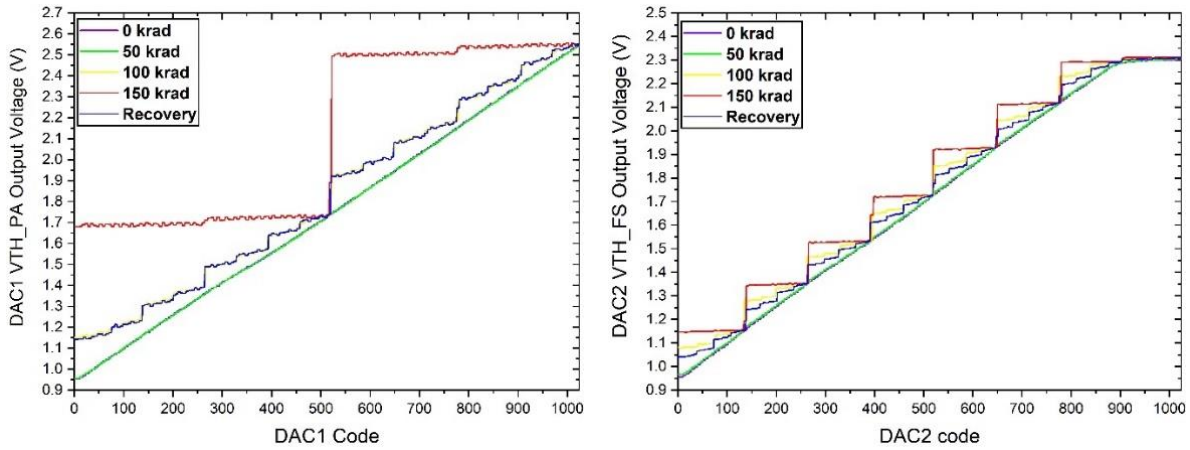

Fig. 3.32 *DUT DAC1 linearity (left side) and DAC2 linearity measurements after three runs of 50 krad (Si) and after recovery*

3.4 Conclusions

The SPACIROC ASIC will operate with very low error rates within the JEM-EUSO experiment over its full 5-years mission. Due to the very low dose rate expected ($\sim 2 \cdot 10^{-4}$ rad/s) any increase of the power consumption will be mitigated almost instantly through a rapid recovery process. However, in terms of SEE more tests are required in order to have a complete view of its reliability, as the maximum cosmic particle LET in space may reach a value of up to 40 MeV $\cdot$ cm^2/mg.

Chapter 4
Characterization of the KINTEX-7 FPGA Under Radiation Exposure

4.1 Device Under Test

The smallest device from Xilinx KINTEX-7 family, the XC7K70T circuit, was proposed as the main active component on the LHCb-RICH PDMDBs. The Xilinx 7-series family [20] is the first FPGA family manufactured by using the advanced TMSC's high performance and low power CMOS process that embeds a 28 nm high-k metal gate technology node.

To establish the reliability of KINTEX-7 FPGA in a radiation environment, a custom experimental setup was designed to ensure: power management, monitoring of various internal signal state as well as to control its functionality. Various firmware versions were proposed and designed to evaluate reliability of multiple general-purpose resources such as: FFs, CRAM, BRAM and I/O blocks, against SEE. Also, the susceptibility to radiation-induced SEL as well as to TID cumulative effects was measured.

4.2 Experimental Setup

The general layout of the experimental setup that was designed to test and evaluate the KINTEX-7 FPGA – named the DUT from now on within this chapter – is shown in fig. 4.2. It has four main components: the DUT test board, the power supply board, the DAQ system and the readout board. Several design procedures were followed in order to comply with the radiation testing constrains as well as to adapt easily for various irradiation environments and facilities, e.g. DUT placed either in vacuum chambers for irradiation with heavy ion beams or outside on a mechanical support with the proton-beam or X-ray beam extracted in air [21].

The DUT test board, was designed to be as simple as possible to ensure full functionality of the DUT but with minimum external components. No external memory to store the configuration bits was used. Therefore, the DUT was set to operate in JTAG mode and the only way to write/rewrite its configuration was through the JTAG port.

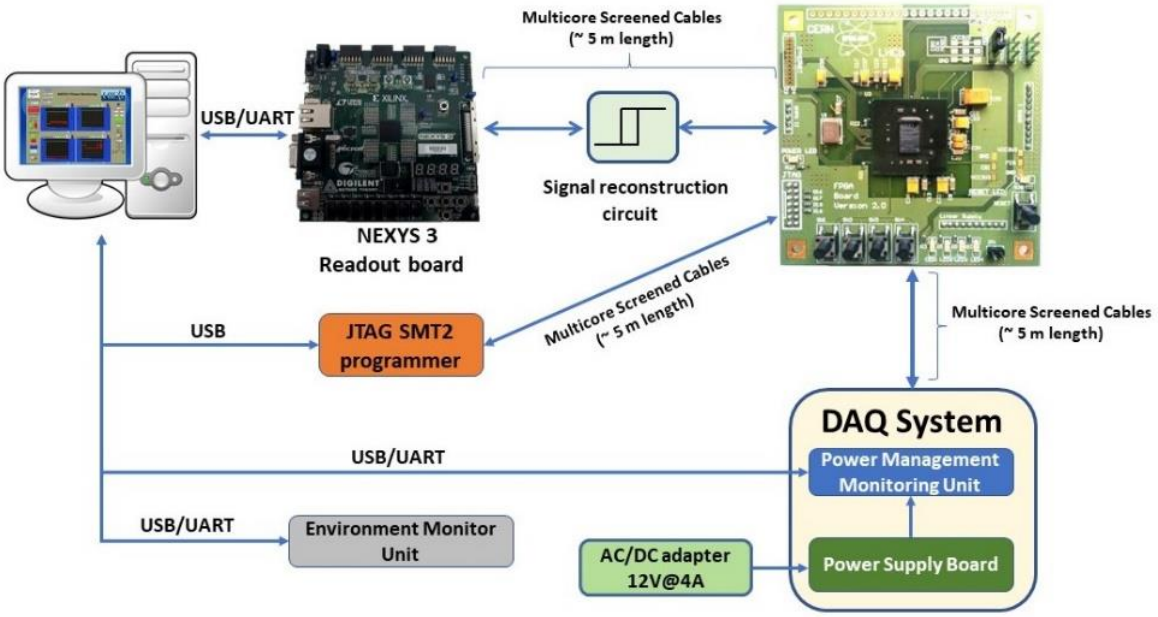

Fig. 4.2 *The general layout of the DUT experimental setup*

The power supply board was designed around ADP5050 [22] integrated circuit. This circuit is a dedicated solution to power complex integrated circuits such as FPGAs. It is a switching mode power supply controller and it has various features that were extended to the power supply board like: wide input voltage range (4.5 – 12 V), overheating and overcurrent protections, high efficiency and independent soft start and enable functions for each power supply channel. The power to the DUT was delivered via dedicated power connectors which were linked using multicore screened cables to the power supply board. To compensate for the voltage drops on the long cables, the power supply feedback connections on the most important power rails were moved at the end of the cables, near the DUT.

The power supply quality is a very important step to ensure the functionality of the DUT without errors or failures due to voltage drops. In this way, a custom electronic load was designed to test and stress the power supply board, respectively its power rails and to measure their output quality [23].

A custom DAQ system was designed to monitor four most important power rails (VCCINT, VCCAUX, VCCO and VCCIO) that are powering the DUT. The power monitoring was done with high-side current sense amplifiers, on which the current flow through a shunt resistor is converted into a voltage. The resulted voltage is filtered through a low-pass RC filter before is fed into the ADC block of an 8-bit microcontroller. The microcontroller acquires the data with a resolution of 1 mV and equivalent to 1 mA, respectively, and sends it, on user request, via an UART communication to a LabVIEW GUI

at every 50 ms. The LabVIEW GUI shown in fig. 4.5 is used to communicate to the DAQ system and to ensure the power management as well as power monitoring of the DUT. The user can perform power cycle of the DUT and to save the data in computer files for offline analysis. Several additional functions were implemented to facilitate the SEE-dedicated counting and identification of such events – e.g. SELs.

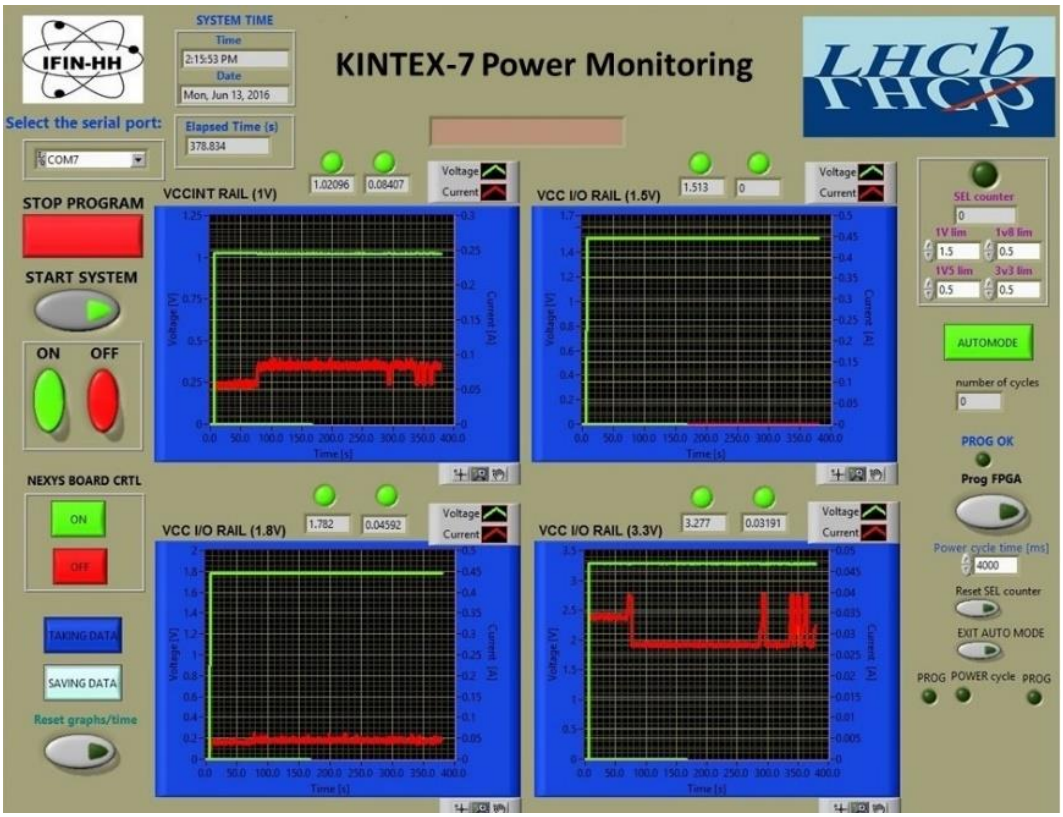

Fig. 4.5 *The LabVIEW GUI designed to power and monitor the DUT as well as to control the DAQ system*

4.3.2 Solutions to Test and Mitigate Errors for Dedicated Logic Resources

Several firmware versions were designed to test logic resources like the FFs, BRAM and the I/Os. For some of them the SEM core internal scrubber was used to ensure the error mitigation as well as to test the CRAM itself and to extract the SEU rates within the CRAM while the DUT was being irradiated.

The SEU rates within the user FFs were measured by using four firmware configurations with the FFs arranged in single chain and by using various TMR configurations.

A special attention was dedicated to test the I/O block reliability against radiation-induced SEUs. Here a custom firmware embedding 4 ring oscillator (RO) architectures was designed

within the I/O banks of the DUT. Such structure was designed by using only the I/O buffers primitives set as delay elements in which the signal is shifted through the I/O blocks chain. The output signal of the last I/O block is inverted by using a logic inverter gate and its output is connected to the first delay element. The architecture presented in fig. 4.14 meets the requirements to generate a full self-oscillation while using only one LUT to implement the logic inverter as additional logic resource.

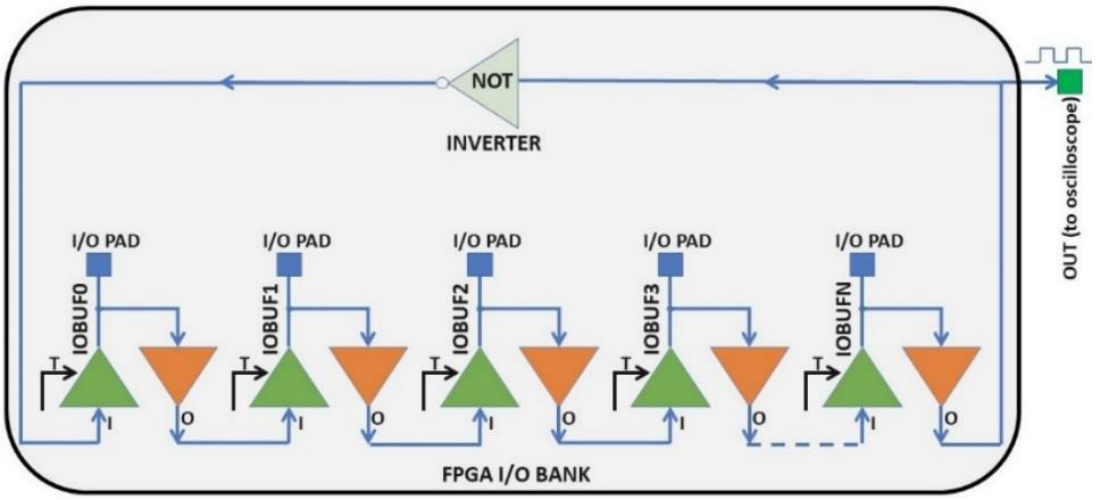

Fig. 4.14 *The single inverter ring oscillator architecture within the DUT I/O blocks -self citation [24]*

4.4 Test Beam Results and Analysis

The Kintex-7 FPGA was tested with various particle beams by using protons, ions, X-Rays and a mixed radiation field. The following facilities were used to establish the DUT reliability in a radiation environment:

- Ions at SIRAD facility [16] from Legnaro National Laboratories in Italy;
- Ions at Heavy Ion Facility (HIF) [25] from Université Catholique de Louvain in Belgium;
- 200 MeV protons at the proton irradiation facility (PIF) [17] from Paul Scherer Institute in Switzerland;
- 35 MeV protons from pre-accelerator of the 2.88 GeV Cooler Synchrotron COSY-Jülich [18] from Juelich Research Center in Germany;
- X-rays at the X-ray radiation facility [19] from Padova University in Italy.
- Mixed field of radiation at the CHARM facility [26] from CERN.

4.4.1 Ion Irradiation

Several measurements of the CRAM single-bit SEU were carried out by using ions with a broad range of LET between (1.3 +/ -0.26) MeV · cm^2/mg to (32.4 +/- 6.48) MeV · cm^2/mg. The threshold LET value was found to be below (1.3 +/ -0.26) MeV · cm^2/mg with a single-bit SEU cross-section value of (1.75 +/-0.18) · 10^{-4} cm^2/DUT. At the maximum LET of (32.4 +/- 6.48) MeV·cm^2/mg the single-bit SEU cross-section value was measured to be (170 +/- 26) · 10^{-4} cm^2/DUT.

Besides the CRAM integrity, a careful attention was given to the SEL detection within the DUT. The threshold LET for SEL was measured with ions to be at around (15.6 +/- 3.12) MeV · cm^2/mg which is confirmed by other independent measurements. Three SEL cross-section values were measured: (2.8 +/- 0.7) · 10^{-6} cm^2/DUT for an LET of (15.6 +/- 3.12) MeV · cm^2/mg, (28 +/- 8.8) · 10^{-6} cm^2/device for an LET of 20.4 MeV · cm^2/mg and (78 +/- 18) · 10^{-6} cm^2/DUT for an LET of 32.4 MeV · cm^2/mg [27]. A sample of an ion-induced SEL set can be observed in the right side of fig. 4.22. The SELs were mitigated by power cycles of the DUT and no permanent effects were observed.

The I/O blocks resilience against radiation was tested by using RO structures. Even though the overall usage of CRAM bits was very low with only 0.19 % ratio of essential bits, several types of failures within the RO structure were observed and most notable were the complete loss of oscillation where at least one I/O block is affected by SEU. The complete loss of oscillation failure probability cross-sections were found to be respectively $0.6^{+1.15}_{-0.47}$ ·10^{-5} cm^2/DUT for an LET of (13.35 +/- 1.36) MeV·cm^2/mg [28].

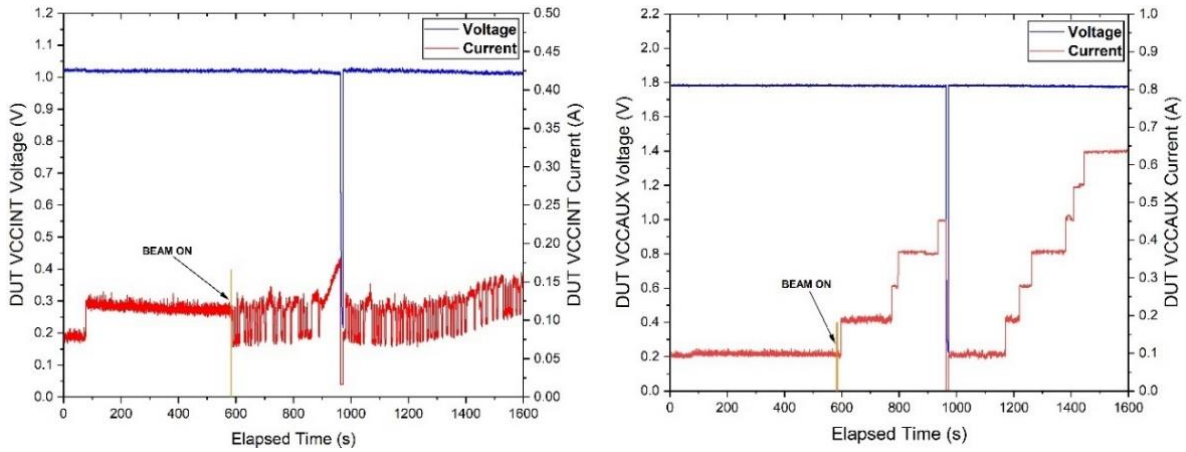

Fig. 4.22 *The evolution of the VCCINT (left side) and VCCAUX (right side) power consumption while the DUT was irradiated during the 5th irradiation run*

4.4.2 Proton Irradiation

With protons, the average CRAM single-bit SEU cross-section was measured to be (15.82 +/- 0.96) · 10^{-8} cm^2/DUT for 35 MeV protons, and (7.6 +/- 1.6) · 10^{-8} cm^2/DUT for 200 MeV protons. Both measurements are in agreement with other independent measurements provided by the literature.

The error rates within the FFs were measured by using different firmware configurations. Several FF chain architectures that include various TMR designs were tested with 35 MeV protons and most significant improvement was observed for the basic TMR design with respect to single chain of FFs. The cross-section value of (8.62 +/ -0.06) · 10^{-17} cm^2/FF obtained with the basic TMR architecture shows a good improvement of masking the SEUs within the FFs with respect to the (1.65 +/ -0.01) · 10^{-16} cm^2/FF value obtained for a single chain of FFs.

The cross-section value for the I/O blocks failures was measured to be $2.22^{+1.4}_{-1}$ · 10^{-11} cm^2/DUT for 35 MeV proton beam [24]. No proton-induced SELs were observed during the irradiation.

4.5 Conclusions

The KINTEX-7 has an excellent resilience against TID effects at least up to about 1 Mrad (Si) and for small TID rates < 100 krads/h – these testing TID rates are much higher than experiment TID rates, though. The main concern remains the integrity of the CRAM, as its SRAM-based structure is very sensible to SEUs. Large SEU numbers within the CRAM lead to the activation of the parasitic circuits within the DUT that contributed to increase within the power consumption, mostly visible on the VCCINT and VCCAUX power rails. These effects were mitigated with a full reconfiguration of the DUT done with a hybrid scrubbing procedure.

Ensuring a fast SEU mitigation in CRAM shall be the main concern when proposing such device to be used in a radiation environment similar with the one expected at LHCb-RICH, or in other equivalent radiation environments, with thousands of such circuits operating simultaneously in the experiment systems.

Chapter 5
Characterization of the Axcelerator FPGA Under Radiation Exposure

The Axcelerator FPGA family from Microsemi (now Microchip) are antifuse FPGAs designed with the advanced 0.15 µm CMOS antifuse process [29] to be used in safety-critical applications. Due their antifuse technology that makes them a good candidate to be used in radiation environments, this family was proposed as a backup solution for the KINTEX-7 FPGA within the LHCb-RICH application at CERN. Therefore, the AX250-FG484 FPGA was evaluated in a radiation environment, too.

5.1 Experimental Setup

To test the reliability of the AX250 device – from now on referred as DUT – under ionizing radiation, a custom experimental setup was designed to power, monitor and control the DUT all times – that is before, during and after the irradiation tests.

The experimental setup architecture is given in fig. 5.1, and is mainly composed of: a custom DUT test board and an FPGA-based DAQ system. The DAQ system is used to ensure the power management of the DUT as well as to control and to read out the DUT logic circuitry. The connections between each component are made with screened cables of at least 5 meters length and, for the high-speed data and clock signals a HDMI cable was used to ensure a proper signal integrity. Plugin adapters were designed to facilitate remote communication and control of the DUT via the DAQ system and to allow testing the DUT I/O pins.

The experimental setup has the following features that were implemented either on hardware or software level:

- Power monitoring on up to 8 power rails with a resolution of 62.5 µV and 62.5 µA;
- SELs or high current states detection, marked by current increasings within the DUT power rails; (individual for each power rail)
- Power cycle and power-up sequencing;
- High-speed readout through custom communication boards; (1 – 10 MHz)

- Dedicated software routines to detect and measure the radiation-induced SEUs within the DUT logic;
- Temperature monitoring of DUT package and the environment by using 2 PT1000 temperature sensors.

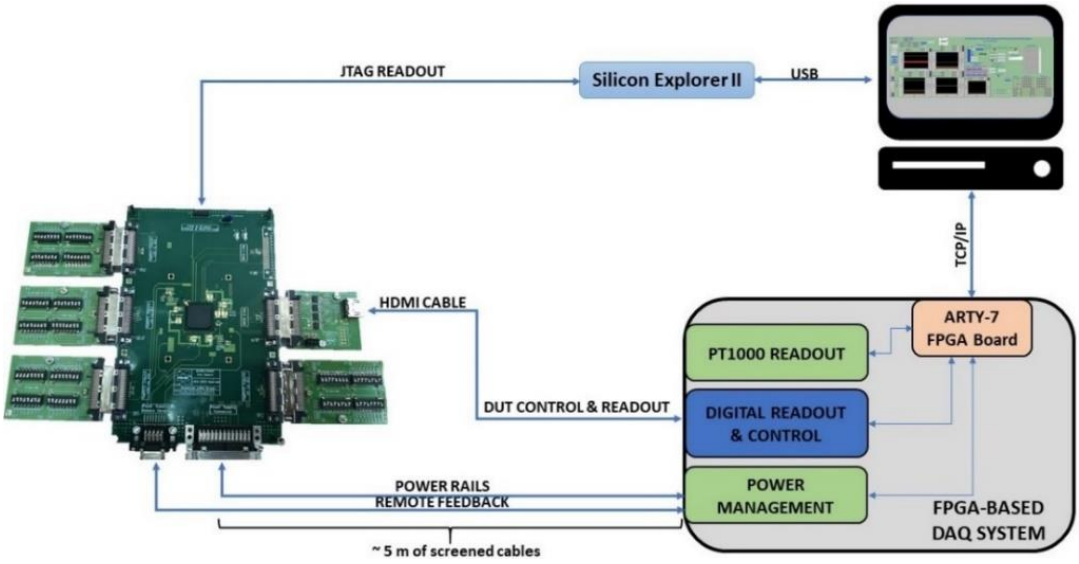

Fig. 5.1 *Experimental setup architecture proposed for monitoring and control of the DUT*

The DUT test board, was designed on a 8-layer PCB around the AX250-FGG484 device, ensuring an operation with close to full FPGA functionality and with a minimum number of components on the board.

The DAQ system, is a key component of the experimental setup due to its role of controlling and monitoring the DUT activity. It includes 2 parts: a commercial FPGA development board, and a custom acquisition and control board. The acquisition and control board, which can be seen in fig. 5.4, was designed on a 6-layer PCB with all the features needed to control and read out the DUT as well as to ensure the power management.

The DUT is powered through 7 independent power rails over at least 5 meters of multi-core screened cable. The power supply is designed around 2 integrated circuits with 4 buck regulators each, the ADP5050 device [22]. The design takes into account the fact that the DUT has to be powered over a long cable. To mitigate the voltage drops on the cables as well as to secure a good transient response and the stability of each power rail, a remote feedback technique was implemented. This technique was implemented with unity gain differential amplifiers that were used to measure the voltage across each power rail supplying the DUT. In this way, the amplifier outputs the voltage to the ADP5050 feedback network, allowing the controller to adjust the voltage and stabilize it to a desired value, thus the voltage drops on the

cables are cancelled. To test the reliability of each power rail and to simulate various radiation-induced scenarios, a custom electronic load was designed and used for this purpose [30].

A complex GUI was designed by using the LabVIEW software to control the DAQ system and respectively to read out the DUT data and its electrical parameters using either an UART or TCP/IP interface. It was designed using a finite state machine architecture that allows fast control and high acquisition rates. The GUI front panel is shown in fig. 5.7.

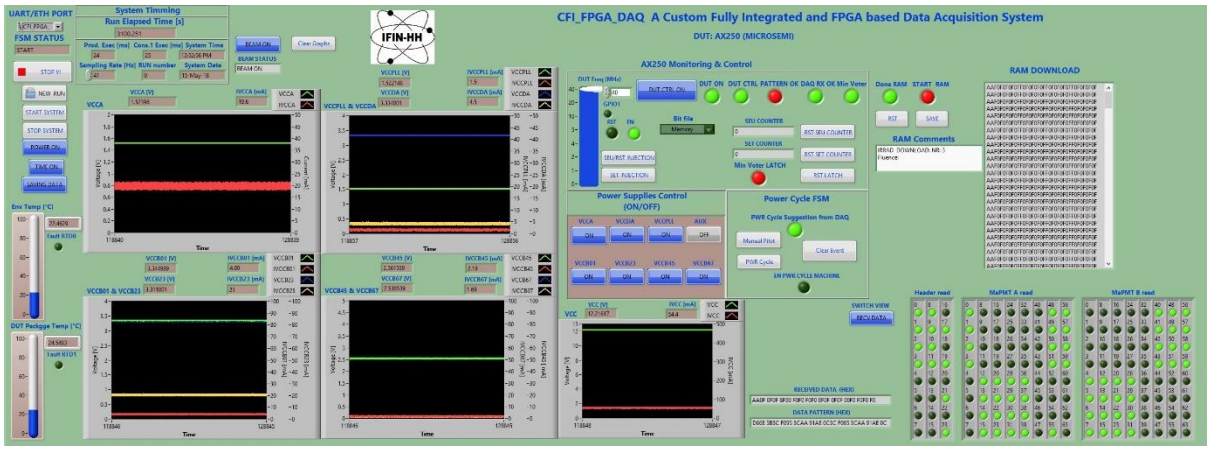

Fig. 5.2 *The LabVIEW-based GUI designed to communicate with the DAQ system*

5.3.1 Proton Irradiation

The SIRAD facility provided 24 MeV protons beam with flux values between 10^8 and 10^9 protons/cm^2/s and the DUT was exposed to a fluence of about (2.5 +/- 0.5) · 10^{13} protons/cm^2.

During the proton irradiation, 3 failures were observed: one logical error that was only recovered by a hardware reset (power cycle), and 2 SEUs within the data frame coming from the DUT. Therefore, by summing up these errors a value of $3^{+3.4}_{-1.4}$ for a 95 % CL is obtained, and the upper limit of logic error cross-section was calculated to be (2.56 +/- 0.51) · 10^{-13} cm^2/DUT for a fluence of (2.5 +/-0.5) · 10^{13} protons/cm^2. This cross-section corresponds to extreme circumstances of a high dose rate (1 krad/s), hence it should be counted more as an upper limit on SEU rate than as an actual measurement of the SEU cross-section.

In terms of TID, the DUT withstood - with no operational failures - up to a dose of (8 + 2) Mrad, that with high dose rates of (1248 +/- 312) rad/s. High TID-induced increase of the global power consumption was observed, more visible within its core power rail, after a TID

of (320 +/- 64) krad (Si). This effect was proven to be restricted to experiments with high TID rates comparable or within few orders magnitude to 1krad/s. A sample of evolution of the DUT core power consumption, as well its package temperature during a run with the DUT irradiated up to (3.2 +/- 0.64) Mrad can be seen in fig. 5.14.

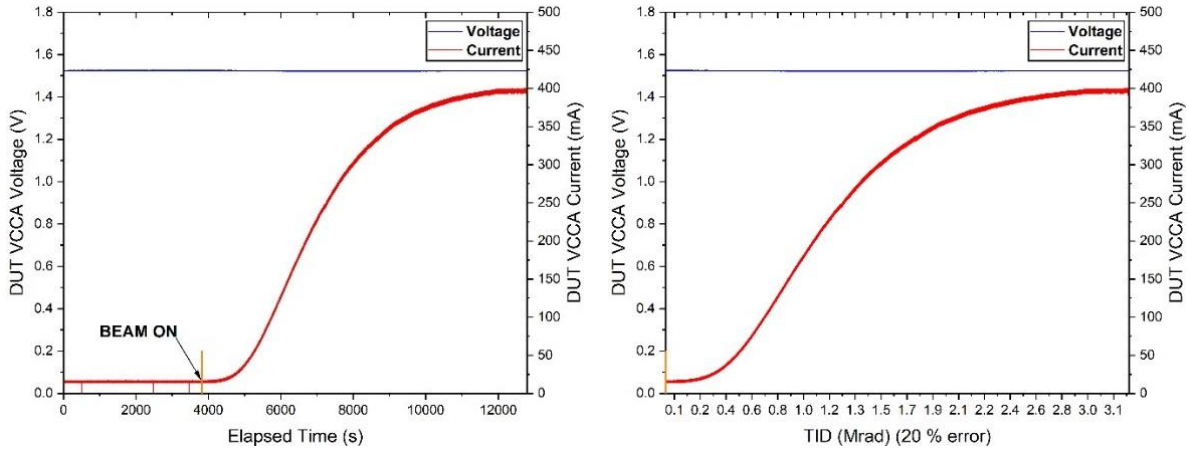

Fig. 5.3 *The evolution of DUT core current as a function of time (left side) and TID (right side) during a run of (3.2 +/- 0.64) Mrad (Si) done with a dose rate of (363 +/- 73) rad/s s, no such effects are expected in LHCb environment with 10^4 times less dose rate value*

Several measurements of SEU rates within the embedded RAM resources were carried out with ((24 +/- 0.5) – 3.7) MeV protons beam. The average value of SEU cross-section was measured to be (3.57 +/- 0.18) · 10^{-14} cm^2/bit.

5.5 Conclusions

The AX250 FPGA is an excellent alternative to be used in applications operating in radiation environment, as a very low number of radiation-induced failures was measured during the proton test beam. However, a few tradeoffs have to be taken into account regarding this FPGA when designing an application, such as: one-time programmability, logic resource density is lower compared with latest generation FPGAs, its power consumption is higher due to its older technology and additional circuitry may be needed when interfacing with very low voltage peripherals.

Chapter 6
Conclusions and Original Contributions

Within this PhD thesis, the reliability of 3 complex integrated circuits, one ASIC and two FPGA technologies, was investigated in several radiation environments. The measured experimental data was extrapolated to their target applications.

6.1 Summary of Results

6.2 Original Contributions

I am employed since August 2014 by Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering (IFIN-HH) and since then I am an Associate Electronics Engineer and PhD student (with LHCb author rights due to specific contribution) to the LHCb collaboration at CERN respectively in the Romanian LHCb group. From the beginning I was directly involved in activities related to the upgrade program of the LHCb-RICH sub-detectors. During my PhD thesis I participated at various R&D activities focused on the development of hardware and software/firmware solutions related to the LHCb-RICH PDMDBs as well as to design test prototype systems to carry out quality assurance tests on the PDMDBs and their plugin modules.

Within the Romanian LHCb Group, besides the LHCb related activities, I was involved in various capacities in irradiation tests done for various integrated circuits, which were proposed to operate in radiation environments. Part of original contributions are repeated at each tested integrated circuit and consequently they are grouped into "General original contributions". Then, specific original contributions for each tested integrated circuit are presented.

General original contributions

- Major contributions into establishing the irradiation testing strategy for each tested integrated circuit (e.g. irradiation setup proposal, irradiation strategy etc.);
- For each tested integrated circuit, a compressive irradiation setup was designed and implemented following strict rules in terms of radiation and facility constrains;
- Each irradiation setup was connected to dedicated LabVIEW GUIs; these GUIs were developed in this PhD thesis for each irradiation setup, allowing close monitoring and full control of the circuit under test as well as data saving for later analysis;
- Each irradiation setup, had a DAQ system that was controlled by either a micro-controller or an FPGA, hence besides the hardware design of each DAQ system, I wrote the firmware for each of them either in C or VHDL language;
- One key component within the irradiation setups was the power supply boards, which had to be tested in advance by simulating radiation-induced high current states. Therefore, custom active electronic loads were designed to establish the reliability of the power supplies before they were used in the irradiation tests; [A5, C4]
- Important contributions into proposing several testing methodologies to detect and measure various radiation-induced effects within the tested integrated circuits, and which were largely described in this PhD thesis; (e.g. latch-up detection, SEU detection and mitigation in all three circuits)
- Several contributions were brought to mitigate or to reduce the impact of radiation-induced effects within the tested integrated circuits; (e.g. the hybrid scrubber architecture to detect and correct SEUs within the CRAM for the KINTEX-7 FPGA and presented in section 4.3.1)
- Multiple software scripts were designed, mainly by using Python language and LabVIEW, to analyze the post irradiation data and to extract the cross-section values for different experiments in order to explain the circuits behavior in a particular radiation environment.

Beside these, a lot of work was carried out at the irradiation facilities in terms of irradiation setup arrangement as well as data taking and full supervision of the circuit under test.

Original contributions within the SPACIROC2 ASIC evaluation:

- The symmetrical power supply board, the DAQ system and its associated LabVIEW GUI were designed in order to ensure individual power monitoring of the ASIC on both analog and digital cores as well as to monitor various internal signals; [A4]
- The DAQ system was configured to cope with the monitoring requirements via its LabVIEW GUI and the latter to save the data in computer files for later analysis;
- Full software integration was ensured in order to be able to communicate with the ASIC registers via the DAQ system to detect and correct the radiation-induced SEUs;
- After each irradiation, laborious data analysis was carried out based on the measured data, and the circuit behavior under ionizing irradiation was established and presented in section 4.4.

Original contributions within the KINTEX-7 FPGA evaluation:

- Several contributions were brought to the hardware part of the irradiation setup containing the FPGA test board, the power supply board and its associated DAQ system; [C3]
- The FPGA test board was designed in accordance with various radiation constrains with the FPGA as the only active component on the board, and in the same time it ensured a full functionality with minimum components;
- Several FPGA firmware architectures were proposed to test and mitigate radiation-induced failures within several critical resources of the KINTEX-7 FPGA under radiation exposure and the VHDL code for few of them can be seen in annex A1-A4; [C1]
- A complex power management and DAQ architecture dedicated for the LHCb-PDMDBs that embeds the KINTEX-7 FPGAs was proposed when these PDMDBs were irradiated in the mixed field of radiation at the CHARM facility from CERN. The FPGAs were powered and monitored over about 50 meters of cables, by this custom DAQ system. Four independent DAQ systems were tied to the same LabVIEW GUIs in order to allow remote controlling and monitoring of the FPGA (details in section 4.4.4);
- Laborious data analysis was carried after each irradiation test beam in order to extract the error rates and to conclude the FPGA behavior under ionizing radiation exposure. (details in section 4.4)
- Several irradiation results were published and presented at various international conferences. [A1-A2, C1-C2]

Original contributions specific to the Axcelerator FPGA evaluation:

- The monitoring and testing strategy of the Axcelerator FPGA under radiation exposure was proposed;
- A new and more complex irradiation setup was designed (hardware and software contributions);
- Multiple boards were designed using Altium Designer that were required to ensure the functionality of the irradiation setup: FPGA test board, FPGA DAQ board, the communication plugin boards and the I/O plugin boards; (for schematic diagrams see annex A5-A7)
- Every board that was part of the irradiation setup was assembled completely manually as follows: 9 FPGA test boards, 3 DAQ boards, 5 communication boards and 12 I/O plugin boards;
- Several firmware architectures were proposed to test and mitigate radiation-induced failures within several critical resources of the Axcelerator FPGA and their VHDL code can be seen in annex A8-A10;
- Due to the fact that the antifuse FPGAs are one-time programmable, careful simulation and testing of the firmware architectures on other FPGA platforms was carried out before programming the antifuse device;
- Compressive data analysis was performed based on the measured data during irradiation and the FPGA behavior under a specific source of radiation was extracted and presented in section 5.3.

To summarize, over 10 articles and conference proceedings related to this PhD thesis were published. More than 20 presentations were held at various international conferences and workshops, including as well as within the LHCb collaboration general meetings. The complete list of communications and papers can be found in section 6.3.

A much more completed and upgraded version of the irradiation setup presented in section 5.1, is proposed to be patented. This new system is a scalable and dedicated system designed to carry out full monitoring and control of various integrated circuits when are exposed to ionizing radiation.

6.3 List of Papers and Conference Participations

6.3.1 Published Papers Related to this PhD Thesis Topic

A. Published papers in ISI indexed journals with UPB affiliation

A1. V. M. Placinta, L. N. Cojocariu, and C. Ravariu, *Proton-induced radiation effects in the I/O blocks of an SRAM-based FPGA*, **Journal of Instrumentation**, vol. 14, no. 10, pp. T10001–T10001, Oct. 2019, WOS:000501798500001, IF = 1.452 (2019), Q3, ISSN: 1748-0221, doi: 10.1088/1748-0221/14/10/T10001.

A2. L. N. Cojocariu and **V. M. Placinta**, *Ion Beam Irradiation Effects in KINTEX-7 FPGA Resources*, **Romanian Journal of Physics**, vol. 61, no. 901, p. 10, IF = 1.197 (2018), Q3, ISSN: 1221-146X.

A3. M. K. Baszczyk,…,**V. M. Placinta**,…. et al., *Test of the photon detection system for the LHCb RICH Upgrade in a charged particle beam*, **Journal of Instrumentation,** vol. 12, no. 01, pp. P01012–P01012, Jan. 2017, WOS:000395769600012, IF 1.220 (2016), Q3, ISSN: 1748-0221, doi: 10.1088/1748-0221/12/01/P01012. (6 citations)

A4. V. M. Placinta, L. N. Cojocariu, and C. Ravariu, *Test Bench Design for Radiation Tolerance of Two ASICs*, **Romanian Journal of Physics**, vol. 62, no. 903, p. 12, 2017, WOS:00040577260012, IF = 1.758 (2016), Q2, ISSN: 1221-146X. (4 citations)

A.5. V.-M. Placinta, F. Babarada, C. Ravariu, and L. G. Alecu, *Digitally Controlled Electronic Load for Testing Power Supplies Reliability*, **Rev. Roum. Sci. Techn.–Électrotechn. et Énerg**, vol. 64, no. 2, pp. 131–136, 2019, IF = 0.76 (2019), Q4.

A6. C. Ravariu, D. E. Mihaiescu, A. Morosan and **V. M. Placinta**, *New steps for advancing the Nothing On Insulator Triode 3nm gap and preliminary expanded technology*, **Romanian Journal of Information Science and Technology**, vol. 23, no. 2, p. 13, 2020, WOS:000532321500002.

In the next papers (section B), a selection of 12 papers are given with the author names in alphabetical order. Given my status as a PhD student and with my thesis topic related to the LHCb upgrade program, I have been included in the LHCb collaboration author list, which gave me the opportunity to be co-author on more than 170 high-impact papers related to the LHCb physics program.

B. Published papers in ISI journals related to the LHCb collaboration with IFIN-HH affiliation

B1. R. Aaij, C. A. Beteta, T. Ackernley,…, **V. Placinta**, et al., *First Observation of Excited Ω_b^- States*, **Physics Review Letters**, 124, 082002, February 2020, IF = 8.385 (2019), Q1, doi: 10.1103/PhysRevLett.124.082002

B2. R. Aaij, C. A. Beteta, T. Ackernley,…, **V. Placinta**, et al., *Measurement of the B_c^- meson production fraction and asymmetry in 7 and 13 TeV pp collisions*, **Physical Review D**, 100, 112006, December 2019, IF = 4.833 (2019), Q1, doi: 10.1103/PhysRevD.100.112006

B3. R. Aaij, C. A. Beteta, T. Ackernley,…, **V. Placinta**, et al., *Measurement of Charged Hadron Production in Z-Tagged Jets in Proton-Proton Collisions at $\sqrt{s}$ = 8 TeV*, **Physics Review Letters**, 123, 232001, December 2019, IF = 8.385 (2019), Q1, doi: 10.1103/PhysRevLett.123.232001

B4. R. Aaij, C. A. Beteta, T. Ackernley,…, **V. Placinta**, et al., *Observation of CP Violation in Charm Decays*, **Physics Review Letters**, 122, 211803, 2019, IF = 8.385 (2019), Q1, doi: 10.1103/PhysRevLett.122.211803

B5. R. Aaij, C. A. Beteta, M. Adinolfi,…, **V. Placinta**, et al., *Search for beautiful tetraquarks in the $\Upsilon(1S)\mu^+\mu^-$ invariant-mass spectrum*, **Journal of High Energy Physics**, 86, 2018, WOS:000447516300002, IF = 5.833 (2018), Q1, ISSN: 1029-8479, doi: 10.1007/JHEP10(2018)086

B6. R. Aaij, C. A. Beteta, M. Adinolfi,…, **V. Placinta**, et al., *Search for lepton-flavour-violating decays of Higgs-like bosons*, **European Physical Journal C**, 78, 12, December 2018, WOS:000453066200003, IF = 4.843 (2018), Q1, ISSN: 1434-6044, doi: 10.1140/epjc/s10052-018-6386-8

B7. R. Aaij, C. A. Beteta, M. Adinolfi,…, **V. Placinta**, et al., *Measurement of Antiproton Production in p-He Collisions at root S-NN=110 GeV*, **Physics Review Letters**, 121, 22, November 2018, WOS:000451582500005, IF = 8.385 (2018), Q1, ISSN: 0031-9007, doi: 10.1103/PhysRevLett.121.222001

B8. R. Aaij, C. A. Beteta, T. Ackernley,…, **V. Placinta**, et al., *Search for weakly decaying b-flavored pentaquarks*, **Physical Review D**, 97, 3, 032010, February 2018, WOS:000425304300001, IF = 4.368 (2018), Q1, ISSN: 2470-0010, doi: 10.1103/PhysRevD.97.032010

B9. R. Aaij, C. A. Beteta, T. Ackernley,…, **V. Placinta**, et al., *Search for Dark Photons Produced in 13 TeV pp Collisions*, **Physics Review Letters**, 120, 6, 061801, February 2020, WOS:000424507800010, IF = 9.227 (2018), Q1, ISSN: 0031-9007, doi: 10.1103/PhysRevLett.120.061801

B10. R. Aaij, B. Adeva, M. Adinolfi, **....,V. Placinta**, et al., *Bose-Einstein correlations of same-sign charged pions in the forward region in pp collisions at root s=7 TeV*, **Journal of High Energy Physics**, 12, 025, December 2017, WOS:000417757900003, IF = 5.541 (2017), Q1, ISSN: 1029-8479, doi: 10.1007/Jhep12(2017)025.

B11. R. Aaij, B. Adeva, M. Adinolfi,…, **V. Placinta**, et al., *Search for lepton-flavour-violating decays of Higgs-like bosons*, **European Physical Journal C**, 77, 12, 812, November 2017, WOS:000417101000002, IF = 5.172 (2017), Q1, ISSN: 1434-6044, doi: 10.1140/epjc/s10052-017-5178-x

B12. R. Aaij, B. Adeva, M. Adinolfi, **....,V. Placinta**, et al., *Measurement of the J/psi pair production cross-section in pp collisions at root s = 13 TeV*, **Journal of High Energy Physics**, 10, 068, October 2017, WOS:000412907800015, IF = 5.541 (2017), Q1, ISSN: 1029-8479, doi: 10.1007/Jhep10(2017)068.

C. Published papers in conference proceedings indexed in ISI or IEEE with UPB affiliation

C1. V.-M. Placinta and L. N. Cojocariu, *Radiation Hardness Studies and Evaluation of SRAM-Based FPGAs for High Energy Physics Experiments*, **in Proceedings of Topical Workshop on Electronics for Particle Physics - PoS(TWEPP-17)**, Santa Cruz, California, Mar. 2018, p. 085, doi: 10.22323/1.313.0085.

C2. V. M. Placinta, L. N. Cojocariu, and C. Ravariu, *I/O Blocks Reliability for an SRAM-Based FPGA When Exposed to Ionizing Radiation*, **in Proceedings of 2018 International Semiconductor Conference (CAS)**, Sinaia Romania, Oct. 2018, WOS:000514386700038, ISBN: 978-1-5386-4482-9, doi: 10.1109/SMICND.2018.8539743

C3. L. N. Cojocariu, **V. M. Placinta**, and L. Dumitru, *Monitoring system for testing the radiation hardness of a KINTEX-7 FPGA*, **in Proceedings of 9TH INTERNATIONAL PHYSICS CONFERENCE OF THE BALKAN PHYSICAL UNION (BPU-9)**, Istanbul, Turkey, 2016, p. 140009, doi: 10.1063/1.4944199.

C4. V. M. Placinta, L. N. Cojocariu, and C. Ravariu, *Evaluating the switching mode power supplies used in radiation hardness tests of integrated circuits*, **in Proceedings of 2017 International Semiconductor Conference (CAS)**, Sinaia, Oct. 2017, pp. 305–308, WOS:000425844500068, ISBN: 978-1-5090-3985-2, doi: 10.1109/SMICND.2017.8101232.

C5. M. Serbanescu, **V. M. Placinta**, O. E. Hutanu, and C. Ravariu, *Smart, low power, wearable multi-sensor data acquisition system for environmental monitoring*, **in Proceedings of 2017 10th International Symposium on Advanced Topics in Electrical Engineering (ATEE)**, Bucharest, Romania, 2017, pp. 118–123, WOS:000403399400024, ISBN: 978-1-50-0-5160-1, doi: 10.1109/ATEE.2017.7905059.

C6. C. Ravariu, C. Parvulescu, and **V. M. Placinta**, *Technology and Optimizations for the NOI-Nano-Triode*, **in Proceedings of 2019 International Semiconductor Conference (CAS)**, Sinaia, Romania, Oct. 2019, pp. 75–78, WOS:000514295300014, ISBN:978-1-7281-1888-8, doi: 10.1109/SMICND.2019.8923917.

List of scientific research reports during the PhD program:

1. **Introduction Nuclear Engineering and the R&D within CERN High Energy Experiments**
2. **Radiation-Induced Failure within the Semiconductor Electronics Devices**
3. **Test Bench Design for Radiation Tolerance of Two ASICs**
4. **Radiation Hardness Studies and Evaluation of SRAM-Based FPGAs for High Energy Physics Experiments**
5. **Data Analysis and Investigation of Proton Induced Radiation Effects in 0.15 µm CMOS Antifuse FPGA**

Without the financial support from Romanian funding agencies supporting the materials and expenses of this work I would not been able to complete these studies and popularize the results and gain the necessary experience. Hence, I am grateful to Ministry of National Education and Research and Institute of Atomic Physics (IFA) for providing the funding under the following grants:

- IDEI PN-II-ID-PCE-2011-3-0749 (2012 - 2016);
- contract/project IFA "Capacitati" LHCb 3/3.12.2012 (2012 - 2015);

- IFA projects and contracts PN-III 5.2 Romania-CERN LHCb 7/16.03.2016 (2016 - 2019) and LHCb 9/16.03.2020 (2020 - 2021);
- PN-III-P4-IDPCE-2016-0480 (2017 - 2019);
- national project "Nucleu" PN 19 06 01 04 (2019 - 2021), as well as other institutional IFIN-HH projects.

6.3.2 Presentations Held at International Conferences, Workshops, Symposiums and within the LHCb Collaboration at CERN

1. **V. M. Placinta**, L. N. Cojocariu and Florin Maciuc, *Radiation Hardness Tests Done on KINTEX-7 FPGA for High Energy Physics Experiments*, **Topical Workshop on Electronics for Particle Physics 2019**, University of Santiago de Compostela, Santiago de Compostela, Spain, September 2^{nd} – 6^{th} 2019, available at: TWEPP 2019 (poster)
2. **V. M. Placinta**, L. N. Cojocariu and Florin Maciuc, *Radiation Hardness Tests Done on KINTEX-7 FPGA for High Energy Physics Experiments*, **19th International Balkan Workshop on Applied Physics and Materials Science (IBWAP 2019)**, University of Santiago de Compostela, Ovidius University of Constanta, Constanta, Romania, July 16^{th} – 19^{th} 2019. available at: link (poster)
3. **V. M. Placinta**, L. N. Cojocariu and Florin Maciuc, *Investigation of Proton-Induced Radiation Effects in 0.15 µm Antifuse FPGA*, **Topical Workshop on Electronics for Particle Physics 2018**, KU Leuven, Antwerp, Belgium, September 17^{th} – 24^{th} 2018, available at: TWEPP 2018 (presentation)
4. **V. M. Placinta**, L. N. Cojocariu, *Radiation Hardness of Field Programmable Gate Arrays in LHC Experiments*, **SAD -ETTI symposium,** Bucharest, Romania, July 2018 (presentation + poster)
5. **V. M. Placinta**, L. N. Cojocariu, *Radiation Hardness of Field Programmable Gate Arrays in LHC Experiments*, **Third Barcelona Techno Week – Course on semiconductor detectors**, Barcelona, Spain, July 2017 (poster)
6. **V. M. Placinta** and L. N. Cojocariu, *Radiation Hardness Studies and Evaluation of SRAM-Based FPGAs for High Energy Physics Experiments*, **Topical Workshop on Electronics for Particle Physics 2017**, Santa Cruz Institute of Particle Physics (SCIPP), California, USA, September 11^{th} – 14^{th} 2017, available at: TWEPP 2017

(presentation + conference proceeding)

7. **V. M. Placinta**, *First Results on KINTEX-7 FPGA testing in mixed field radiation at CHARM facility*, **Topical Workshop on Electronics for Particle Physics 2017**, Santa Cruz Institute of Particle Physics (SCIPP), California, USA, September 11th – 14th 2017, available at: TWEPP 2017 (presentation)
8. **V. M. Placinta** and L. N. Cojocariu, *Test Bench Design for Evaluating the Performance of Multi-anode Photomultiplier Tubes*, **17th International Balkan Workshop on Applied Physics and Material Science**, Ovidius University of Constanta, Constanta, Romania, July 11th – 14th 2017. (presentation)
9. **V. M. Placinta** and L. N. Cojocariu, *Test Bench for ASIC radiation hardness evaluation*, **Workshop on Sensors and High Energy Physics (SHEP 2016)**, Stefan Cel Mare University of Suceava, Suceava, Romania, October 21st – 22nd 2016, available at: SHEP 2016 (presentation)
10. **V. M. Placinta,** L. N. Cojocariu, et al, *Kintex-7 Irradiation, Test Bench and Results*, **Topical Workshop on Electronics for Particle Physics 2016**, Karlsruhe Institute of Technology (KIT), Karlshure, Germany, September 26th – 30th 2016, available at: TWEPP 2016 (presentation)
11. **Vlad-Mihai Placinta** and Stephen Wotton, *PT1000 Temperature Readings Through GBT-SCA ADC Lines*, **General RICH Meeting**, 12th of November 2019, available at: link (private communication)
12. **Vlad-Mihai Placinta** and Stephen Wotton, *Update on SCA-ADC Temperature Readings and Calibration*, **RICH Upgrade – Integration and Commissioning**, 1st of November 2019, available at: link (private communication)
13. **Vlad-Mihai Placinta** and Stephen Wotton, *Update on SCA-ADC Temperature Calibration*, **RICH Upgrade – Integration and Commissioning**, 25th of October 2019, available at: link (private communication)
14. **Vlad-Mihai Placinta**, Floris Keizer and Stephen Wotton, *Temperature Reading through GBT-SCA ADC lines*, **RICH ECS meeting**, 10th of October 2019, available at: link (private communication)
15. **Vlad-Mihai PLACINTA**, *Summary of the PDMDB module testing*, **RICH upgrade PDMDB testing progress meeting**, 15th of March 2019, available at: link (private communication)

16. **Vlad-Mihai PLACINTA**, *Summary of Modules testing*, **RICH upgrade PDMDB testing progress meeting**, 7th of March 2019, available at: link (private communication)
17. **Vlad-Mihai PLACINTA**, *Antifuse FPGA Irradiation Setup*, **LHCb RICH Upgrade meeting**, 5th of June 2018, available at: link (private communication)
18. **Vlad-Mihai PLACINTA**, *Antifuse FPGA Irradiation Campaign Status*, **LHCb RICH Upgrade meeting**, 26th of February 2018, available at: link (private communication)
19. **Vlad-Mihai PLACINTA**, *Updates regarding the DAQ system proposed for PDMDB monitoring*, **LHCb RICH Upgrade mini-meeting**, 12th of April 2017, available at: link (private communication)
20. **Vlad-Mihai PLACINTA**, *First measurements of the I/O signals in KINTEX-7 FPGA in proton beam*, **Mini-meeting on irradiation for RICH Upgrade**, 24th of November 2017, available at: link (private communication)

6.3.4 Participation at International Schools and Courses

- *GRIDS 2019 – Graduate Instrumentation and Detector School*, organized by **TRIUMF facility within University of British Columbia**, June 10th – 21th 2019, Vancouver British Columbia, Canada. (website available at: link)
- *Third Barcelona Techno Week – Course on semiconductor detectors*, organized by **Institute of Cosmos Sciences within Barcelona University**, July 2nd – 6th 2018, Barcelona, Spain. (website available at: link)
- *SERESSA 2017 – The 13th International School on the Effects of Radiation on Embedded Systems for Space Applications*, organized by **Spectrum Aerospace with Technical University of Munich**, October 23rd - 26th 2017, Munich, Germany. (website available at: link)
- *ESIPAP 2017 – European School of Instrumentation in Particle & Astroparticle Physics*, organized by **European Scientific Institute (ESI)**, February 20th to March 17th 2017, Archamps, France. (website available at: link)
- *ISOTDAQ 2016 – International School of Trigger & Data Acquisition*, organized by **Weizzman Institute of Science**, January 24th to February 2nd 2016, Rehovot – Tel Aviv, Israel. (website available at: link)

6.4 Future Perspectives

During my PhD program, I have gained a vast experience in developing high performance FPGA-based DAQ systems intended to power, control and to read out complex integrated circuits in harsh environment with radiation background. The enormous knowledge involving the interaction of radiation with matter, directly correlated to semiconductor electronic devices, have proved to be very useful into preparation of complex systems operating such environments. Therefore, I will continue the radiation testing program for new high density and high-performance FPGAs, as well as other complex integrated circuits proposed to operate in harsh environments with radiation background such as the space and the accelerator experiments.

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