



Europass Curriculum Vitae

Personal information

First name(s) / Surname(s)

Gabriel BANARIE

Work experience

Dates	
2002 – present	
Name and address of employer	Analog Devices International, Raheen Business Park, Limerick, Ireland
Type of business or sector	Semiconductor Industry
Occupation or position held	Senior Analogue IC Design Engineer
Main activities and responsibilities	<p>Top level architecture design for Sigma-Delta and SAR ADCs, embedded voltage references and temperature sensors.</p> <p>Mentoring junior engineers.</p> <p>Design and verification of analogue circuit blocks (amplifiers, voltage references, temperature sensors, etc.)</p> <p>Main projects:</p> <p><i>AD7745, AD7747</i> (monolithic capacitive to digital converters – CDC): Sigma-Delta modulator implementation, mathematical analysis of modified front-end and implementation of common mode correction interface (two US patents), work in top level mix-signal verification.</p> <p><i>ADuC7030</i> (automotive battery sensor): design work in voltage reference and crystal oscillator blocks.</p> <p><i>ADuC7224</i> (micro-converter ASIC for Velux): Design work on power line digital interface, work in top level mix-signal verification.</p> <p><i>AD7150</i> (automotive CDC for keyless entry systems): Sigma-Delta modulator design and implementation, work in top level mix-signal verification.</p> <p><i>AD7780</i> (low power, low cost ADC for weigh scales): Sigma-Delta modulator design and implementation, work in top level mix-signal verification.</p> <p><i>AD7190</i> (industrial sigma-delta ADC): Sigma-Delta modulator design and implementation, input current cancelling design for capacitive programmable gain amplifier (PGA) front-end, work in top level mix-signal verification.</p> <p><i>AD7154</i> (automotive complex impedance to digital converter): Signal chain design including complex calibration technique (patented) and Sigma-Delta modulator followed by single bin DFT filtering technique, design and implementation of various analogue blocks, work in top level mix-signal verification.</p> <p><i>AD7180</i> (automotive ASIC for complex impedance measurement): providing technical expertise for implementation of complex calibration.</p> <p><i>AD7175</i> (high FoM industrial Sigma-Delta ADC): multi-bit architecture design (patented), second order mismatch error shuffling architecture design (patented), design and implementation of various analogue blocks, work in top level mix-signal verification.</p> <p><i>AD7124</i> (low power, high FoM Sigma-Delta ADC): lead analogue designer, architecture design, voltage reference architecture design and implementation.</p> <p><i>AD7606B</i> (16-bit, simultaneous sampling, analog-to-digital data acquisition system (DAS) with eight channels, each channel containing analog input clamp protection, a programable gain amplifier (PGA), a low-pass filter, and a 16-bit SAR ADC): architecture and implementation of converter cores.</p>

Dates **1999 – 2001**

Name and address of employer **University Politehnica of Bucharest, Romania**

Type of business or sector 3rd level education

Occupation or position held **Assistant Lecturer**

Main activities and responsibilities Coordinating seminars and laboratory activities for undergraduate engineering students in following modules:
Signals, Circuits and Systems
Coding and Compression of Audio Signals
Adaptive Filtering.

Education and training

Dates 2015 – 2021

Title of qualification awarded PhD in Electronic Engineering
Thesis: “Advanced Monolithic Temperature Sensors”.

Name and type of organisation providing education and training University Politehnica of Bucharest, Romania

Dates 2008 – 2010

Title of qualification awarded Master of Engineering in VLSI Systems
Final project “Multi-bit Sigma-Delta Modulator Suitable for DC Input Signals”.

Name and type of organisation providing education and training University of Limerick, Ireland

Dates 1994 – 1999

Title of qualification awarded Bachelor of Engineering in Digital Communications and Multimedia Systems
Final project “Software Implementation for Blind Decoding using Viterbi Algorithm”.

Name and type of organisation providing education and training University Politehnica of Bucharest, Romania

Personal skills and competences

Mother tongue(s) **Romanian**

Other language(s)

Self-assessment
European level ()*

English

French

Italian

Understanding				Speaking				Writing	
Listening		Reading		Spoken interaction		Spoken production			
C2	Proficient user	C2	Proficient user	C2	Proficient user	C2	Proficient user	C2	Proficient user
B1	Independent user	C1	Proficient user	B1	Independent user	B1	Independent user	B1	Independent user
A2	Basic user	B1	Independent user	A1	Basic user	A1	Basic user	A1	Basic user

(*) [Common European Framework of Reference for Languages](http://www.cedefop.europa.eu/en/files/questdocument/1482/14822010.pdf)

<p>Research</p>	<p>Co-author of nine US patents (US10236905B1, US9806552, US9800262, US9600014, US9389275, US9124290, US8653996, US7304483, US7235983) in the area of Sigma-Delta, sensor signals acquisition and measurement, voltage references, and temperature sensors.</p> <p>Author or co-author of seven papers presented to internal ADI technical conferences.</p> <p>Co-author of a paper at the ISSC 2018 technical conference, Belfast, UK.</p> <p>Co-author of a paper at the MIXDES 2018 technical conference, Gdynia, Poland.</p> <p>Co-author of a paper at the ISSCS 2017 technical conference, Iasi, Romania.</p> <p>Co-author of a paper at the MIXDES 2017 technical conference, Bydgoszcz, Poland.</p> <p>Co-author of a paper at the ISSC 2015 technical conference, Carlow, Ireland.</p> <p>Presenter of a paper at the ISSC 2008 technical conference, Galway, Ireland.</p> <p>Co-author of a paper presented at the ADDA 2005 technical conference, Limerick, Ireland.</p> <p>Co-author of a paper published in <i>Sensors</i> 2005 IEEE journal.</p>
<p>Computer skills and competences</p>	<p>MATLAB, C (for circuit blocks modelling purposes), ADICE (ADI proprietary SPICE), Spectre RF, VerilogA.</p>
<p>Additional information</p>	<p>Member of IEEE (UK & Rep. of Ireland Section) since 2002.</p>