POLYTECHNIC UNIVERSITY OF BUCHAREST

Doctoral School of Electrical Engineering

PHD Thesis

Isolated step down DC-DC 3.2kW converter for electrical and hybrid vehicles

– Summary –

Author: Ing. Amir-Oliviu BOGZA

Scientific coordinator: Prof.dr.ing Dan FLORICĂU

Bucharest 2021

Content

Key words: Power electronics, isolated full bridge DC-DC converter, synchronous rectifier, electric vehicle (EV), hybrid vehicle (HEV, PHEV).

INTRODUCTION

The large number of cars around the world that use fossil fuels for propulsion generates serious environmental problems and affects people's comfort and health, the impact of which even becomes severe in large urban agglomerations. Given the increasingly rapid depletion of natural resources, battery-powered electric cars (BEV – Battery Electric Vehicle) and hybrid cars (HEV – Hybrid Electric Vehicle, PHEV – Hybrid Electric Vehicle Plugin) are becoming a solution of interest for the replacement of conventional cars.

We are currently seeing a sustained increase in the number of electric cars sold globally. It is estimated that by 2040, 35% of the total number of newly sold cars will be electric according to Bloomberg [1]. The main driver of this increase will be the continuous decrease in the cost of batteries and the significant increase in the use of electric cars for public transport and future autonomous cars. This paper aims to make important contributions in the field of design and optimization of DC-DC power converters used in electric cars. The DC-DC converter plays an essential role in the proper functioning, safety and efficiency of an electric car. The role of this converter is well defined, being highlighted in the block wiring diagram of the car.

Block electrical diagram of an electric car

In Fig.1 the typical electrical diagram of an electric car is shown.

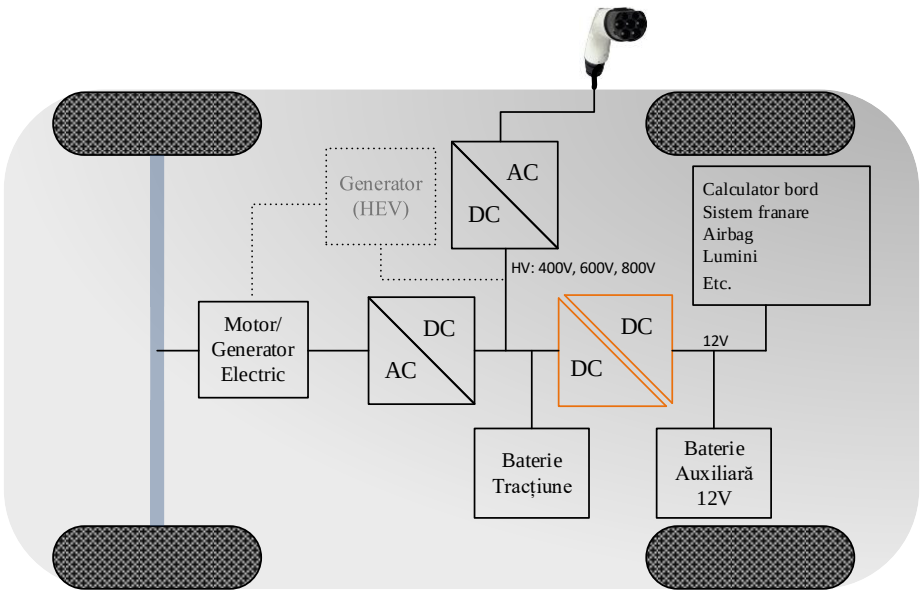


Fig. 1 Typical block electrical diagram of an electric car.

It can be seen that the electrical network of an electric car is complex, containing several blocks as follows:

Electric motor – ensures the conversion of electricity into mechanical energy necessary for propulsion. In general, the electric motor is designed to allow working in generator mode in order to recover the braking energy.

Inverter – is a DC-AC converter that converts the continuous voltage of the main (traction) battery into a three-phase alternating voltage required for the electric motor. Most often, this converter is bidirectional to allow the brake energy to be recovered and stored in the main battery by using the engine in generator mode.

On-board charger – is an AC-DC converter that ensures the charging of the main battery of the car from the grid electrical network. More recently, this converter can also be bidirectional, allowing the transfer of energy from the car to the electrical network through a concept called V2G (vehicle-to-grid) [2].

DC-DC converter – ensures the conversion of energy from the main battery to the auxiliary low voltage battery (12V) supplying vital consumers of the car such as:

- On-board computer;
- Airbags; Braking system;
- Steering system;
- Lighting system;
- Fans, pumps, actuators;
- Infotainment (GPS, multimedia systems, etc.).

Due to these functions, the operating, reliability and safety specifications of this converter are very strict. Failure to function properly or failure of this converter can lead from the limitation of performance to the immediate stop of the car.

Thesis content

This paper is structured as follows: introduction, six chapters and general conclusions:

- Introduction
- CAP. 1 – Topologies used for DC-DC conversion
- CAP. 2 – Dimensioning of power components and calculation of efficiency
- CAP. 3 – Design and optimization of the leakage inductor
- CAP. 4 – Analysis and optimization of magnetic components
- CAP. 5 – Parallel connection of full bridge converters
- CAP. 6 – Practical realization of the converter
- General conclusions

In CAP. 1 the main DC-DC conversion topologies are reviewed and evaluated according project specifications. In the first section, the topology for the primary side is chosen and in the second section the optimal topology for the secondary side (rectifier) is selected. Selection of

topologies is done after evaluation of the advantages and disadvantages of alternative topologies. In the end, the electrical schematic was designed and the concept was verified by simulation.

In CAP. 2 a new calculation method for sizing the power components of the phase-shifted bridge converter is presented. Thus, starting from the project specifications, it was proceeded to choose the transformer ratio, to calculation of the output inductors, the RMS currents and the power dissipated on the power elements of the converter. After calculating the voltage and current stress for each section of the converter, the semiconductor and magnetic components were selected. In the last section of this chapter, the total losses were calculated and the efficiency curve for different input voltages was drawn.

In CAP. 3 a new method for calculating the leakage inductance for the full-bridge phase-shifted converter is proposed. The proposed method takes into account most of the parameters of the converter such as: input voltage, output voltage, output current, magnetization inductance, equivalent series resistors of power semiconductors and magnetic elements . After calculating the minimum value of the leakage inductance, its value is optimized by adjusting the magnetization inductance of the power transformer.

In CAP. 4 the design and optimization of the magnetic power components using the finite element (FEM) method was done. This method is used to evaluate and optimize the performance of the power transformer, the leakage inductor and the output inductior. Using the FEM method, the parameters and losses of the magnetic components were determined and basing on these parameters, the optimal configurations were selected. The main advantage of this method is that it allows the analysis and optimization of magnetic components without the need for a physical prototype.

In CAP. 5 the main methods of balancing output currents between parallel-connected DC-DC converters were analyzed. Thus, after comparing the advantages and disadvantages of the various known methods, the optimal current balancing solution was chosen. This solution was first implemented at the simulation level and then it was experimentally verified on a functional prototype.

In CAP. 6 the implementation of the converter designed in the previous chapters was carried out with the aim of evaluating its performance. In the first two sections, the block diagram was presented and a picture of the prototype detailing the functional blocks was presented. In the third section, measurements of the converter waveforms were made in static and dynamic mode, then an infrared scan of the top surface of the prototype was presented to highlight the temperature distribution. In the last section, efficiency measurements were done at three input voltages (minimum, nominal and maximum).

CAP. 1 TOPOLOGIES USED FOR DC-DC CONVERSION

For DC-DC conversion of energy, a wide range of topologies is available which can be used. They can be split into two categories, non-isolated and isolated. Non-isolated topologies assume the existence of a common connection between the energy source at the input of the converter and its output. Isolated topologies involve galvanic isolation between the input and output of the converter by using a separating transformer.

The selection of the topology is an important step in the design of the converter. It is chosen according to the application, aiming to meet the requirements of the project:

- Nominal output power;
- Galvanic isolation (if needed);
- Efficiency;
- Input/output voltage range;
- Output nominal current.

1.1 Non-isolated topologies

Table 1.1 shows the main types of converters used for DC-DC conversion without galvanic isolation [3], [4]. At the same time, we also find the transfer function in continuous conduction mode depending on the duty-cycle (D), where the duty-cycle is given by the relationship below:

$$D = \frac{T_{on}}{T} \tag{1.1}$$

It was noted with T_{on} the duration during the switch is controlled in ON state (in conduction), and with T the commutation period expressed by the relation:

$$T = \frac{1}{f} \tag{1.2}$$

where, f is the converter switching frequency.

When choosing the topology of the converter, the aim is to use a minimum number of power switches with nominal voltages and currents in order to lead to an optimal solution from technical and cost point of view, at the same time respecting the project specifications.

Considering the transfer function and the duty-cycle D that has values between 0 and 1, we can deduce that the *Buck* topology is a step down converter and the *Boost* is a step up converter. Therfore, the output voltage is always lower than the input voltage in the case of *Buck* and higher than the input in the case of Boost converter.

Buck-Boost, Cuk and Sepic topologies can be both step down (D<0.5) and step up (D<0.5) depending on the value of the duty-cycle. As can be seen, the output voltage can have the same polarity as the input voltage (*Buck, Boost, Sepic*) or opposite polarity (*Buck-Boost, Cuk*).

Table 1.1 Non-isolated DC-DC converter topologies

Topology	Transfer function	Switch voltage stress
Buck	D	$V_{Q1} = V_i$
Boost	$\frac{1}{1-D}$	$V_{Q1} = V_i$
Buck-Boost	$-\frac{1}{1-D}$	$V_{Q1} = V_i + V_o$
Cuk	$-\frac{D}{1-D}$	$V_{Q1} = V_i - V_o + \frac{V_{c1\_riplu}}{2}$
Sepic	$\frac{D}{1-D}$	$V_{Q1} = V_i + V_o + \frac{V_{c1\_riplu}}{2}$

1.2 Isolated DC-DC topologies

Table 1.2 shows the main topologies used for DC-DC conversion that ensure galvanic isolation [3], [4]. In order to have galvanic separation it is necessary to use an isolation transformer between the primary and secondary switching circuits. Galvanic separation is mainly used when:

- It is desired to isolate the secondary circuit from the primary one for safety reasons;
- The ratio of the input and output voltage is high resulting in a very low duty-cycle ratio (D < 0.2);
- Multiple output voltages with the same polarity or opposite are required.

Table 1.2 Isolated DC-DC topologies

Topology	Transfer function	Switch voltage stress
Flyback	$\frac{D}{1-D} \cdot \frac{Ns}{Np}$	$V_{Q1} = V_i + V_o \cdot \frac{Ns}{Np}$
Forward	$D \cdot \frac{Ns}{Np}$	$V_{Q1} = 2 \cdot V_i$
Push-Pull	$2D \cdot \frac{Ns}{Np}$	$V_{Q1} = 2 \cdot V_i$
Half Bridge	$D \cdot \frac{Ns}{Np}$	$V_{Q1} = V_i$
Full Bridge	$2D \cdot \frac{Ns}{Np}$	$V_{Q1} = V_i$
Full Bridge Phase Shifted	$D_{eff} \cdot \frac{Ns}{Np}$	$V_{Q1} = V_i$

In addition to the notations in the previous section, it was noted with Np the number of turns of the primary winding and with Ns the number of turns of the secondary winding of the isolation transformer.

The *Flyback*, *Forward* and *Push-Pull* topologies lead to a voltage stress for power switch up to twice the input voltage of the converter. *Flyback* and *Forward* converters are mainly used at low power (<200W) and P*ush-Pull* converter is generally used when the input voltage of the converter is below 200V.

For input voltages higher than 200V and powers above 0.5kW, half bridge, full bridge or full bridge phase shifted converters are preferred because they lead to optimal use of power switches.

1.3 Selection of the topology for the primary circuit of the converter

Given the range of the input voltage (240V... 430V), the output power level of 3.2kW and the need for galvanic separation, for this application the full-bridge phase shifted converter will be selected. It ensures an efficient use of the transformer, a voltage stress equal (theoretically) to the input voltage and most importantly, the possibility to achieve zero voltage witching (ZVS) for the power switches by using of stored energy in the parasitic circuit elements.

1.4 Secondary rectifier circuit

Given the topology already selected for the primary circuit, the optimal variant for the secondary rectifier circuit [4], [5] must be selected. Since for bridge converter the voltage available at the terminals of the secondary winding of the transformer is bipolar, a full wave rectifier is needed for the secondary side. In Fig. 1.1 two types of full wave rectifier circuits are presented: center taped and current doubler rectifier [5].

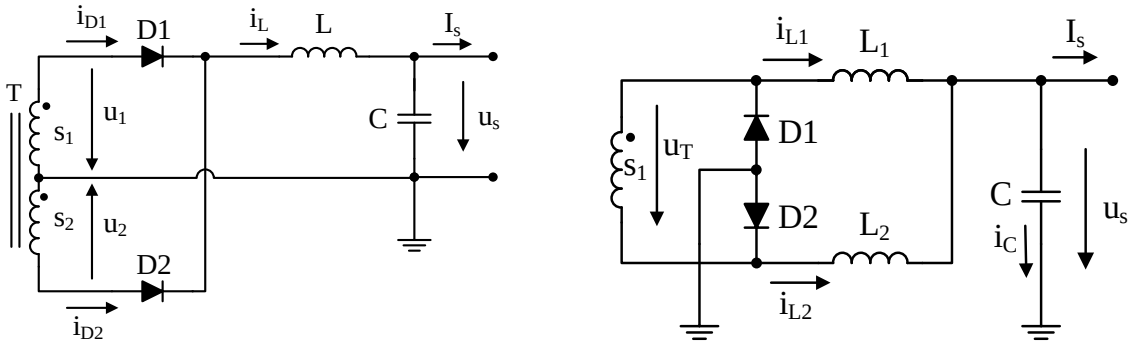


Fig. 1.1 Full wave rectifiers topologies.

A comparison of the two variants is given in Table 1.3. Analyzing the advantages and disadvantages of the two rectifier structures, the current doubler rectifier is be selected.

Table 1.3 Center tapped and current doubler topologies comparison

Type	**Center tapped**			**Current doubler**		
Magnetic components	**S_1**	**S_2**	**L**	**S**	**L1**	**L2**
Switching frequency	$\frac{f_c}{2}$		f_c	$\frac{f_c}{2}$		
Primary no. of turns	N			N		
Secondary no. of turns	1	1	-	2	-	-
RMS currents	$\frac{I_s}{2}$	$\frac{I_s}{2}$	I_s	$\frac{I_s}{2}$	$\frac{I_s}{2}$	$\frac{I_s}{2}$
Output inductor	-	-	L	-	≤ L	≤ L

1.5 Simulation of the Full-Bridge Phase Shifted converter

Two possible implementations will be analyzed, the rectifier made with diodes and synchronous rectifier.

1.5.1 Diode rectifier

For the beginning, the full-bridge phase shifted converter with diodes rectifier will be evaluated. This type of rectifier is very common in DC-DC converters due to its simplicity. The simulation schematic diagram is shown in Fig. 1.2 [6], [7].

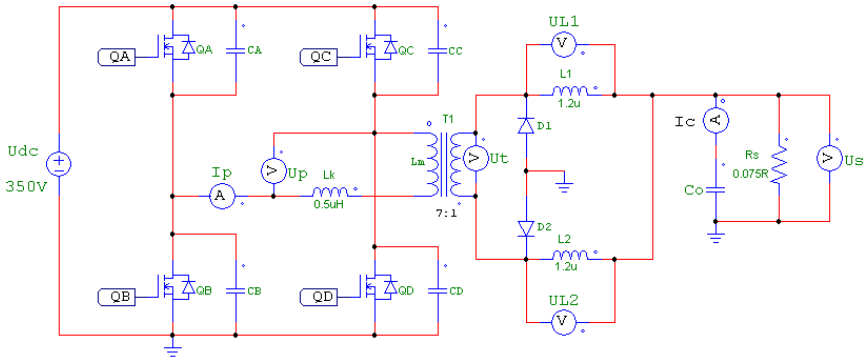


Fig. 1.2 Electrical schematic for simulation of the full-bridge phase shifted converter with diode current doubler.

The diode rectifier is a simple solution and is recommended in situations where the rated output current is small enough so that conduction losses on diodes due to power failure are acceptable. At high currents, this solution becomes impractical.

1.5.2 The full-bridge phase shifted converter with synchronous current doubler rectifier

The implementation of a synchronous rectifier is achieved by replacing the rectifier diodes D1 and D2 in the power schematic with power semiconductor devices such as

MOSFETs (METAL Oxide Semiconductor Field Effect Transistor) devices. he MOSFET switches exhibit very low ON resistance and high switching speed compared to bipolar or IGBT transistors. The electrical diagram is shown in Fig. 1.3. For the converter simulation, the following values for the converter components were considered: CA-CD = 120pF, Co = 120µF, Lm = 80µH, Fsw = 200kHz.

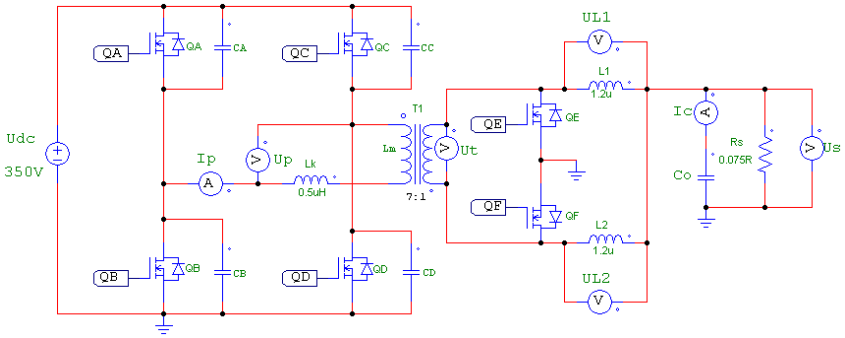


Fig. 1.3 Electrical simulation schematic of the converter

The electrical control diagram can be found in Fig. 1.4. It also contains the activation signals of the two power switches QE and QF.

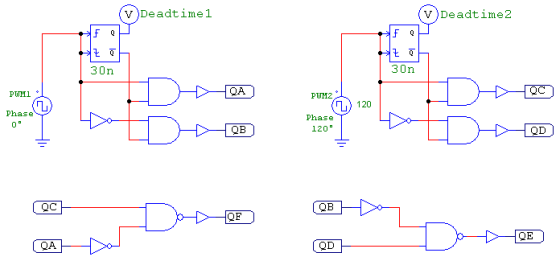
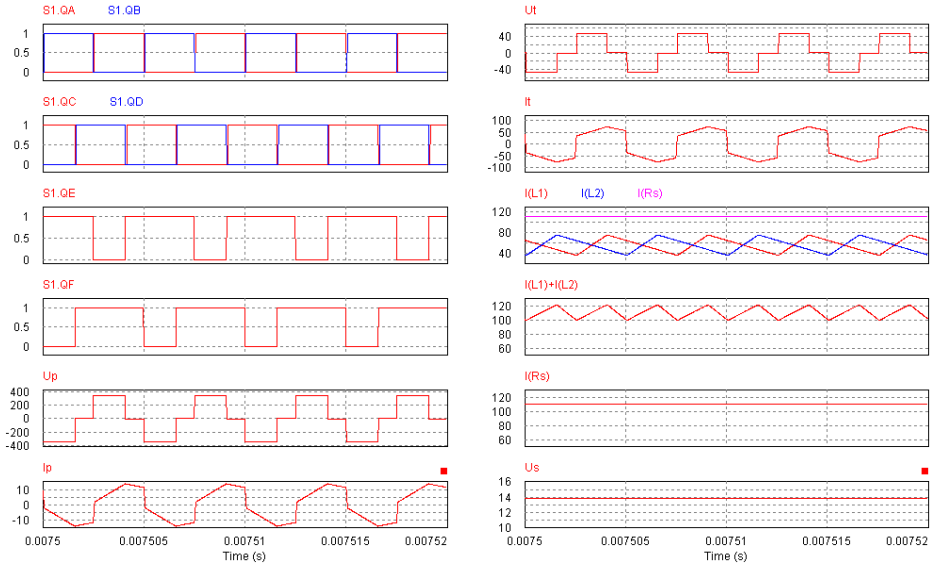


Fig. 1.4 Electrical schematic of the control circuit.



a) Primary side waveforms b) Secondary side waveforms

Fig. 1.5 Simulation of full-bridge converter with synchronous current doubler rectifier.

The simulation results of the full-bridge converter with synchronous current doubler rectifier are shown in Fig. 1.5.

1.6 Conclusions

In this chapter, the main topologies of DC-DC converters were evaluated and the optimal topologies were chosen for the two sections of the converter, primary and secondary.

CAP. 2 DIMENSIONING OF POWER COMPONENTS AND EFFICIENCY CALCULATION

For the sizing of the components, various methods are found in the literature [8], [9]. In general, the calculation of components is done without taking into account the loss of duty-cycle due to the leakage inductance, series resistances in conduction of power switches, transformers and inductors in the power circuit. This can lead to the design the power transformer with inadequate tunrs ratios and to insufficient output voltage under maximum load [10], [11], [12], [13].

The high efficiency at light load makes the design of the converter based on a single power module very difficult to achieve because no load losses are proportional to the rated power. In order to be able to achieve the efficiency targets, the total power of the converter will be divided into two identical power modules [14]. The power schematic of the converter with two modules connected in parallel, is shown in Fig. 2.1.

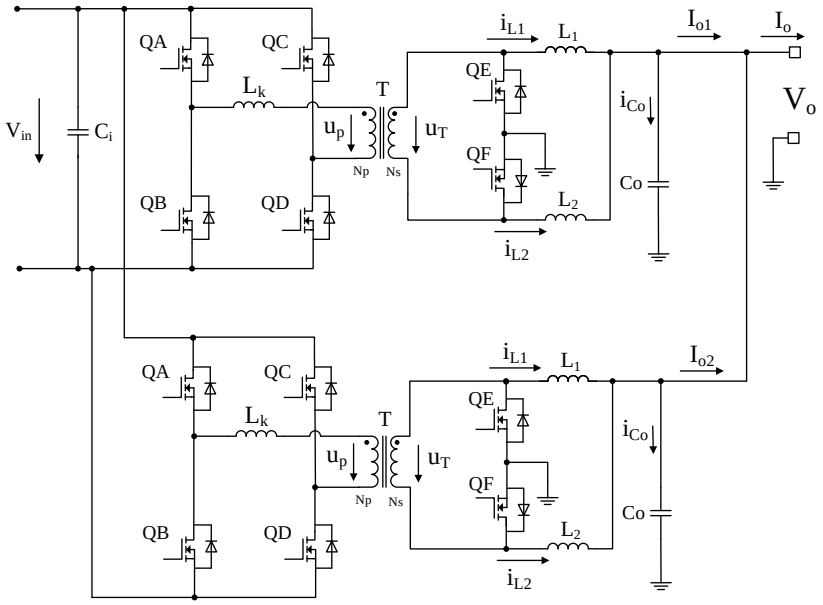


Fig. 2.1 The power schematic of the converter with two modules connected in parallel.

The division of the converter power schematic into two identical modules sized at half of the rated output has the following advantages:

- easy cooling due to the uniform distribution of losses;

- high efficiency at low load by turning off one module;
- redundancy if one module fails;
- reduced current ripple through the input and output capacitors by using the phase shifted control for the two modules.

2.1 Converter final specifications

In Table 2.2, the final specifications of the converter are given, considering the division of the power schematic into two identical modules.

Table 2.2 Final specifications of the DC-DC converter

Specification	**Module 1**	**Module 2**	**Modules 1+2**
Output power	1.6kW	1.6kW	3.2 kW
Input voltage	345 V (260 V– 420 V)		
Output voltage	14 V (12 V– 16 V)		
Output current	115 A	115 A	230 A
Efficiency	90% 93% 92%	Io = 0.15·In Io = 0.5·In Io = 1.0·In	

2.2 Power transformer turns ratio calculation

The turns ratio can be deducted from the converter transfer function:

$$\frac{Np}{Ns} = \frac{Vin_{\min}}{Vo_{\max}} \cdot D_{\max} \tag{2.1}$$

where, $Vin_{\min}$ is the minimum input voltage, $Vo_{\max}$ is the maximum output voltage, Ns/Np is the turns ratio iar $D_{\max}$ the maximum allowed duty-cycle.

2.3 Deduction of the ideal and effective duty-cycle

The ideal duty-cycle can be found by replacing the nominal operating parameters in the converter transfer function in Table 2.2.

$$D = \frac{Vo}{Vin} \cdot \frac{Np}{Ns} \tag{2.2}$$

Since the equation (2.2) refers to the ideal duty-cycle, voltage drops on the leakage inductance L_k and non-ideal circuit elements are not considered. If all these voltage drops are taken into account, the effective duty-cycle become:

$$D_{eff} = \frac{Vo + \delta Vo}{Vin - \delta V_{Lk} - \delta V_{TR} - \delta V_{Rdson}} \cdot \frac{Np}{Ns} \tag{2.3}$$

where, was noted with δV_{Lk} the voltage drop on leakage inductance, with δV_{TR} voltage drop on power transformer windings, with δV_{Rdson} the voltage drop on the power switches during conduction and with δVo the voltage drop on output inductor.

2.4 Dimensioning of the output inductor

In this section, the output inductance value, the peak and the effective current through inductor as well as the maximum core flux density are calculated.

2.4.1 Output inductor value calculation

The output inductance value is calculated according to the relation below:

$$Lo = \frac{Vin \cdot \frac{Ns}{Np} \cdot D \cdot (1-D)}{\Delta i_{Lo} \cdot Fsw} \tag{2.4}$$

where, was noted with Δi_{Lo} the inductor ripple current .

2.4.2 Calculation of the peak and RMS inductor current

To calculate the RMS current, the waveform of the current through the inductor will be used during a commutation period. Thus, the maximum (I_{Lo_max}) and minimum (I_{Lo_min}) values of the current through the output inductors of the converter are:

$$I_{Lo\_\max} = \frac{Io}{2} + \frac{\Delta i_{Lo}}{2} \tag{2.5}$$

$$I_{Lo\_\min} = \frac{Io}{2} - \frac{\Delta i_{Lo}}{2} \tag{2.6}$$

The inductor RMS current is given by the equation below:

$$I_{Lo\_rms} = \int_{DT}^{T} \left(i_{Lo}(t)\right)^2 dt = \sqrt{\frac{I_{Lo\_\min}{}^2 + I_{Lo\_\max}{}^2 + I_{Lo\_\max} \cdot I_{Lo\_\min}}{3}} \tag{2.7}$$

2.4.3 Selection of magnetic core and calculation of maximum flux density

The maximum flux density in the magnetic core is calculated according to the peak current thorugh the inductor, the number of turns and cross section of the core. The value of the maximum flux density in the core is calculated with the relation below:

$$B_{\max} = \frac{Lo \cdot I_{Lo\_\max}}{N_{Lo} \cdot Ac} \tag{2.8}$$

where, N_{Lo} is the number of turns of the inductor and Ac is the area of the core.

For this application, a ferrite type material 3C90 from the Ferroxcube manufacturer was selected [16] due to the high switching frequency and high saturation flux density.

2.5 Dimensioning of the power switches from the secondary circuit

When choosing the type of power switch, the switching frequency, the voltage at the terminals during the operation, the peak and RMS current values through the switch must be considered.

2.5.1 Calculation of maximum and RMS currents in the secondary circuit

The rectifier circuit is a full wave type having two branches with two power switches QE and QF. The current through each branch of the rectifier is equal to the sum of the output inductor currents.

The value of the RMS current passing through the power switch of the rectifier circuit is:

$$I_{SR\_RMS} = \sqrt{D \cdot I_{SR\_RMS\_ON}{}^2 + (0.5 - D) \cdot I_{SR\_RMS\_FW}{}^2} \tag{2.9}$$

2.5.2 Selection of the power switch for synchronous rectifier

A power switch which fits well to this application is for example *AUIRF7669L2* from the manufacturer Infineon Technologies [18]. This MOSFET power switch is small in size and has low switching time and equivalent low drain-source resistance (4.4mΩ @ Tj = 100°C).

2.6 Dimensioning of power switches for the primary circuit

For selection of power switches for the primary side, the same parameters of the converter as those of the secondary circuit will be considered: the switching frequency, the maximum operating voltage, the maximum and effective value of the current through the device.

2.6.1 Calculation of currents value through power switches from the primary circuit

In order to determine the currents through power switches from the primary side, the waveforms of the voltages and currents in the primary of the transformer [15] is analyzed. During converter conduction interval **[0, DT]**, when the energy is transferred from the input source to the secondary circuit, the RMS current in the primary winding is:

$$Ip_{rms\_ON} = \sqrt{\frac{\mathrm{I}\,p_{\min}{}^2 + \mathrm{I}\,p_{\max}{}^2 + \mathrm{I}\,p_{\min} \cdot \mathrm{I}\,p_{\max}}{3}} \tag{2.10}$$

During freewheeling interval **[DT, (0.5-D)T]**, the energy stored in the leakage inductance (L_k) will circulate through both the primary and secondary circuits, so the RMS current during this interval is:

$$Ip_{rms\_FW} = \sqrt{\frac{I\,p_{\min 2}{}^2 + I\,p_{\max}{}^2 + I\,p_{\min 2} \cdot I\,p_{\max}}{3}} \tag{2.11}$$

Taking in the account the duty-cycle, it is possible to calculate the RMS current through power switch in the primary circuit:

$$I_{PR\_RMS} = \sqrt{D \cdot Ip_{rms\_ON}{}^2 + (0.5 - D) \cdot Ip_{rms\_FW}{}^2} \tag{2.12}$$

By using the below equation, the value of the RMS current from the primary winding of the transformer is obtained:

$$Ip_{RMS} = \sqrt{Ip_{rms}{}^2 + Ip_{rms}{}^2} \tag{2.13}$$

2.6.2 Selection of the power switch for the primary circuit

A MOSFET device optimized for this type of application will be selected. One such device is IPB65R110CFDA in CoolMOS technology from the manufacturer Infineon Technologies [19]. According to the specifications, this power switch has a nominal voltage of 650V, a drain-source resistance of 180mΩ and a nominal current of 19.7A@100°C.

2.7 Calculation of available energy in leakage inductance

Under nominal operating conditions, the current in the primary winding of the transformer before the polarity change is I_{pmin2}. Therefore, the energy stored in the leakage inductor is:

$$E_k = \frac{1}{2} \cdot L_k \cdot Ip_{\min 2}{}^2 \tag{2.14}$$

2.8 Output capacitor calculation

The capacitance value of the output capacitor is determined according to the maximum accepted ripple of the output voltage of the converter. The maximum ripple of current through the capacitor is given by the sum of the currents of the two output inductors and is reached during the conduction interval [0, DT]:

$$\delta I_{Co} = \Delta i_{L1} + \Delta i_{L2} \tag{2.15}$$

The required minimum output capacitance is:

$$Co_{\min} = \frac{\delta I_{Co}}{8 \cdot \Delta Us \cdot Fsw \cdot 2} \tag{2.16}$$

2.9 Calculation of converter losses

In order to calculate the efficiency of the converter, it is necessary to calculate the power losses on all the circuit elements of the converter.

2.9.1 Losses in the output inductors

Power losses in the output inductors consist in losses due to resistance of the windings and due to magnetic core.

$$P_{Lo} = P_{DCR\_Lo} + P_{core\_Lo} \tag{2.17}$$

It was noted with P_{DCR_Lo} the power loss due to DC resistance of the inductor winding and P_{core_Lo} the power loss in the magnetic core.

2.9.2 Power losses on power switch from the primary circuit

The power dissipation on the power switches in the primary circuit is equal to the sum between conduction and switching losses.

$$P_{PR} = P_{cond\_PR} + P_{sw\_PR} \tag{2.18}$$

2.9.3 Power dissipated on power switches from the secondary circuit

The losses on power switches from the rectifier circuit are calculated similarly to those for primary circuit:

$$P_{SR} = P_{cond\_SR} + P_{sw\_SR} \tag{2.19}$$

2.9.4 Losses in the power transformer

Similarly to output inductors, losses in the transformer are composed of losses due to the resistance of the windings and losses in the magnetic core:

$$Pt = P_{res\_prim} + P_{res\_\sec} + Pt_{core} \tag{2.20}$$

2.9.5 Power consumed by control circuits

The power consumed for activating and deactivating power semiconductor devices is:

$$P_{DRV} = V_{cc}\left(4Qg_{PR} + 4Qg_{SR}\right)\cdot Fsw \tag{2.21}$$

where, it was noted with Vcc the supply voltage of the control circuit, with Qg_{PR}, Qg_{SR} the gate charge of the primary and secondary power switches which must charged/discharged during each switching cycle.

2.9.6 Power dissipated due to voltage stress limiting circuits

In order to prevent a possible situation where the voltages may exceed the nominal voltage power switches, containment measures must be implemented. A simple method is to connect a series RC (resistance-capacitor) circuit to the terminals of the element to be protected as shown in Fig. 2.3 [20]. The power dissipated on the resistor Rs can be calculated with the relation below:

$$P_{snubber} = 2 \cdot Cs \cdot \left(Vin \cdot \frac{Ns}{Np} \right)^2 \cdot Fsw \tag{2.22}$$

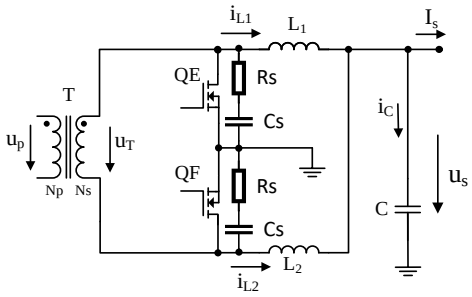


Fig. 2.2 RC circuit series for limiting the voltage stress (Rs, Cs).

2.10 Loss balance and efficiency calculation

The total power dissipated under nominal operating conditions is given by the sum of the losses on all elements of the converter previously calculated:

$$Pd = 2 \cdot P_{Lo} + 4 \cdot P_{PR} + 2 \cdot P_{SR} + Pt + P_{DRV} + P_{snubber} \tag{2.26}$$

In Fig. 2.3, the balance of the power losses on the main elements of the converter at nominal output power and at nominal input voltage is presented. The loss balance is also represented in percentage pie graph.

Section	Power loss
Output inductors	20.28 W
Primary power switches	33.96 W
Secondary power switches	36.96 W
Transformer	15.04 W
Control circuits	1.91 W
Voltage stress limiting circuits	0.46 W
Total power loss	108.6 W
Output power	1610 W
Efficiency	**0.936**

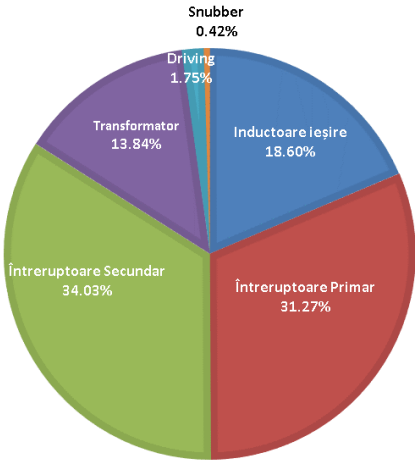


Fig. 2.3 Power losses at nominal operating conditions.

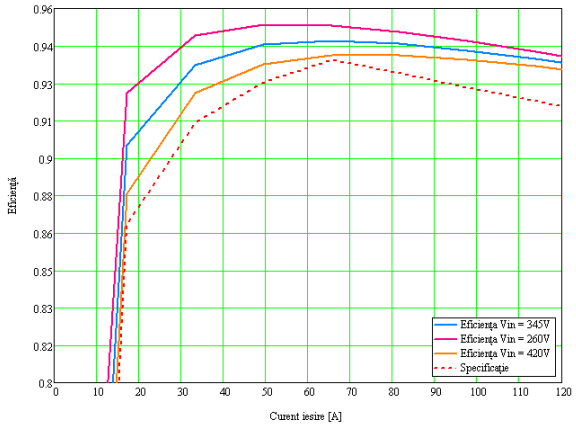


Fig. 2.4 Calculated efficiency of the converter according to the output current and the input voltage.

From the analysis of the efficiency graphs in Fig. 2.4, it can be seen that the efficiency of the converter varies significantly with the supply voltage especially at low and medium output load. At large output currents, close to the rated current, the efficiency of the converter is much less dependent on the input voltage.

2.11 Conclusions

In this chapter, a calculation method for a full-bridge phase shifted converter equipped with a double current rectifier was presented. Starting from the specifications of the DC-DC power converter, it was proceeded to the choice of the transformation ratio, the calculation of the output inductors, of the RMS currents and power dissipated on the power elements of the converter. After calculating the voltage and current stresses for each section of the converter, the semiconductor and magnetic components were selected.

CAP. 3 Calculation of the leakage inductance value

In this chapter, a method for calculation of the optimal value of the leakage inductance is presented. An optimal value ensures ZVS performance conditions in the primary circuit over a wide range of converter operation and with a minimum duty-cycle. The advantage of switching in ZVS mode is that the energy from the leakage inductance is transferred to the parasitic capacitances without power dissipation. With this mechanism, the total losses on the primary circuit are greatly reduced and the efficiency of the converter increases significantly [21], [22], [23], [24].

3.1 Deduction of design equations for the leakage inductance

In Fig. 3.1 the electrical schematic of the full-bridge phase shifted converter with the parasitic capacities of other semiconductor devices (CA, CB, CC, CD) is presented. The sizing of the additional leakage inductance must be made in such a way to obtain ZVS for the primary power switches over a wide range of output current, input voltage and output voltage [15].

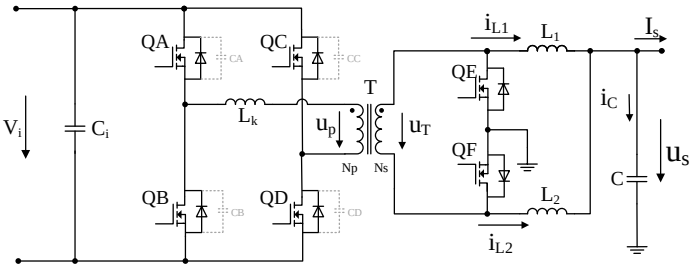


Fig. 3.1 Converter power schematic with highlighted parasitic capacitances.

To calculate the leakage inductance value the following parameters of the converter will be taken into account: the drain-source parasite capacities of power switches, the parasitic capacitance of the power transformer, the minimum and maximum input voltage, the minimum output current from which the ZVS mode is desired.

The condition for achieving ZVS in the primary circuit is that the energy stored in the leakage inductor E_{Lk} is greater than or at least equal to the energy stored in the parasitic capacitance E_{cap} of the primary circuit.

$$E_{Lk} \geq E_{cap} \tag{3.1}$$

The energy stored in parasitic capacitance is:

$$E_{cap} = \frac{1}{2}\left(2C_{oss} + C_{tr}\right) \cdot V_{in}^2 \tag{3.2}$$

It was noted with Coss the parasitic capacitance of the primary power switch and with Ctr the parasitic capacity of the power transformer.

The energy stored by the leakage inductor is given by the relationship:

$$E_{Lk} = \frac{1}{2} L_k I_k^2 \tag{3.3}$$

where, L_k is the leakage inductance and I_k is the current value just before the state of the primary switch changes.

In the worst-case situation, I_k equals I_{pmin2} which is the instantaneous value of the current through primary winding of the transformer just before the voltage polarity changes.

The value of I_{pmin2} is given by the relationship below:

$$Ip_{\min 2} = \frac{1}{2} \cdot \left(\frac{N_s}{N_p} \cdot \left(I_o + \frac{\left(V_{in} \cdot \frac{N_s}{N_p} - V_o \right) \cdot D}{L_o \cdot F_{sw}} \right) \cdot e^{-\frac{R_e}{L_k}(0.5-D)\cdot T} + \frac{V_{in} \cdot D}{L_p \cdot F_{sw}} \right) \tag{3.4}$$

The total energy stored in leakage inductance available to achieve ZVS is obtained after replacing the result from (3.4) in equation (3.3).

$$E_{Lk} = \frac{1}{2} L_k \cdot \left(Ip_{\min 2}\right)^2 \tag{3.5}$$

According to equation (3.4) the energy stored in the leakage inductance available to achieve ZVS depends on several parameters: the equivalent series resistance of the power switches and inductors, the magnetization inductance of the transformer, the output inductance, the input/ output voltages, the output current and the switching frequency.

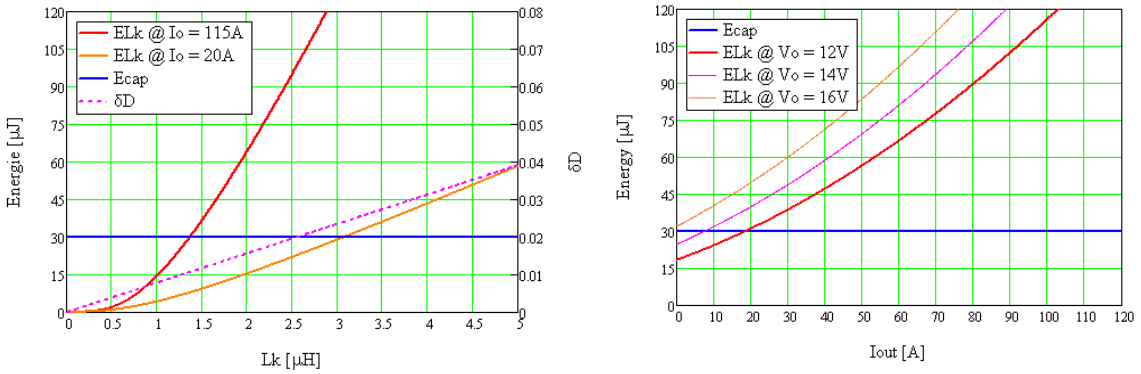
3.2 Leakage inductance design

The relationships deduced in the previous section will be used to find the optimal value of the leakage inductance. According to equation (3.2) the maximum energy stored in parasitic capacities in the primary circuit corresponding to the worst case conditions is:

$$E_{cap} = \frac{1}{2}\left(2C_{oss} + C_{tr}\right) \cdot V_{in\max}^2 = \frac{1}{2} \cdot \left(2 \cdot 120\,pF + 100\,pF\right) \cdot 420V^2 \approx 30\mu C \tag{3.6}$$

ZVS switching of the power switches in the primary circuit is possible only if the energy available in the leakage inductance is at least 30µC. In Fig. 3.2a equations (3.6) and (3.5) are shown in graphical form. From this graph one can extract the minimum value of the leakage inductance. This can be found at the intersection of the energy curve of leakage inductance E_{Lk} with the energy stored in the parasitic capacitances E_{cap}.

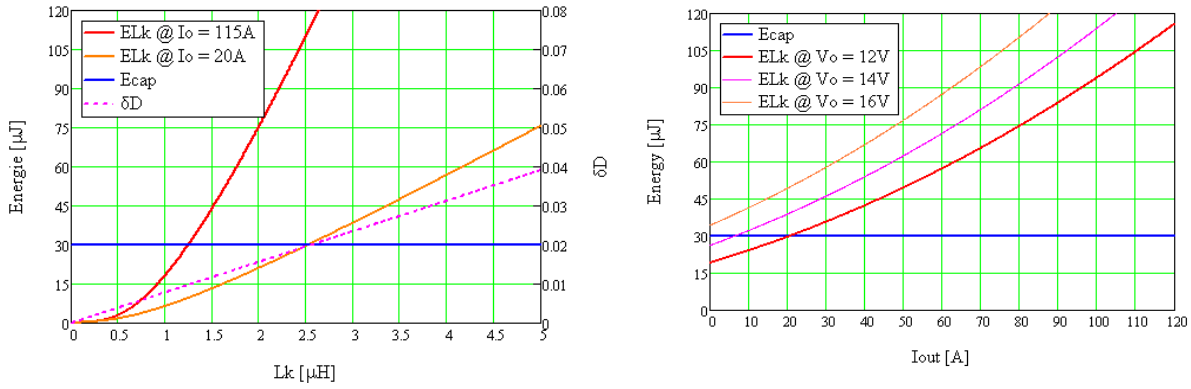
In order to achieve ZVS on a wide load current range (20A – 115A), the value corresponding to the minimum current will be selected, this point is at L_k = 3.15µH.



a) E_{Lk} dependency of L_k b) E_{Lk} dependency of the output voltage Iout

Fig. 3.2 Energy stored in the leakage inductance

According to the graphs in Fig.3.2b, reaching the ZVS switching regime depends significantly on both the load current and the programmed level of the output voltage. Fig. 3.3a shows the graph of the energy stored in the leakage inductance as a function of L_k, but for a magnetization inductance value L_p of 100µH. In this case, the minimum leakage inductance required to achieve ZVS is 2.5µH.



a) E_{Lk} as function of Lk

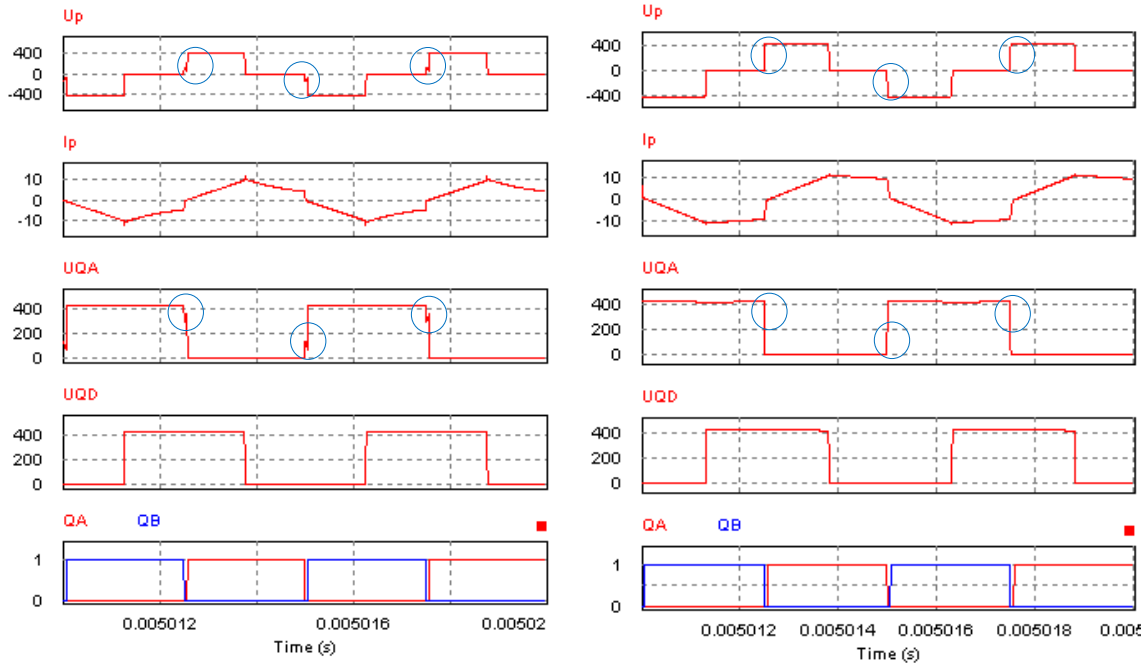
b) E_{Lk} as function of the output voltage and current

Fig. 3.3 E_{Lk} as function of the L_k for Lp = 100µH.

Fig. 3.3b shows the graph of the energy stored in the leakage inductance as function of output current and output voltage of the converter for L_k = 2.5µH and L_p = 100µH. The graph looks very similar to the one from Fig. 3.2 although the leakage inductance have been reduced by 25%. Increasing the energy stored in L_k by this method has the advantage that the energy required to achieve the ZVS is obtained with a lower voltage drop on leakage inductance.

3.3 Simulation of the converter at various values of L_k

In Fig. 3.4, the simulation results of the converter with the leakage inductance of 0.5µH and 2.5µH are presented.



a) Simulation with L_k = 0.5µH, Lp = 147µH

b) Simulation with L_k = 2.5µH Lp = 100µH

Fig. 3.4 Converter simulation for two values of L_k at V_{in}= 420V, V_o= 12V, I_o= 60A.

According to Fig. 3.4a, the energy stored by the leakage inductance is not sufficient to charge/discharge the parasitic capacities of QA and QB (see highlighted areas) for $L_k = 0.5\mu H$. For this reason, the power switches from the primary side cannot switch in ZVS mode, resulting in significant switching losses.

In the case of $L_k = 2.5\mu H$ from Fig. 3.4b, both arms of the primary bridge are switching in ZVS mode. Compared to Fig. 3.4a, the voltage at the terminals of QA is pushed to zero before the activation command arrives, so the power switch is activated with zero voltage at the terminals. Similarly, when deactivating, the voltage at the terminals of QA is brought to the level of the supply voltage before the deactivation command comes, so in the same way an effortless change of state for the power switches from the primary circuit.

3.4 Conclusion

In this chapter, a new calculation method for the leakage inductance for the full-bridge phase shifted converter was presented. The proposed method takes into account the main parameters of the converter: input/output voltages, output current, equivalent series resistors of the power elements and magnetization inductance.

CAP. 4 Analysis and optimization of magnetic components

In this chapter, the power magnetic components of the full-bridge phase shifted converter will be analyzed and optimized. This study will be carried out using numerical simulation with a simulation program that allows finite element analysis (FEM).

The FEM has been and is successfully used in the low-frequency range for modeling high-voltage three-phase transformers, asynchronous motors and generators [25], [26], [27], [28]. The method is also used at high frequencies to evaluate the performance of wireless power transfer [29], [30], [31], [32]. Fig. 4.1 shows the power electrical schematic of the converter where the magnetic components to be analyzed and optimized using the FEM method are highlighted.

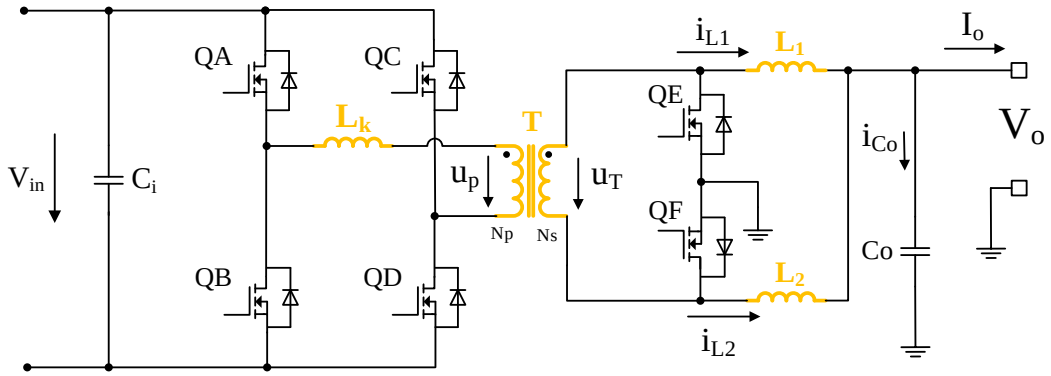


Fig. 4.1 Electrical power schematic of the converter.

The FEM method allows for an accurate evaluation of complex phenomena such as proximity and skin effects. The main advantage of this method being the possibility to evaluate, modify and optimize magnetic components without the need for a physical prototype.

4.1 Power transformer

The power transformer ensures the galvanic separation and energy transfer of the converter from the primary to the secondary circuit.

4.1.1 Transformer specification

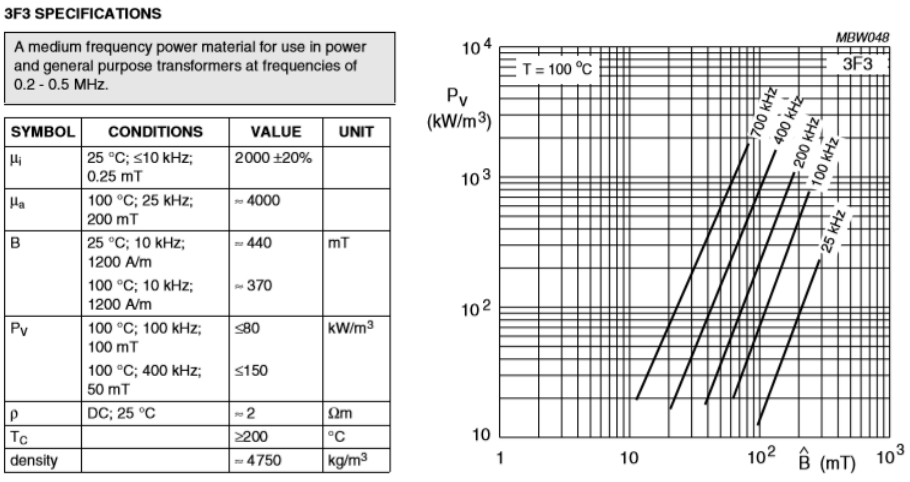
The transformer specifications can be deducted from the specifications of the converter which are shown in Table 4.1.

Tabel 4.1 Converter specifications

Parameter	**Notation**	**Module**
Output power	Po	1.6kW
Input voltage	Vin	260 V– 420 V
Output voltage	Vo	12 V– 16 V
Output current	Io	115 A
Magnetizing inductance	L_p	100µH
Transformer ratio	Np/Ns	7

4.1.2 Selection of magnetic core material

Since the switching frequency of the converter is 200kHz, it is necessary to use a high frequency ferrite material. For this application, the 3F3 material from the Ferroxcube manufacturer was selected [33]. The datasheet of this material is presented in Fig. 4.2.



3F3 SPECIFICATIONS

A medium frequency power material for use in power and general purpose transformers at frequencies of 0.2 - 0.5 MHz.

SYMBOL	CONDITIONS	VALUE	UNIT
μ_i	25 °C; ≤10 kHz; 0.25 mT	2000 ±20%	
μ_a	100 °C; 25 kHz; 200 mT	≈ 4000	
B	25 °C; 10 kHz; 1200 A/m	≈ 440	mT
	100 °C; 10 kHz; 1200 A/m	≈ 370	
P_V	100 °C; 100 kHz; 100 mT	≤80	kW/m³
	100 °C; 400 kHz; 50 mT	≤150	
ρ	DC; 25 °C	≈ 2	Ωm
T_C		≥200	°C
density		≈ 4750	kg/m³

Fig. 4.2 Datasheet of the 3F3 magnetic material.

The 3F3 material has a saturation flux density of 370mT and the Curie temperature of 200°C and is suited for the operating frequency range 200kHz – 500kHz. The specific losses are ≈230kW/m^3 at a core flux density of 100mT.

4.1.3 Selection of the size and model of the magnetic core

In order to find the optimal solution, three planar core models are proposed to be analyzed using numerical simulation. Constructive models and their dimensions are presented in Table 4.2 [35].

Tabel 4.2 Models of planar cores proposed for the power transformer

Core model	Core area	Core volume	Bobbin window
E43/10/28	229 mm^2	13.9 cm^3	13.3 mm
ER51/10/38	314 mm^2	25.8 cm^3	10.9 mm
E58/11/38	308 mm^2	24.6 cm^3	21.1 mm

4.1.4 Numerical simulation of the power transformer

In order to perform numerical simulation, it is necessary first to define the conditions and simulation models for each proposed core variant. It is considered that all three constructive transformer variants have the same turns ratio (N = 7) and are built in planar technology on a six-layer PCB (printed-circuit-board).

For FEM numerical simulation, the Ansys Maxwell software from the Ansys Electromagnetics suite will be used. For the analysis, an adaptive mesh will be used. The adaptive mesh means that the mesh density is high in areas where the distribution of the magnetic field (e.g. airgap) is non-uniform and lower density in areas where the magnetic field is uniform. This type of mesh allows to significantly reduce the simulation time without sacrificing the accuracy of the results. For all FEM simulations performed, a maximum error of 2% was imposed.

Simulation models of the transformer

The FEM simulation models of the three core variants for the transformer are shown in Fig. 4.3.

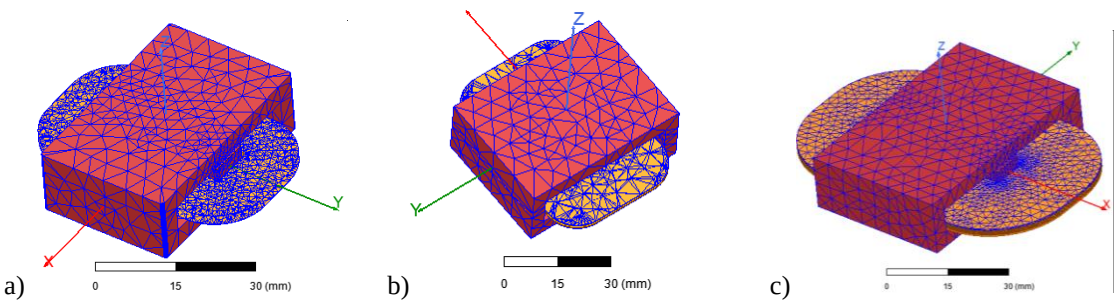


Fig. 4.3 FEM simulation models for the power transformer (E43, ER51 and E58).

The windings connections and distribution across PCB layers is presented in Fig. 4.4.

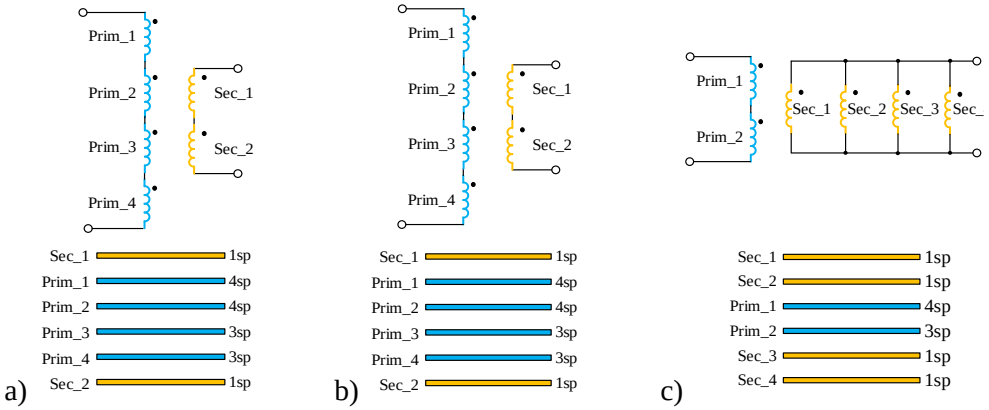


Fig. 4.4 Windings connection and distribution over PCB layers.

Eddy currents simulation

The Eddy currents simulation assume sinusoidal excitations for current and voltage accross transformer windings. This provides important information about transformer, such as winding inductances (L_p, L_{sec}), leakage inductance (L_k), maximum flux density (B_{max}), coupling factor (K), ac winding resistances (R_{prim}, R_{sec}), and power losses in the core and windings. Table 4.3 show the transformer parameters and the values of the losses from the FEM analysis for the three core variants proposed.

Table 4.3 Transformer parameters obtained from Eddy simulation

a)

	Freq [kHz]	Lp [uH]	Lsec [uH]	Lk [uH]	Rprim [mOhm]	Rsec [mOhm]	K	Bmax [tesla]
1	10.00	106.44	2.16	0.83	214.71	5.76	0.99633	1.532
2	100.00	104.37	2.12	0.72	521.28	11.48	0.99675	0.157
3	200.00	104.28	2.12	0.71	581.54	12.67	0.99678	0.078

b)

	Freq [kHz]	Lp [uH]	Lsec [uH]	Lk [nH]	Rprim [mOhm]	Rsec [mOhm]	K	Bmax [mTesla]
1	10.00	102.74	2.09	168.05	70.77	0.71	0.99918	2432.47
2	100.00	102.65	2.09	124.39	113.74	1.74	0.99939	244.10
3	200.00	102.79	2.09	113.81	134.54	2.19	0.99945	122.07

c)

	Freq [kHz]	Lp [uH]	Lsec [uH]	Lk [nH]	Rprim [mOhm]	Rsec [mOhm]	K
1	10.00	101.35	2.06	420.39	157.47	2.17	0.99792
2	100.00	100.75	2.05	407.65	241.50	3.69	0.99797
3	200.00	100.74	2.05	403.82	279.65	4.30	0.99799

Fig. 4.4 shows the distribution of the magnetic field in the core together with the distribution of the current density in the windings. According to results, the flux density in the magnetic core E43 is around 80mT, in the case of ER51 is 122mT and for E58 is 60mT. The average current density in the windings for the E43 core is around 60A/mm^2, for ER51 is 9A/mm^2 and in the case of the E58 configuration it is 8A/mm^2.

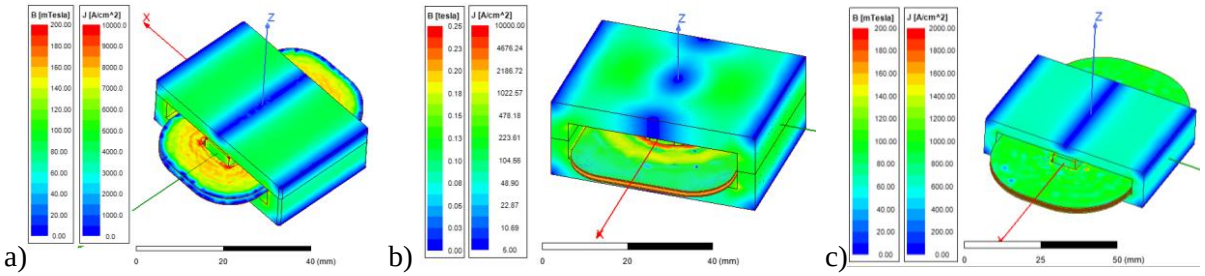


Fig. 4.4 Distribution of magnetic field and current density.

Transient simulation of final transformer version (E58)

In order to obtain a clear picture about the transformer performance, a transient simulation coupled with FEM model will be performed according to the electrical schematic from Fig. 4.5. The simulation results are presented in Fig. 4.6 and the distribution of power losses over transformer components are shown in Fig. 4.7.

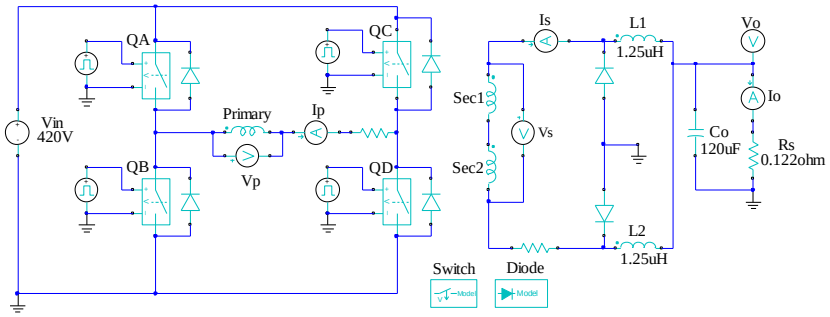


Fig. 4.5 Transient simulation schematic for E58 transformer configuration.

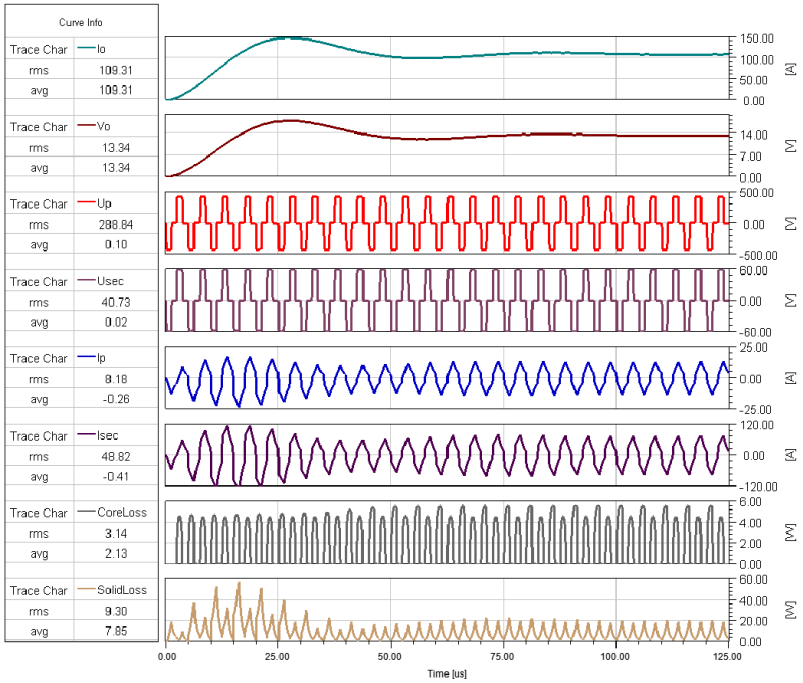


Fig. 4.6 Results of transient simulation for E58 transformer configuration.

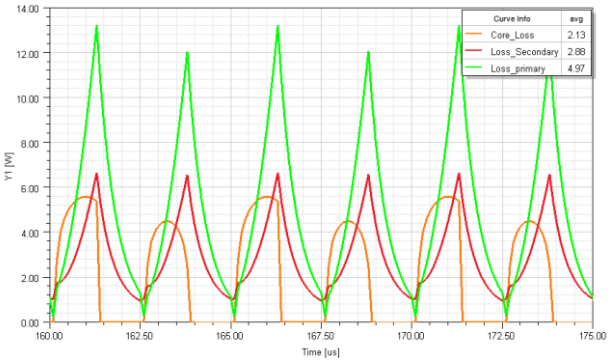
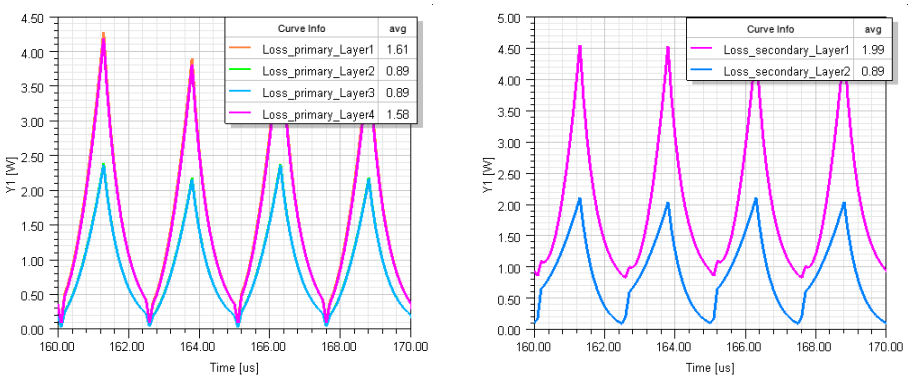


Fig. 4.7 Power losses distribution across E58 transformer.

According to the results of Fig. 4.6 and Fig. 4.7, the losses averaged over the time interval [160us, 175us] are:

- Losses in primary winding = 4.97 W;
- Losses in secondary winding = 2.88 W;
- Core losses = 2.13 W;
- Total losses = 9.98 W.

Additionally, the losses distribution over the PCB layers can extracted in order to check for losses concentrations in windings structure. The distribution of losses per layer for the primary and secondary windings is presented in Fig. 4.8.



a) Primary winding losses distribution b) Secondary winding losses distribution

Fig. 4.8 Losses distribution over the PCB layers of the E58 transformer configuration.

According to the results from Fig. 4.8, the power losses in layers one and four of the primary winding are greater than ones from other two layers. This was expected because the number of turns per layer is larger. In the case of secondary winding, a similar difference is observed between the two layers. This difference occurs because the top layer is closer to the air-gap where the leakage magnetic field generates losses through Eddy currents. The Table 4.4 show the summary of losses for the three variants of cores analyzed. According to the results, the E58 core configuration is optimal due to the low core and windings losses. Given that the E58 variant offers the best performance, this configuration is selected for the design of the power transformer.

Tabel 4.4 Losses summary for transformer core configuration

Configuration	Core losses	Winding losses	Total
E43/10/28	2.18 W	19.55 W	21.73 W
ER51/10/38	8.21 W	4.57 W	12.78 W
E58/11/38	2.13 W	7.85 W	9.98 W

4.2 Leakage inductance L_k

In this section, the material, core model and the air-gap will be selected and the losses will be calculated for each proposed configuration using FEM analysis.

4.2.1 Leakage inductance speficication

Based on the results from the previous sections, the specifications leakage inductance are:

- L_k = 2.5 µH, I_{Lmax} = 15A, Fsw = 200kHz, B_{max} = 125mT.

where, I_{Lmax} is the peak inductor current.

4.2.2 Core material selection

As the operating conditions are similar to those of the power transformer, the same type of material will be chosen for the magnetic core (3F3).

4.2.3 Selection of the size and model of the magnetic core

In order to select the optimal configuration for the leakage inductance core, two planar core models will be evaluated. They are shown in Table 4.5.

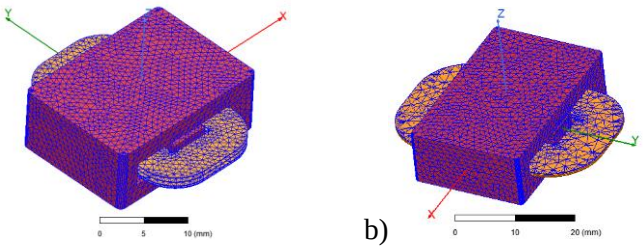
Table 4.5 Models of planar cores proposed for leakage inductance.

Core model	Core area	Core volume	bobbin window
E22/6/16	78.5 mm^2	2.4 cm^3	5.9 mm
E32/6/20	130 mm^2	4.56 cm^3	9.2 mm

4.2.4 FEM analysis of leakage inductor

Definition of simulation models

FEM simulation models of leakage inductor are shown in Fig. 4.9.



a) b)

Fig. 4.9 FEM simulation models leakage inductor.

Eddy simulation

Table 4.6 gives the main inductor parameters for both variants obtained from FEM analysis. The simulation was performed at several air-gap values in order to choose the optimal size.

Table 4.6 The main parameters of the leakage inductor as function of the air-gap.

a) E22

	$gap [um]	L [uH]	RL [mOhm]	CoreLoss [W]	SolidLoss [W]	Total Loss [W]	Imax [A]	Bmax [mTesla]
1	700.00	3.22	50.78	1.09	5.71	6.80	15.00	139.98
2	750.00	3.04	51.69	0.96	5.82	6.77	15.00	131.54
3	800.00	2.88	52.42	0.85	5.90	6.75	15.00	124.98
4	850.00	2.73	53.55	0.76	6.02	6.78	15.00	120.15
5	900.00	2.60	54.22	0.68	6.10	6.78	15.00	113.93
6	950.00	2.48	55.37	0.61	6.23	6.84	15.00	109.30

b) E32

	$gap [um]	L [uH]	RL [mOhm]	CoreLoss [W]	SolidLoss [W]	Total Loss [W]	Imax [A]	Bmax [mTesla]
1	650.00	3.06	21.19	1.39	2.38	3.77	15.00	104.41
2	700.00	2.88	21.26	1.21	2.39	3.60	15.00	98.43
3	750.00	2.72	21.53	1.07	2.42	3.49	15.00	93.10
4	800.00	2.58	21.90	0.95	2.46	3.42	15.00	88.24
5	850.00	2.46	21.99	0.85	2.47	3.33	15.00	84.34
6	900.00	2.35	22.14	0.77	2.49	3.26	15.00	80.14

According to Table 4.6, in the case of E22 core the total losses of the inductor are approximately constant for the air-gap value in the range [0.8mm – 0.95mm]. Since for the converter a higher leakage inductance is beneficial, the value of the air-gap equal to 0.85mm will be chosen for performing the transient simulation. At this value, the inductance is equal to 2.73µH and the total losses are 6.78W. In the case of E32 configuration, the total losses are constant for the air-gap range of [0.7mm – 0.8mm]. Therefore, an air-gap of 0.75mm will be selected. At this value the inductance is 2.72µH and the total losses are 3.49W.

The Fig. 4.10 shows the distribution flux density in the core and the current density in the windings.

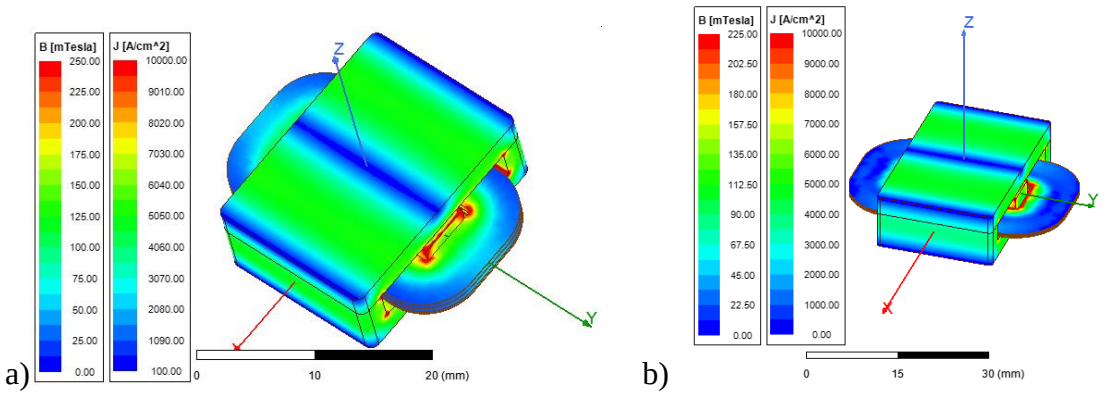


Fig. 4.17 Magnetic field and current density distribution for leakage inductor (E22 and E32).

According to the results, for E22 configuration the flux density in the magnetic core is 120mT and the average current density in the windings is 15A/mm^2. In the case of the E32 the flux density is 90mT and the average current density in the windings is 10A/mm^2.

Transient simulation

The results of the transient simulation coupled with FEM analysis of leakage inductor for both core variants are shown in Fig. 4.18.

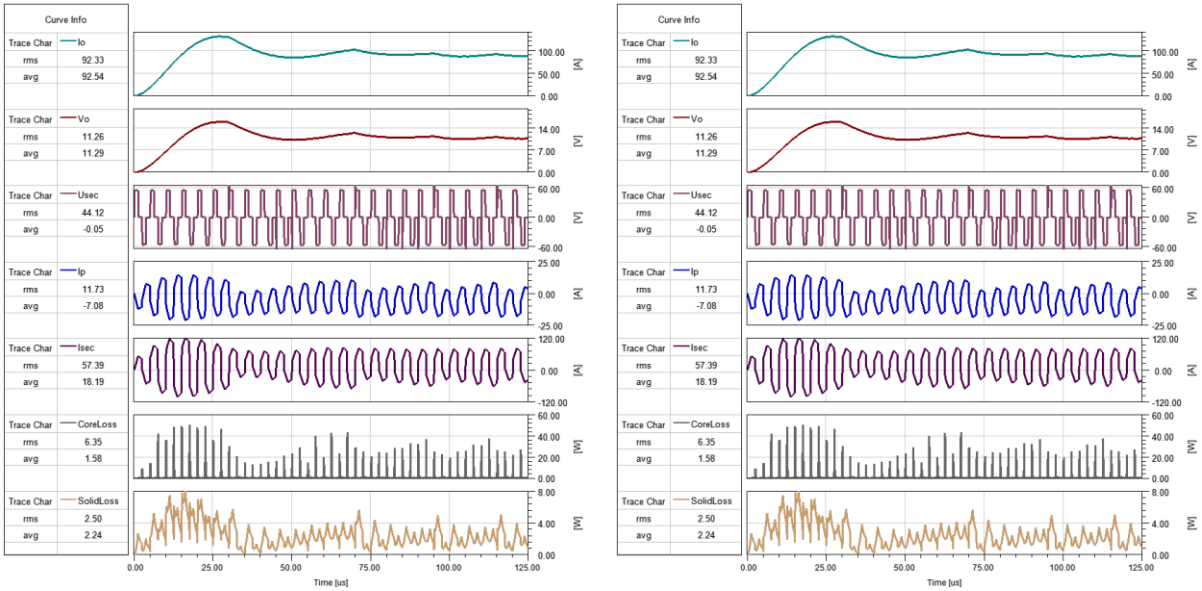


Fig. 4.18 Main converter waveforms from transient simulation of leakage inductor.

According to the results, the averaged power losses over the range [160us, 175us] are:

- Core losses E22/E32 = 1.17W/1.58 W;
- Windings losses E22/32 = 5.32W/2.24 W;
- Total losses E22/E32 = 6.49W/3.82 W.

Studying the losses summary show that the total losses are significantly lower for the E32 configuration compared to the E22. Although both configurations can be used, the selected core variant is E22 due to the limitation of the PCB space.

4.3 Output inductor Lo

The output inductor together with the output capacitor realize the filtration of the output voltage of the DC-DC converter.

4.3.1 Output inductor specifications

Based on the results in the chapter two, the output inductor specifications are the following: L = 1.2 µH, I_{Lmax}= 80A, Fsw = 200kHz, B_{max} = 380mT.

4.3.2 Selection of magnetic core material

Since the output inductor has a small ac flux swing, a material that has a higher saturation flux density can be selected, such as material 3C90 [34].

4.3.3 Selection of the size and model of the magnetic core

For this inductor, a planar core E32/6/20 was chosen. It has a bobbin window width equal to 9.2 mm and an effective cross section area of 130 mm^2.

4.3.4 FEM analysis of output inductor

Definition of the simulation model

The FEM simulation model of the E32/6/20 core output inductor together with the mesh are shown in Fig. 4.19.

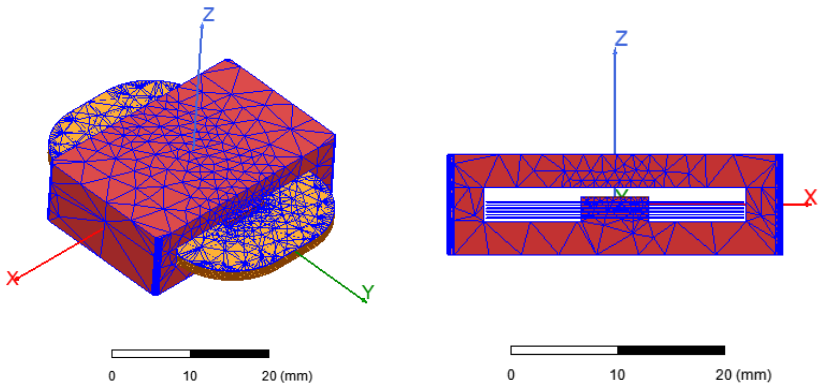


Fig. 4.19 FEM analysis model of the E32/6/20 core output inductor.

Magnetostatic simulation

Due to the significant DC current bias, the FEM magnetostatic analysis will be performed. In Fig. 4.20 the graph of peak flux density as a function of core air-gap at I_{Lmax} = 80A is presented.

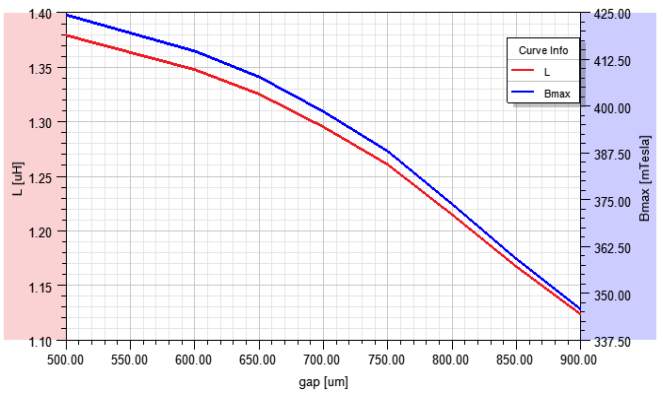


Fig. 4.20 Inductance L and flux density B_{max} as function of the core air-gap.

In order to limit the maximum flux density to a reasonable value, an air-gap of 0.85 mm will be selected. At this value of the air-gap the inductance is 1.16 μH.

Transient simulation

The results of the transient simulation of the inductor are presented in Fig. 4.21.

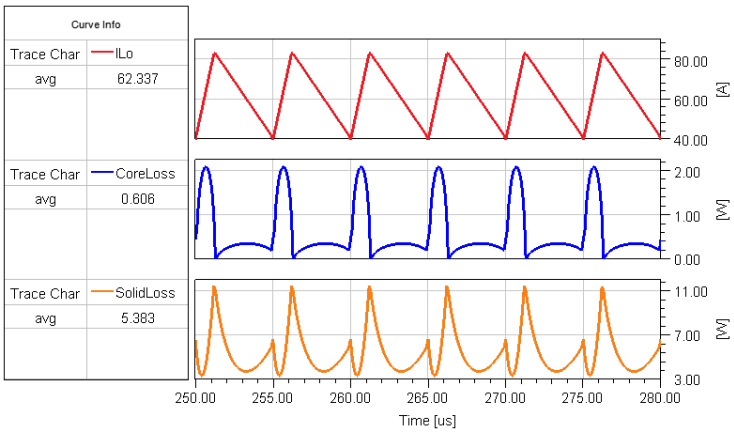


Fig. 4.21 Inductor waveforms during transient simulation.

The distribution of losses by layer is highlighted in Fig. 4.22. Analyzing the results, a good balance of the dissipated power over the PCB layers is observed.

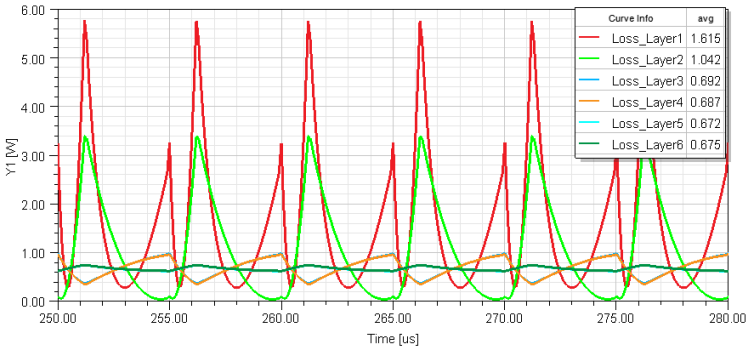


Fig. 4.22 Distribution of the inductor windings losses per PCB layer.

4.4 Conclusions

In this chapter, the main scope was the optimization and selection of power magnetics components for the converter by using the FEM analysis.

CAP. 5 DC-DC converter parallel operation

In this chapter, the main methods of current balancing are investigated and a new balancing method will be proposed for the full-bridge phase shifted converters. In order to validate the concept, the new current balancing method is analyzed using simulations and experimental verification on a functional prototype (see Chapter 6).

5.1 Methods of parallel connection of DC-DC converters

Connecting the power converters in parallel has many advantages, but it also poses an important difficulty. This consists in ensuring equal current sharing between converters in both static and dynamic mode.

5.1.1 Current limit method

This method involves the use of converters connected in parallel in the current limit mode. In this way, when one of the converters delivers the maximum current that it can provide, its output voltage decreases and the second converter begins to deliver current. When the second converter reaches to its current limit, the third one will start to deliver current. This method does not always ensure an equal sharing of the output currents of the converters unless they all operate in current limitation mode.

5.1.2 Droop method

This method of parallel connection involves the design of converters with a finite output resistance so that the output voltage will decrease linearly with the increase in current. In this way, if the converters are initially adjusted individually for an operating point, they will contribute equally to the total output current over the entire operating range of the converter. Although this solution is simple to implement, it offers a low output voltage accuracy due to high converters output resistance.

5.1.3 Common feedback method

This method involves the use of a single feedback loop for all modules connected in parallel to stabilize the output voltage. In this mode, the control block (regulator) will provide the same duty-cycle ratio to all modules connected in parallel. If the power modules are identical built, their output currents will be equal and the total current will be delivered in the load. In practice, it is almost impossible to achieve this objective because the tolerances of the components and production process.

5.1.4 Average current mode method

This method consists of implementing a current regulator for each module connected in parallel. These regulators communicate the current information with each other and adjust the individual duty-cycle so that the average output currents of the converters are equal. This method provides the best balancing for output currents of the modules connected in parallel in static operation, but also redundancy in case of failure of a module. In dynamic mode, however, because the regulators operate with the average current value, they are not fast enough to equalize the converters current during steep load changes.

5.1.5 Peak current mode method

This method involves stabilizing the output voltage of the converter by controlling the peak value of the current in the output inductors. Given that the regulator imposes the same current reference for all modules connected in parallel, the current sharing between modules is very precise in both static and dynamic mode.

The main advantages of the peak current mode control are:

- precise balancing of the output currents of the modules in static and dynamic mode;
- elimination of the DC component at the transformer terminals that allows the elimination of the DC blocking capacitor;
- intrinsic overcurrent protection;
- uniform power losses on power semiconductor devices;
- very fast dynamic response;
- does not require a current sensor at the output, the regulator can be implemented with a current transformer on the power path of the primary circuit.

Due to the advantages mentioned above, especially for the precise current sharing and the possibility of removing the DC blocking capacitor and current shunts, this concept will be selected for the parallel connection of two DC-DC full-bridge phase shifted converters with 1.6kW nominal power.

5.2 Simulation of the peak current mode control for one module

The power electrical schematic is shown in Fig. 5.1 and consists of an input filter (L_f, C_{in}), current transformer (CT), primary bridge (QA,QB,QC,QD), power transformer (T1), synchronous rectifier (QE, QF) and output filter (L_{o1}, L_{o2}, C_{o1}).

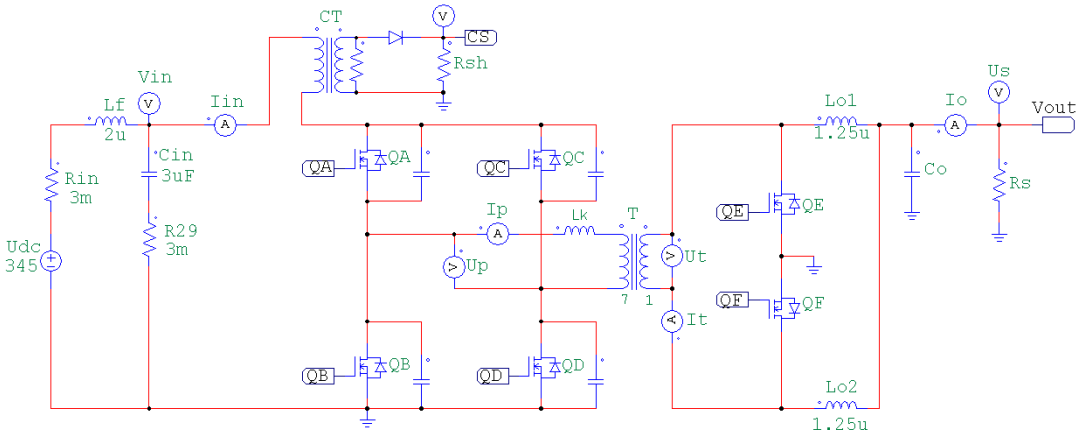


Fig. 5.1 Converter simulation schematic in PSIM software.

The electrical schematic of the control circuit is shown in Fig. 5.2. It consists in four main blocks. The output voltage regulator, ramp generator, clock signal generator and PWM module.

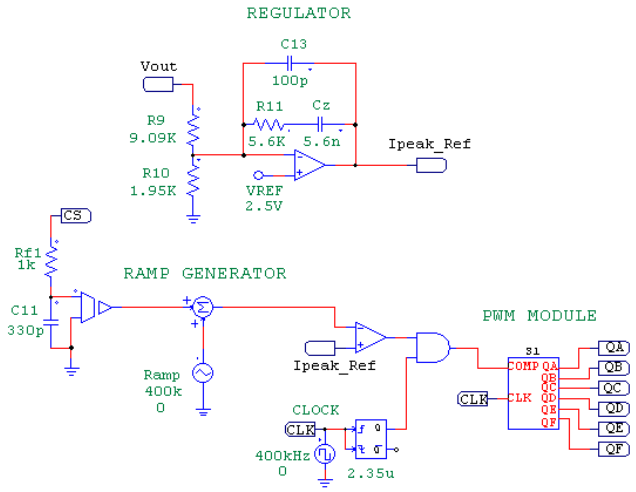


Fig. 5.2 Peak current mode control schematic in PSIM software.

5.2.1 Simulation of the peak current mode control in static mode

The results of the simulation are shown in Fig. 5.3. As can be seen, the Up voltage across primary winding of the power transformer is formed by overlap of the conduction interval of two power switches from diagonals of the primary bridge QA, QD and QB, QC. The duty-cycle is determined by the intersection of the I_{peak_Ref} reference given by the voltage regulator and the peak value of the input current given by the CT current transformer and the shunt resistor R_{sh}.

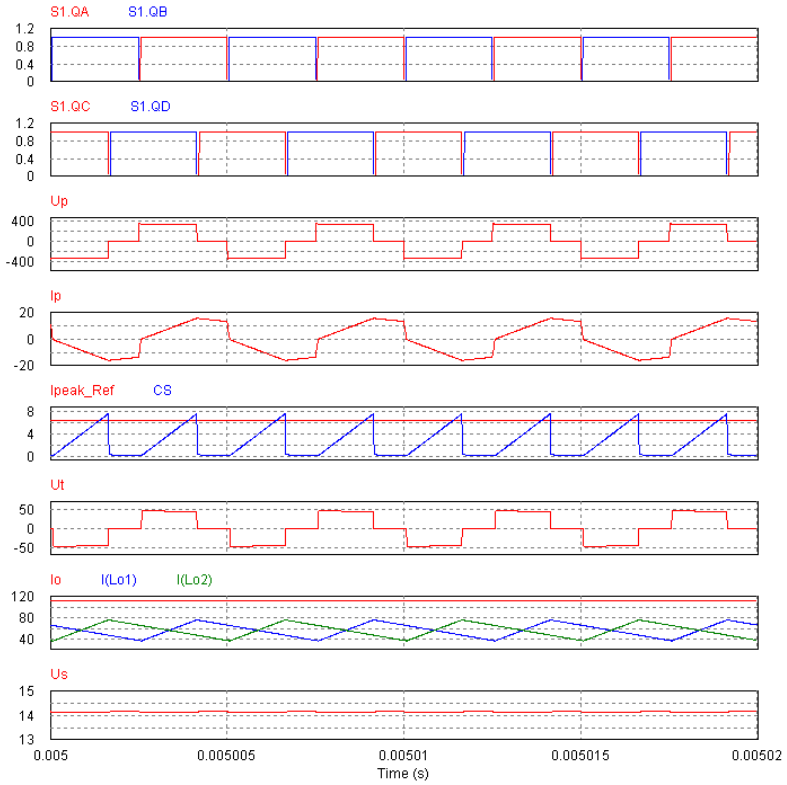


Fig. 5.3 Simulation of a single module in static mode la Us = 14V, Io = 115A.

The currents of the inductors are noted with I_{Lo1} and I_{Lo2}, the output current is represented by Io and the output voltage is noted with Us. For this particular case, nominal operating conditions were considered: U_{dc} = 345V, Us = 14V, Io= 115A.

Analyzing the results, it can be observed that the peak current mode control works properly on this type of topology. In this way, the amplitude of the peak input current is controlled on both polarities, this guarantees the cancellation of the DC component in the primary of the power transformer.

5.2.2 Simulation of peak current mode control in dynamic mode

The results of the simulation in dynamic mode are shown in Fig. 5.4. The graph reveals the dynamic behavior of the converter in the case of a load transition from 50% to 100% of the rated current. This means a current step from 60A to 115A.

As can be seen from the waveforms in Fig. 5.4, the current reference ("I_{peak_Ref}") force the peak value of the input current be the same on both polarities. During current transitions, the output voltage varies by a maximum of ±2V.

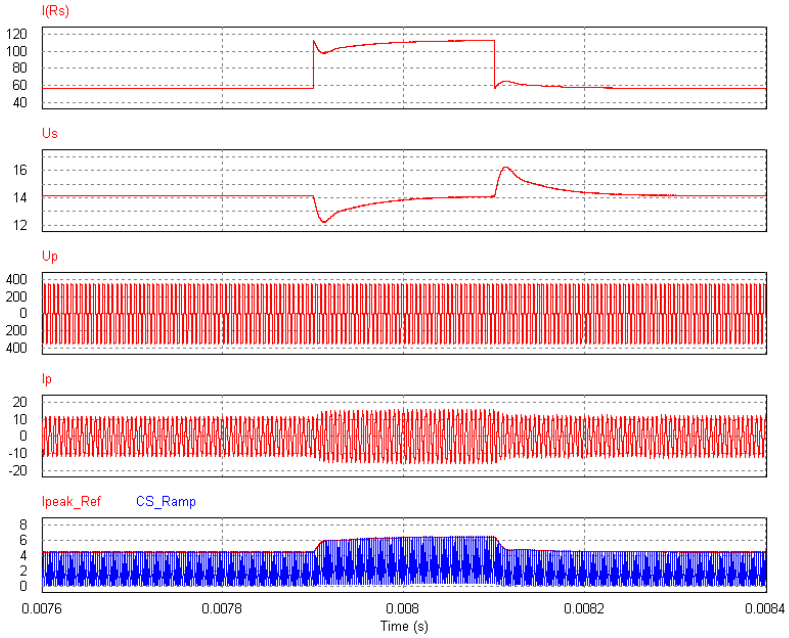


Fig. 5.4 Dynamic response for load step from 50% to 100% of nominal current.

5.3 Simulation of the peak current mode control for two DC-DC modules in parallel operation

For the simulation, a second module will be added in the schematic and connected in parallel with the first module. By using the same peak current reference for parallel connected modules, the current sharing between modules is ensured. The Fig. 5.5 shows the power electrical schematic used to simulate the two DC-DC converters in parallel configuration.

The implementation of the peak current mode control for DC-DC parallel operation can be done in two ways. The first possibility is to use the same clock signal for all modules connected in parallel (synchronous operation). The second possibility involves the use of two clock signals with a phase delay (Interleaved operation). In the interleaved operating mode the PWM clocks have a phase offset of 90°.

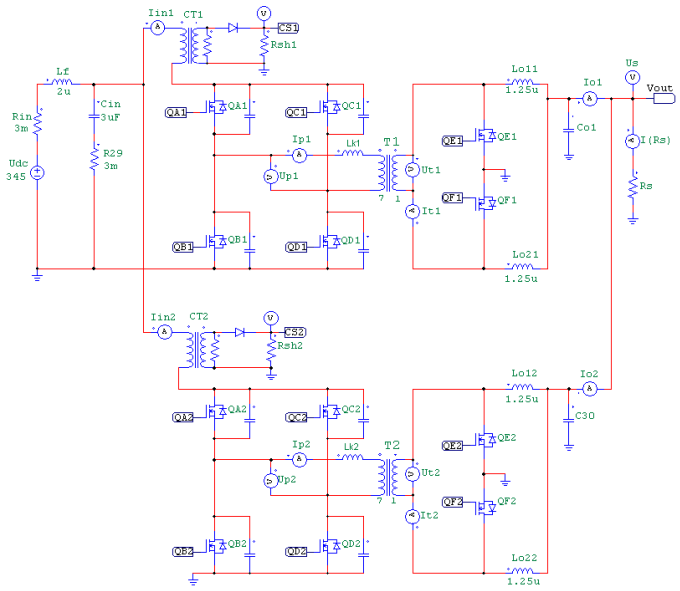


Fig. 5.5 Schema electrică de putere a două convertoare DC-DC în punte conectate în paralel.

5.3.1 Simulation of two DC-DC modules operating in parallel with synchronous PWM clocks

Synchronous operation requires that the clock signals of the two PWM modules of the DC-DC converters connected in parallel are in phase.

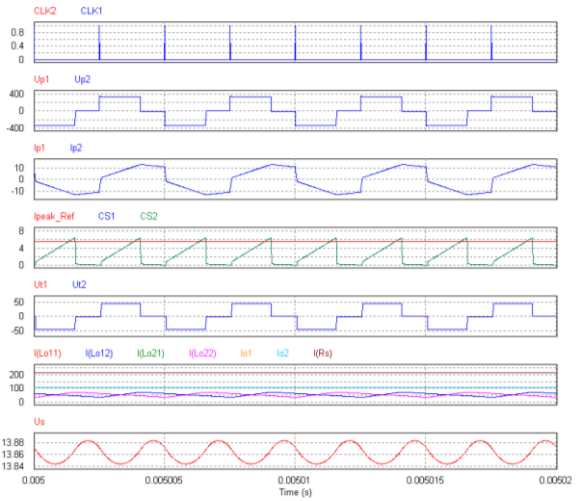


Fig. 5.6 The waveforms of the converter consisting of two modules connected in parallel with the synchronous PWM clock signal at rated load, Us = 14V, Io = 230A.

In Fig. 5.6 CLK1, CLK2 are the clock signals of each module, U_{p1}, U_{p2} are the voltages across primary windings of the power transformers, CS1, CS2 are the signals from the current transformers (CT1, CT2), I_{peak_Ref} is the common current reference provided by the voltage regulator, IRs is the total output current and Us is the voltage on the load. Although it is simpler to implement, the synchronous operation conducts to significant ripple of currents through the input/output filter capacitors.

5.3.2 Simulation of two DC-DC modules connected in parallel with interleaved operation in static mode

Interleaved operation requires that the clock signals of the two DC-DC modules connected in parallel are delayed in phase by 90°. The simulation results for the interleaved operation are presented in Fig. 5.7.

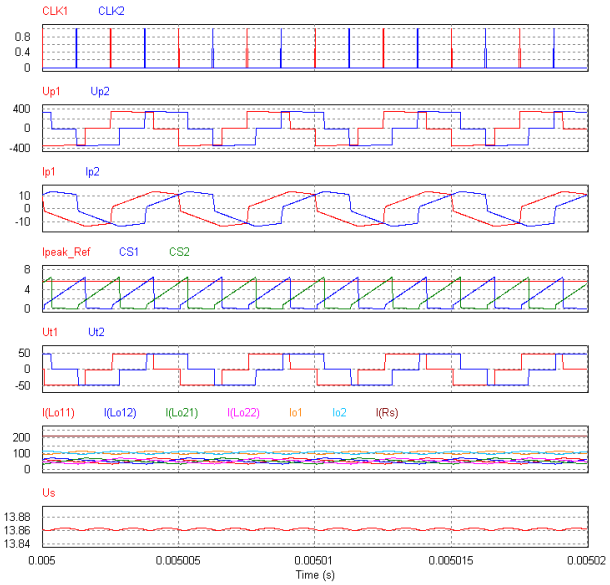


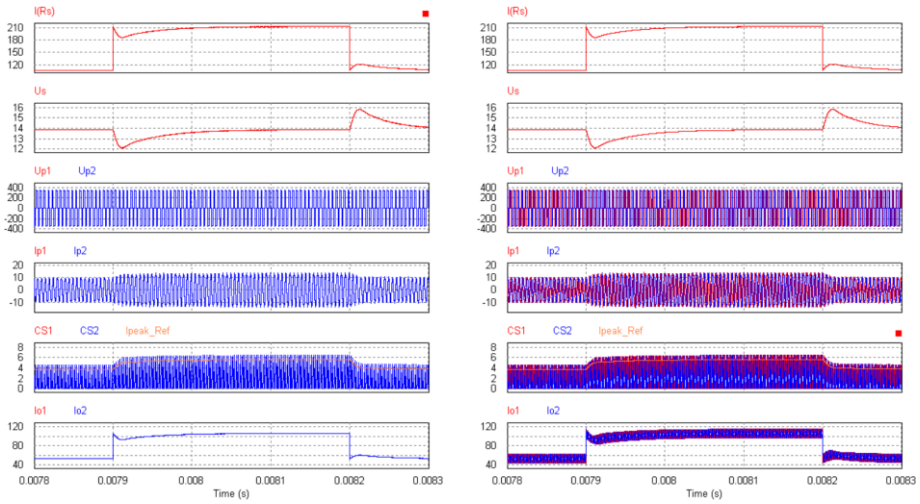
Fig. 5.7 The main waveforms of the converter with two modules connected in parallel in "interleaved" mode at rated load, Us = 14V, Io = 230A.

5.3.3 Simulation of two modules connected in parallel in dynamic mode

The Fig. 5.8 shows the simulation results of dynamic behavior for both operating modes (synchronous and interleaved). After analyzing the dynamic response, it can be seen that there are no visible differences between synchronous and interleaved control modes, both of have the same response time and the same amplitude of the voltage drop/increase during the transitions.

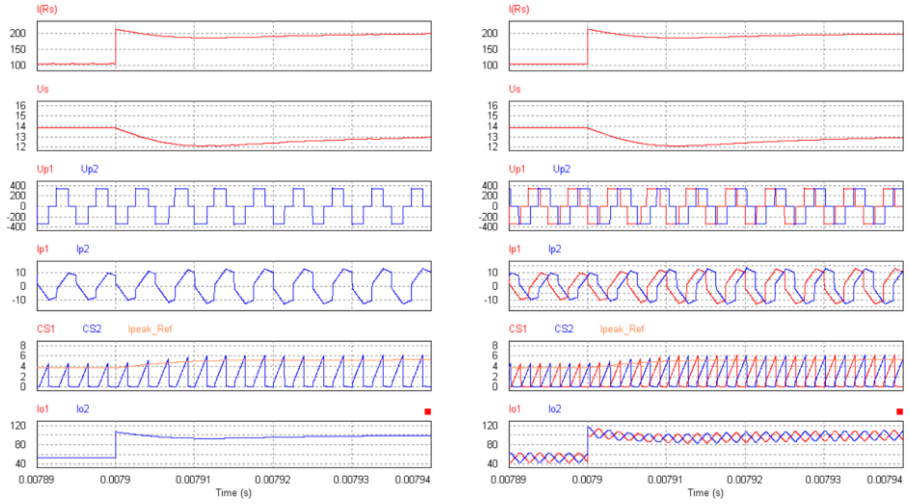
In order to inspect in detail the current sharing during load step, the current transitions were extracted and they can be viewed in Fig. 5.10. By analyzing the results, one can see a very good current sharing between the output currents of the two modules during the transitions for both control methods. In the case of the interleaved mode, some current ripple is observed on the output currents of each module (I_{o1}, I_{o2}). They occur due to the phase shift between the

PWM clocks of the two modules. Since the ripples are out of phase (180°), they cancel each other at the connection point and are not visible in the waveform of the final output current (IRs).



a) Synchronous operation b) Interleaved operation

Fig. 5.9 Dynamic response of the converter working with two modules in parallel at an output current step from 115A to 230A.



a) Synchronous operation b) Interleaved operation

Fig. 5.10 Dynamic converter response during positive load transition.

5.4 Conclusions

In this chapter, the main current sharing methods for DC-DC converters connected in parallel were analyzed. The goal was to find the optimal solution for parallel operation of two full-bridge phase shifted converters. According to simulation results, the peak current mode control proved to be the optimal solution in terms of complexity and performance. The experimental verification of the peak current mode control concept as well the parallel operation of two modules are presented in Chapter 6 of this thesis.

CAP. 6 Prototype realization

In order for the converter application to be implemented in practice, several additional blocks must be added to the power electrical schematic such as: Microcontroller (µC), voltage regulator, protection circuits, driver circuits, communication interface and filters.

These blocks ensure the proper operation of the converter, communication with external equipment and protection in case of short circuit at the output, overload, overvoltage and overtemperature. The protection circuits are necessary to prevent events that could generate a hazard situation in the car such as a major failure or even fire.

6.1 Converter block diagram

The block diagram of the converter containing the two DC-DC modules connected in parallel with the additional blocks is shown in Fig. 6.1.

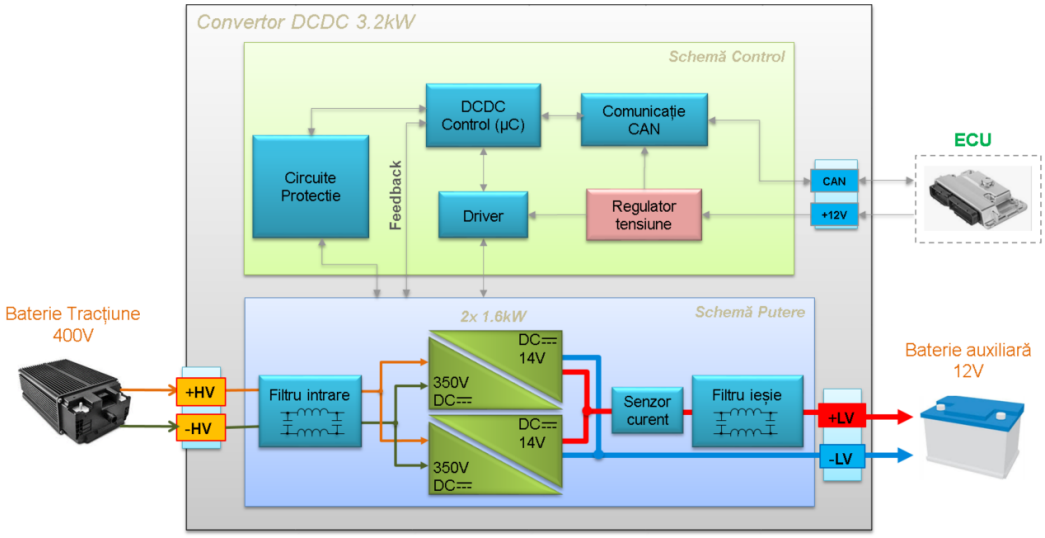


Fig. 6.1 The block diagram of the converter composed of two modules connected in parallel.

6.2 Prototype description

In Fig. 6.2, a picture of the prototype of the converter composed of two modules of 1.6kW connected in parallel is shown. For easier understanding, the converter has been divided into sections as follows:

- Input voltage terminals (Vin);
- Primary side modules 1 and 2;
- T1,T2 power transformers;
- Control circuits together with driver and protection modules;
- Rectifier modules 1 and 2;
- L1, L2 output inductors;
- Converter output terminals (Us).

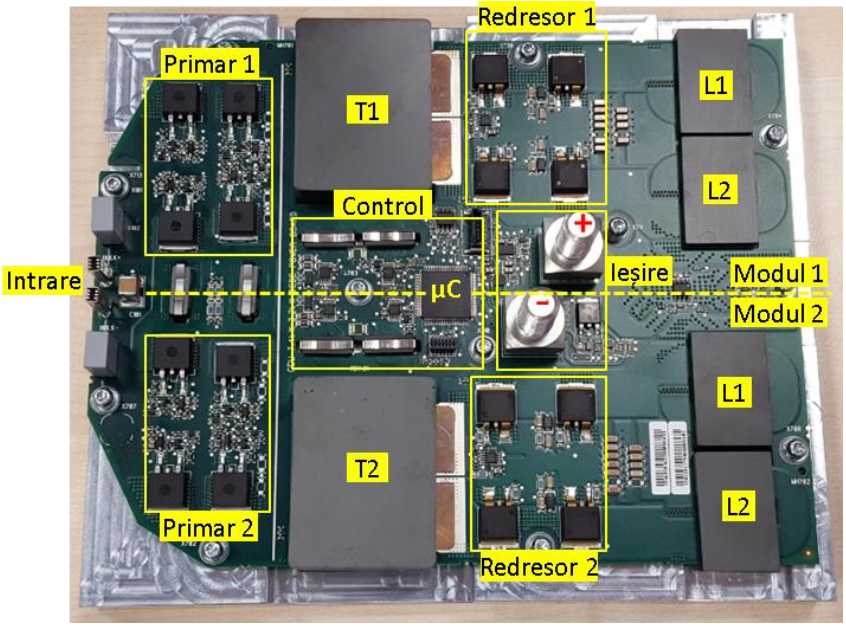


Fig. 6.2 Block diagram of the prototype.

As can be seen, both DC-DC modules are built symmetrically on the same PCB on a small volume (19.5cm x 15.5cm x 4.5cm). The small size is mainly due to the use of planar technology to make magnetic components and cooling mode. The cooling of the power components is done directly through the PCB with the help of an aluminum heatsink and a thermal interface material with electrical insulator properties.

6.3 Waveform measurements and parallel operation

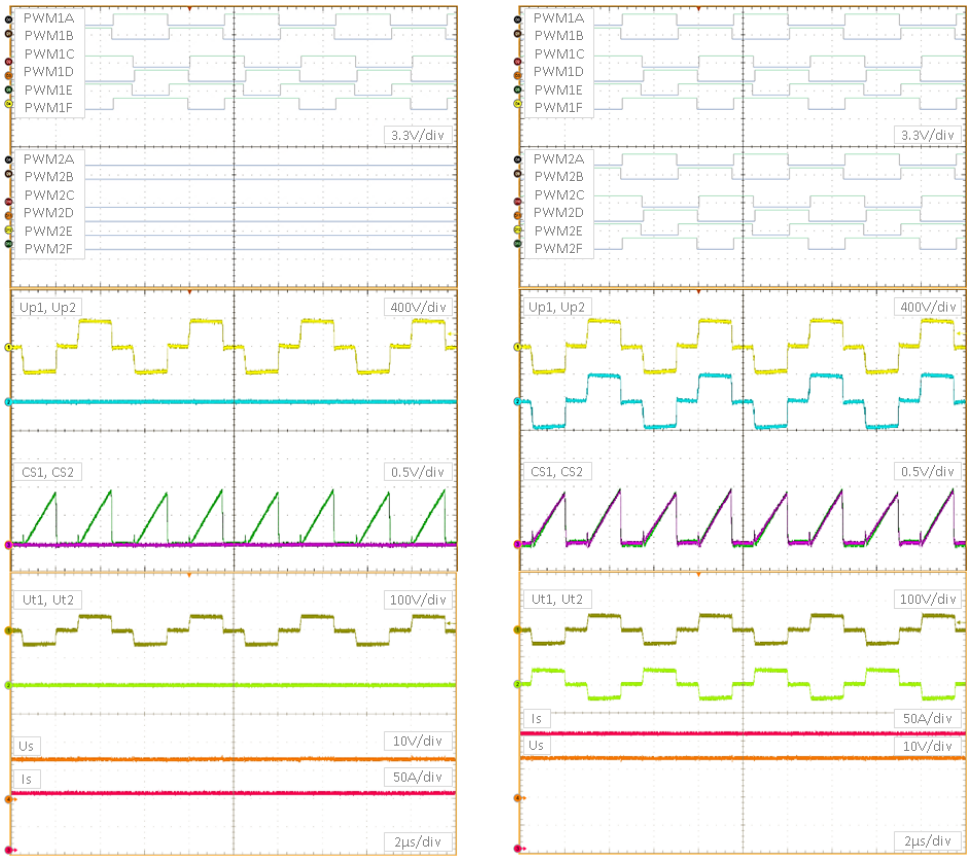
The Fig. 6.3 shows measurements of the main waveforms of the converter for two operating points. In Fig. 6.2a the converter operates with a single module at an output current of 100A. In Fig. 6.2b the two modules are both active and operate in parallel having a total output current of 200A. In both cases, the input and output voltages are nominal (Vin = 350V, Us = 14V).

The dynamic converter response to a current step from 100A to 200A can be observed in Fig. 6.4. The results confirm that the method of peak current mode control is effective in regards of current sharing being verified both by simulation and experimentally.

In Fig. 6.3 and Fig. 6.4 the following notations were used for the measured signals:

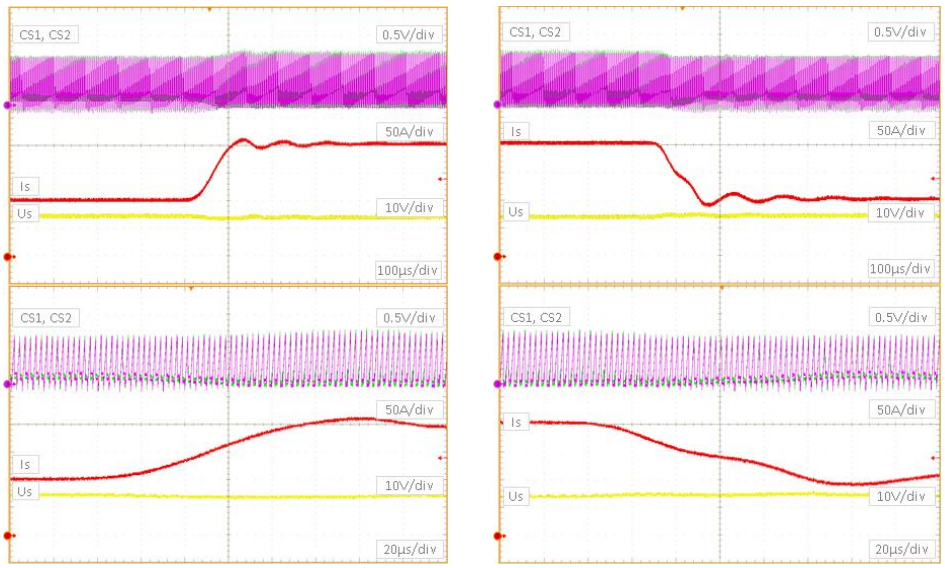
- PWM1A to PWM1D, PWM commands for primary bridge of DC-DC module 1;
- PWM2A la PWM2D, PWM commands for primary bridge of DC-DC module 2;
- PWM1E, PWM1F, PWM commands for rectifier module of DC-DC 1;
- PWM2E, PWM2F, PWM commands for rectifier module of DC-DC 2;
- Up1, Up2, voltages in the primary of power transformers;
- CS1, CS2, signals from current transformers;
- Ut1, Ut2, secondary voltages of power transformers;

- Us, Is the output voltage respectively the output current;
- Is, the total output current of the converter.



a) Operation with one module at Is = 100A b) Operation with two modules at Is = 200A

Fig. 6.3 Converter measured waveforms.



a) 100A→200A transition b) 200A→100A transition

Fig. 6.4 Converter dynamic response to an output load step of 100A.

6.4 Efficiency measurement

In Fig. 6.5 the efficiency of the converter as function of the output current at three input voltages (minimum, nominal, maximum) is shown.

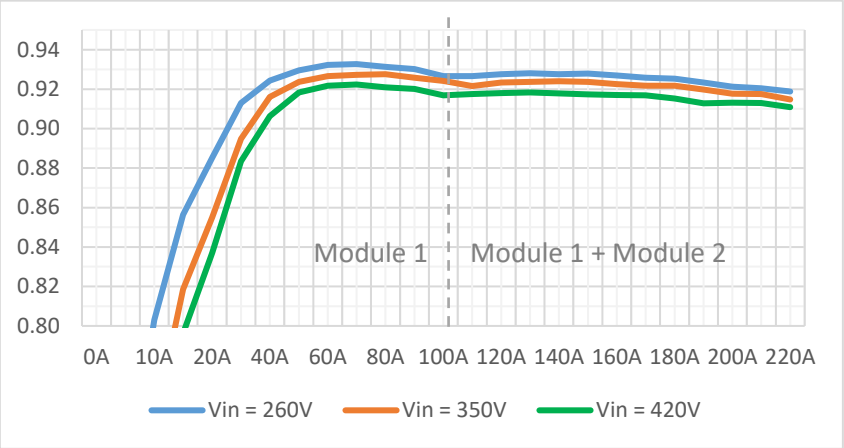


Fig. 6.5 Converter efficiency at different input voltages and output currents.

As can be observed, the converter is operating up to 100A output current with a single module and over 100A the second module is started. At currents >100A, the efficiency of the converter is higher with two modules in parallel than if a single module were used.

By analyzing the results, it can be seen that the peak efficiency of 93.5% is reached at the minimum input voltage and output current of 70A. A new efficiency peak of 93% is also observed when the output load reaches 140A. Above this value, the efficiency begins to drop again to around 91.5% in the worst case condition, at the nominal current and maximum input voltage.

6.5 Thermal measurements on the prototype

Fig. 6.6 shows the infrared thermal map of the converter operating at the nominal conditions (Us = 14V, Is = 230A) with both modules turned on.

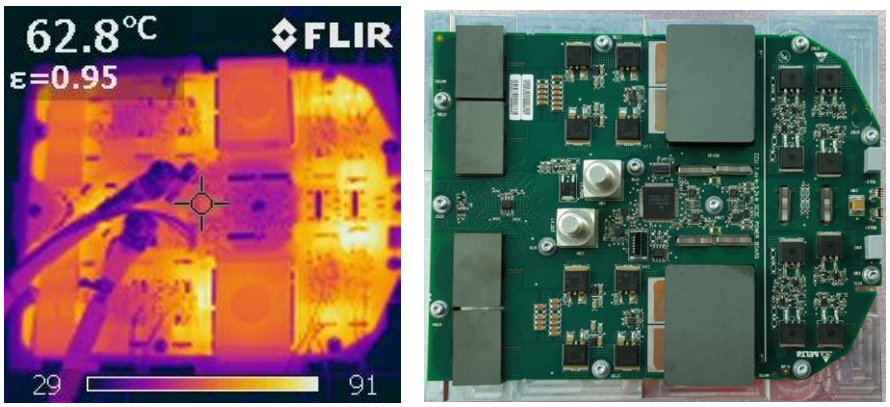


Fig. 6.6 Thermal scanning of the converter at nominal load (Us =14V, Is =230A).

By analyzing the results, a uniform distribution of temperatures is observed on the power sections of the converter. At this operation point, the temperature of the primary stage is slightly higher than in the rest of the converter. The maximum temperature measured on the primary stage is 103°C and is located on one of the power switches of module one. The list of temperatures for each sections of the converter is shown in Table 6.1.

Tabel 6.1 Converter components temperatures.

Component	**Module 1**	**Module 2**
Primary stage	103 °C	97°C
Power transformer core	62°C	62°C
Power transformer windings	96.7°C	93.9°C
Synchronous rectifier	85.3°C	78.6°C
Output inductors	84.1°C	83.2°C
Microcontroller	63°C	
Heatsink	43°C	

General conclusions

In the **first chapter**, the typical specifications of a DC-DC power converter intended to be used in an electric vehicle were presented. Then, the main topologies of DC-DC converters were evaluated and the optimal topology was chosen for each of the two sections of the converter, primary and secondary.

In the **second chapter** a calculation method was presented for the dimensioning of power semiconductors and magnetic components of the full-bridge phase shifted converter.

In the **third chapter**, a calculation method for the converter leakage inductance was presented. The proposed method takes into account the main converter parameters such as: input\output voltages, output current, equivalent series resistances of power switches and magnetization inductance.

In the **fourth chapter**, the design, analysis and optimization of the magnetic power components of the converter with the FEM method was carried out. In the first section, the power transformer was approached and in order to find the optimal solution, three transformer configurations were analyzed: E43, ER51 and E58. In the end, the E58 core configuration proved to be the optimal due to the reduced losses in the magnetic core and windings. In the second section, the leakage inductance was analyzed. In order to find the optimum configuration, two core types were studied: E22 and E32. According to the simulation results, both variants can be used but the E22 variant was selected due to limited PCB space available. In the last section of this chapter, the output inductor of the converter was studied and optimized.

In the **fifth chapter**, the main methods of current balancing for DC-DC converters connected in parallel were evaluated. The main goal was to find the optimal solution for parallel operation of two full-bridge phase shifted converters. The peak current mode control method

has proven to be the optimal solution, offering excellent current sharing and fast dynamic response. In addition, two ways of implementing the peak current mode control were investigated: synchronous and interleaved mode.

In the **sixth chapter**, the implementation of the studied converter was done on physical prototype. In the first section the converter block diagram together with internal blocks was presented. In the second section, the prototype was described and a picture was presented. In the third section, measurements of the main waveforms were presented during operation with one and with two modules connected in parallel. Additionally, an infrared thermal map of the converter operating at nominal conditions and a table with components temperatures was shown. Finally, measurements were done to obtain the efficiency curves versus output current and input voltage.

Original contributions

Personal original contributions can be classified in three categories.

A. Theoretical contributions

1. *The mathematical model of the full-bridge phase shifted converter was derived. The voltage and current stress, power loss on power switches and magnetic components were also evaluated.*
2. *The power semiconductors were selected based on voltage and current stress derived from the mathematical model.*
3. *A new method for calculating and optimizing the value of additional leakage inductance has been proposed. The new method takes into account all converter parameters such as input / output voltages, output current, equivalent circuit series resistances, parasitic capacitances and magnetization inductance.*
4. *For the first time, the peak current mode control method was proposed for current balancing of parallel full-bridge phase shifted converters.*

B. Simulation contributions

1. *The simulation model for converter operation of power schematic together with control and feedback circuits was developed.*
2. *The simulation model for the implementation of the peak current mode control for full-bridge phase shifted converter have been developed.*
3. *The simulation model for two full-bridge phase shifted converters connected in parallel with current balancing by using the peak current mode control with synchronous clock signal and 'interleaved'" was developed.*
4. *Analysis, design and optimization of magnetic power components by using FEM for reducing the power losses.*

5. *Elaboration of the multi-domain coupled simulation model (cosimulation) between the SPICE model of the converter and the FEM models of the magnetic power elements.*

C. Contribution to experimental evaluations

1. *Realization of the converter prototype consisting of two full-bridge phase shifted modules connected in parallel.*
2. *Analysis of current balancing between converters connected in parallel by measuring the input currents of the converters.*
3. *Efficiency measurements from zero to nominal currents at various input voltages.*
4. *Realization of the thermal map of the converter during operation at nominal conditions with the indication of the maximum temperatures on each section.*

Future perspectives

The researches presented during this thesis constitute a starting point and a basis for the design, analysis and optimization of switching converters. Although the thesis has focused on DC-DC power converters intended for use in electric vehicles, the approach presented can be used for any converter topology with any destination.

Analyzing the final results obtained from simulations and measurements on the converter prototype, the following possibilities for development and improvement may be investigated:

- Replacement of the microcontroller with a higher performance one to make it possible to implement the interleaved peak current mode control;
- evaluation of the possibility of coupling the two output inductors on a single core;
- implementation of an ideal diode mode by using existing synchronous rectifier to increase the efficiency at very low load (<10%·In);
- optimization of converter dead-times and magnetization inductance to achieve efficiency targets at maximum input voltage;
- implementation of the digital feedback loop in software;
- comparative analysis of efficiency and cost between the topology used in this paper and the LLC topology.

Bibliography

1. *Tom Randall*, ”Here’s How Electric Cars Will Cause the Next Oil Crisis”, articol online, https://www.bloomberg.com/features/2016-ev-oil-crisis/, pp. 1, 25 Februarie 2016.

2. *Ben Sassi, F. Errahimi, N. Essbai and C. Alaoui*, "V2G and Wireless V2G concepts: State of the Art and Current Challenges, "2019 International Conference on Wireless Technologies, Embedded and Intelligent Systems *(WITS)*, Fez, Morocco, 2019, pp. 1-5.
3. *Steve Mappus*, ”Power Converter Topology Trends”, articol online ”Power Sources Manufacturers Association”, http://www.psma.com, pp. 42-47, Octombrie 2014.
4. *Robert W. Erickson*, ”DC-DC Power Converters”, articol în ”Wiley Encyclopedia of Electrical and Electronics Engineering”, pp. 16-18, Iunie 2007.
5. *Laszlo Balogh*, ”The Current-Doubler Rectifier: An Alternative Rectification Technique For Push-Pull And Bridge Converters”, notă de aplicație Unitrode Slua121 DN-63, pp. 1-3, Decembrie 1994.
6. *Sam Abdel-Rahman*, ”Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier”, notă de aplicație Infineon Technologies North America DN 2013-01, pp. 5-7, Ianuarie 2013.
7. *Steve Mappus*, ”Control Driven Synchronous Rectifiers in Phase Shifted Full Bridge Converters”, notă de aplicație Texas Instruments Slua287, pp. 4-7, Martie 2003.
8. *Sam Abdel-Rahman*, ”Design of Phase Shifted Full-Bridge Converter with Current Doubler Rectifier”, notă de aplicație Infineon Technologies North America DN 2013-01, pp. 5-7, Ianuarie 2013.
9. *Michael O'Loughlin*, “UCC28950 600-W Phase-Shifted Full-Bridge Application Report SLUA560B”, Octombrie 2010, pp. 3-14.
10. *Laszlo Balogh*, ”The Current-Doubler Rectifier: An Alternative Rectification Technique For Push-Pull and Bridge Converters”, notă de aplicație Unitrode Slua121 DN-63, pp. 1-3, Decembrie 1994.
11. *Yungtaek Jang, Milan M. Jovanovic*, ”A New ZVS-PWM Full-Bridge Converter” IEEE Transactions on Power Electronics, Vol. 18, No. 5, Septembrie 2003, pp. 1-3.
12. *Mößlacher Christian, Guillemant Olivier*, ”Improving Efficiency of Synchronous Rectification by Analysis of the MOSFET Power Loss Mechanism”, notă de aplicație AN 2012-03, Martie 2012, pp. 11-13.
13. *Christian Andersson*, “Design of a 2.5kW DC/DC Full bridge Converter”, Teză masterat, Chalmers University Of Technology, Göteborg, Sweden, 2011, pp. 8-11.
14. *A. Bogza, D. Floricau*, “The Parallel Connection of Phase-Shifted Full-Bridge DC-DC Converters”, Rev. Roum. Sci. Techn. – Électrotechn. et Énerg, Vol. 65, pp.229-234, Bucharest, 2020.
15. *A. Bogza, D. Floricau, L. Parvulescu*, “Selection of the Power Components for a Phase-Shifted Full-Bridge Converter with Current Doubler”, pp.1-6, ICATE, Craiova, 2018.
16. Ferroxcube, https://www.ferroxcube.com/upload/media/product/file/MDS/3c90.pdf, specificație material 3C90, pp. 2-3, Sept.2008.
17. *Ferroxcube*, http://ferroxcube.home.pl/prod/assets/e32620.pdf, specificație miez planar de tip “E”, pp. 2-3, Sept.2008,
18. *Infineon Technologies AG*, specificație dispozitiv MOSFET AUIRF7669L2TR, https://www.infineon.com/dgdl/auirf7669l2.pdf?fileId=5546d462533600a4015355ad8c6113f2
19. *Infineon Technologies AG*, specificație dispozitiv MOSFET IPB65R110CFDA, https://www.infineon.com/dgdl/Infineon-IPX65R110CFDA-DS-v02_00-en.pdf?fileId=db3a304336797ff90136ba7c820925a5.
20. *Laszlo Balogh*, ”Implementing Multi-State Charge Algorithm with the UC3909 switchmode Lead-Acid Battery Charger Controller”, notă de aplicație Unitrode U-155, pp. 9-11, Mai1993.

21. *H. Michael, B.A. Potter, S. Shirsavar*, "Analytical calculation of resonant inductance for zero voltage switching in phase-shifted full-bridge converters", IET Power Electronics 6(3). pp. 523-534, Oct. 2012.
22. *M. Jovanovic, W. Tabisz, and F. Lee*, "Zero-voltage-switching technique in high-frequency off-line converters", in Applied Power Electronics Conference and Exposition (APEC), pp. 23-32, Feb. 1988.
23. *Y. Jang, M. Jovanovic, and Y.-M. Chang*, "A new zvs-pwm full-bridge converter", IEEE Transactions on Power Electronics, vol.18, no.5, pp. 1122–1129, Sep. 2003.
24. *Y. Jang and M. Jovanovic*, "A new family of full-bridge zvs converters", IEEE Transactions on Power Electronics, vol.19, no.3, pp. 701-708, May 2004.
25. *D. Constantin, P. Nicolae, Cristina Nitu*, "3D Finite Element Analysis of a Three Phase Power, IEEE transactions", Eurocon 2013 conf., pp. 1548-1551, Zagreb, Croatia, July 2013.
26. *D. MARCSA, M. KUCZMANN*, "Two-dimensional Modeling of the Motion in Induction Motor with Ferromagnetic Hysteresis", Rev. Roum. Sci. Techn. – Électrotechn. et Énerg, vol. 55, 4, pp. 351–356, Bucharest, 2010.
27. *Cristina Gheorghe, L. Melcescu, T. Tudorache, E. Mihai*, „Numerical modeling approaches for the analysis of squirrel-cage induction motor", Rev. Roum. Sci. Techn.–Électrotechn. et Energ, vol. 61, 1, pp.18-2, Bucharest, 2016.
28. *T. Tudorache, I. Trifu*, "Finite Element Analysis of an Axial Flux Hybrid Wind Generator", Rev. Roum. Sci. Techn.–Électrotechn. et Energ, vol. 62, 3, pp.229-232, Bucharest, 2016.
29. *Georgiana Razmerita, Lavinia Bobaru, Marinela Stanculescu, M.Iordache, D. Niculae*, "A Self and Mutual Inductance Calculation Resonators with Finite Element Analysis", IEEE transactions, The 7th International Conference on Modern Power Systems, pp.2-4, Cluj-Napoca, Romania, June, 2017.
30. *D. Alvarez, J. Rosero, E. Mobello*, "Analysis of Impedance Matrix in Transformer Windings", IEEE transactions, PES Transmission & Distribution Conference and Exposition - Latin America, pp.1-5, Colombia, September, 2014.
31. *A. Reatti and K. Kazimierczuk*, "Comparison of various methods for calculating the AC resistance of inductors", IEEE Transactions on Magnetics, vol. 38, no.3, pp. 1512 – 1518, May, 2002.
32. *Margueron, J-P. Keradec, A. Besr*, "Current Sharing between Parallel Turns of a Planar Transformer: Prediction and Improvement Using a Circuit Simulation Software", pp.3-7, IEEE Industrial Application Society 2007, New Orléans, United States, <hal-00289169>, Septembrie 2007.
33. *Ferroxcube*, https://www.ferroxcube.com/upload/media/product/file/MDS/3f3.pdf, 3F3 Material specification, pp. 2-3, Sept.2008.
34. *Ferroxcube*, https://www.ferroxcube.com/upload/media/product/file/MDS/3C90.pdf, 3C90 Material specification, pp. 2-3, Sept.2008.
35. *Ferroxcube*, "Soft Ferrites and Accessories Data Handbook" https://www.ferroxcube.com/en-global/download/download/11 , pp. 347-374, 534-535, July 2013.