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DEPARTAMENTUL DE ELECTROTEHNICĂ

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Doctoral Thesis Summary

CONTRIBUTIONS REGARDING THE ANALYSIS OF ELECTRICAL CIRCUITS WITH NULORS

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BUCURESTI

2022

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SPECIAL THANKS

The scientific study, regarding the analysis of electrical circuits with nullors, developed new models and solutions in the development of this doctoral thesis, requiring a considerable and sustained effort. Inevitably, there are roadblocks, difficult moments, when a piece of advice, encouragement or a life-saving idea can come at the right moment and make the difference between failure and success. That is why, with the completion of this thesis, I cannot but bring a sign of recognition and a thank to those who, during the course of my doctoral studies, were by my side and, directly or indirectly, supported me.

First of all, I want to thank Mr. Prof. Univ. Dr. Ing. Mihai IORDACHE, thanks to whom I realized this thesis and who pushed me, guided and motivated me constantly, with patience and understanding on this objective. His guidance throughout the entire period of study and research, advice given to improve the final paper, contributed significantly to the timely development of the thesis.

My warmest thanks to Mr. PhD, Associate Professor Erdei ZOLTAN, and Mr. PhD. Eng. Associate Dean Dragoș NICULAE, who closely guided my steps to discover the secrets, but also the beauty of this study topic, who had trust in my strengths and were by my side, through guidance and encouragement, throughout the duration of my research activity.

I am grateful to all the teaching staff from the Department of Electrical Engineering of the Faculty of Electrical Engineering at the Politehnica University of Bucharest, who welcomed me warmly and with whom I gained new knowledge in the field of electrical engineering. I also thank the members of the Doctoral School of the Faculty of Electrical Engineering of the POLITEHNICA University of Bucharest, who supported me in various ways in completing this work. I thank everyone for their understanding and support during my PhD studies, but also for their advice and encouragement. Finally, but not least, I thank my family for their support, patience and understanding.

FOREWORD

The main objective of this paper is to correctly define electrical equivalent circuits with nullors. Lately, the use of nullors has intensified in the generation of equivalent circuits for electronic devices, and as a result, it has been necessary to develop new and efficient methods for analyzing these circuits in their different operating regimes.

It has been proven that, according to the principles of symbolic analysis, the Nodal Analysis Method (NAM) is restrictive because the admittance matrix must contain only the elements compatible with the classic Nodal Analysis (NA). This problem can be easily solved by the Modified Nodal Analysis Method (MNAM), adding a row and a column for each element that is not compatible with the classical nodal analysis method, [23, 26]. One of the problems generated by this type of approach is related to the size of the admittance matrix. This matrix will become larger depending on the structure of the circuit and the types of its elements.

When it comes to the models used in analog circuit analysis, the requirement of high accuracy could lead to complicated calculations and then compact models are preferred during circuit analysis, mainly for the use of much simpler equations [1 - 25]. These models are more efficient for optimizing modeling and simulation time during the analysis process. From this point of view, the nullor has already proven its effectiveness in modeling active devices. Also, in models based on the nullor element, all parasitic elements can be included to analyze their contribution to the analog circuit response.

Nullors are very useful for modeling analog circuits because the circuit topology can be represented with two-terminal components such as resistors, capacitors, nullators, shunts, and independent current sources. It can also be pointed out that all controlled sources can be represented with equivalent circuits using bipolar elements and nullors. Therefore, the system of equations, for the equivalent circuit based on nullors and bipolar circuit elements, will be developed according to the classical method of nodal analysis. The nullor will be one of the basic components for models of active electronic devices, considering that the model must be developed in the simplest way, and the accuracy of the simulation of the circuit behavior must be within acceptable limits. According to this approach, problems related to small-signal models of active electronic devices that have been developed with nullors will be presented.

Another objective of this PhD thesis is to correctly define Thévenin, Norton and Hybrid equivalent circuits. These circuits allow the linear portions of electronic circuits to be separated from the non-linear ones and in this way the process of polarizing electronic devices becomes much more efficient. A special type of H ~ model is also introduced, called the nuliffied H ~ model, or simply the H ~ model; and many properties of H patterning are investigated, including circuit energy management. It is shown that H-models are not limited to single-port networks, but also cover multiports. A major property of H patterning is the local biasing of the transistors. The proposed strategy separates the linear and non-linear portions of an analog circuit and takes more control over the non-linear portions. At the end, this leads to a new technique for biasing non-linear electronic components. This separation of portions (components) within the circuit is achieved by introducing a new port patterning that cancels the non-linear device ports.

A particular attention was paid to the development of new methods, specific to the analysis and simulation of switching circuits with inconsistent initial conditions. Circuits with switch-controlled topology containing semiconductor elements are of high interest in power electronics and communications. This domain includes both externally controlled (clock) and internally controlled (state) circuits. Modeling switching circuits (circuits with switched capacitors or switched current circuits, DC-DC converters, switched modulators, etc.) with idealized models (short-circuited or open-circuited elements) very often leads to discontinuities of the variables at times switching.

LIST OF ABBREVIATIONS

VCVS - voltage controlled voltage source

VCCS-voltage controlled current source

CCVS - current controlled voltage source

CCCS- current controlled current source

MNAM- modified nodal analysis method

TM- table method

NAM- nodal analysis method

NA- nodal analysis

Voltage-Mirror - VM

Current-Mirror - CM

CGDM - Current Graph Description Matrix

VGDM- Voltage Graph Description Matrix

KCL - Kirchhoff current law

KVL - Kirchhoff voltage law

1. INTRODUCTION

1.1 STRUCTURE OF THE DOCTORAL THESIS

As a consequence of the accelerated development of computing techniques and increasingly powerful hardware and software equipment, problems related to the design, simulation and analysis of electrical systems have largely moved from the test laboratory to the personal computer. Optimum sizing, stress tests, the degree of demand of some components, all these are currently carried out with the help of specialized programs that offer results and solutions in a short time and with material savings.

In this doctoral thesis, high-performance procedures for the simulation and analysis of complex electronic circuits with nullors were presented. New algorithms and computer programs dedicated to the analysis of analog circuits with nullors have been developed.

The chapters of this research are presented as follows:

The ***First chapter*** – **Introduction** – presents a brief introduction of the whole thesis, the importance and actuality of this research topic, the aims and objectives of the choice of the topic used to develop this topic and the structure of the thesis together with the actuality and practical importance of studying this research topic, and at the end, a presentation of the publications developed during the preparation of this thesis. All this was based on a rich and rigorous documentation of the published publications in the field.

Second Chapter - **Description of the procedures for analyzing analog circuits with nullors** - active devices are described through equivalent circuits containing voltage controlled voltage sources (VCVS - voltage controlled voltage source), voltage controlled current sources (VCCS -voltage controlled current source), current controlled voltage sources (CCVS - current controlled voltage source) or current controlled current sources (CCCS - current controlled current source). These are very useful for designing circuits based on specialized software (eg SPICE). Using this type of software applications, many types of active circuit devices can be built with high precision.

In Chapter 3 – – **Thévenin, Norton and hybrid equivalent circuits –** The objective of this chapter is to introduce such a guided design procedure for polarization. Our strategy separates the linear and nonlinear portions of an analog circuit and takes more control over the nonlinear portions. This separation of portions (components) within the circuit is achieved by introducing a new modeling of ports (gates) that nullifies the ports of nonlinear devices. This, in turn, leads to a new polarization technique for nonlinear components. The result is the replacement of regular DC sources with alternative sources that are attached directly to nonlinear devices. It is shown that a unique and very strong additive property is engaged in carrying out this operation of polarization of components. Another useful property that uses this strategy is the elimination of nonlinearity in the design of the polarization process. This is achieved because, being locally polarized, nonlinear components can be replaced by their linear models operating at those Q points; therefore, the design of the polarization of the circuit is completely linear.

Thévenin, Norton, hybrid and nuliffied hybrid equivalent circuits are used for local polarization of analog circuits, [1 - 15]. Several illustrative examples are presented that highlight the veracity of the procedures elaborated.

In Chapter 4 – **Analysis of switched networks with inconsistent initial conditions –** In this chapter is presented a simple method for the analysis of complex networks with switches considering that the ideal switch avoids these problems. This approach is based on modified nodal analysis, when time-varying resistors are used to model ideal switches.
In Chapter 5 – **The application of fixator-norator pairs in the design of analog circuits-** This chapter describes a new theory of modeling and simulation of electronic devices with the help of fixator-norators pairs.

For the polarization of analog circuits, a different strategy was introduced. This paper introduces a new circuit element concept, the Fixator-Norator (FNP) pairs, which is the center of our strategy for designing the polarization of electronic circuits. Fixators and norators are used in pairs and are effective tools to perform effective polarization of electrical circuits. It is shown that these pairs are very useful in matching the critical polarization specifications with the DC power at the input.

These procedures can be easily implemented in dedicated programs for simulating complex analog circuits with nullors. We present some important examples that prove the validity of models for nullors.

In ***Chapter 6*** **- Conclusions and Original Contributions -** are summarized the results of the scientific activity carried out during the elaboration of the thesis, the main original contributions made, as well as subsequent directions of research.

IN THE ANNEXES are described: the listings of the programs used in this PhD thesis, the results obtained from the running of the programs and the comparison between these results, obtained with different programs, in order to validate their accuracy.

2. PROCEDURE DESCRIPTIONS FOR THE ANALYSIS OF ANALOGUE CIRCUITS WITH NULLORS

2.1 INTRODUCTION

Usually, active devices are described by equivalent circuits containing voltage controlled voltage sources (VCVS)), current controlled voltage sources (CCVS) or current controlled current voltage sources (CCCS). They are very useful for designing circuits based on specialized software (e.g. SPICE, CADENCE, SYSEG, SYTFG; ADS, ANSYS, etc.). Using this type of software applications, many types of devices with active circuits can be built with high precision [23 – 25]. Also, these equivalent circuits are used to develop systems of analog circuit equations based on various methods, such as the NODAL ANALYSIS (NA- nodal analysis) method, the MNAM (modified nodal analysis method) and the table method (TM).
It has been shown that, according to the principles of symbolic analysis, the Nodal Analysis Method (NAM) is restrictive because the admission matrix must contain only the elements compatible with the Nodal Analysis (NA). This problem can be easily solved by the Modified Nodal Analysis Method (MNAM), adding a row and column for each element that is not compatible with the classical method of nodal analysis (MNAM), [23, 26]. One of the problems

generated by this type of approach is related to the size of the admission matrix. This matrix will become larger, depending on the structure of the circuit and the types of its elements.
Nullors are very useful for modeling analog circuits because circuit topology can be represented with two-terminal components such as resistors, capacitors, nullors, norators and independent voltage and/or current sources. It can also be pointed out that all controlled sources can be represented with equivalent circuits using nullors. Therefore, the system of equations, for the equivalent circuit based on nullors, will be developed according to the classical method of nodal analysis. Nullor will be one of the basic components for active device models, given that the model must be developed in the simplest way, and the accuracy of the simulation of the circuit behavior must be within acceptable limits. According to this approach, this chapter will present the problems related to the small signal models of the active devices that have been developed with nullors.
The norator can be defined as an ideal two-terminal circuit (Fig. 2.1.b), which is characterized by random values for the current (i) and voltage (u) at the terminals. In other words, the norator has no defined relationship. The current and voltage have values that are only affected by the external circuit that controls the norator.
The nullator can be defined as an ideal two-terminal circuit, which is characterized by zero values for current and voltage, at the terminals. The symbol used for its graphic representation is shown in Figure 2.1.a. For this type of circuits can be defined two relationships.

A *nullator* and a *norator* together form a normal deport circuit called *nullor* (Fig. 2.1. c), which has the number of definition relationships equal to the number of ports.

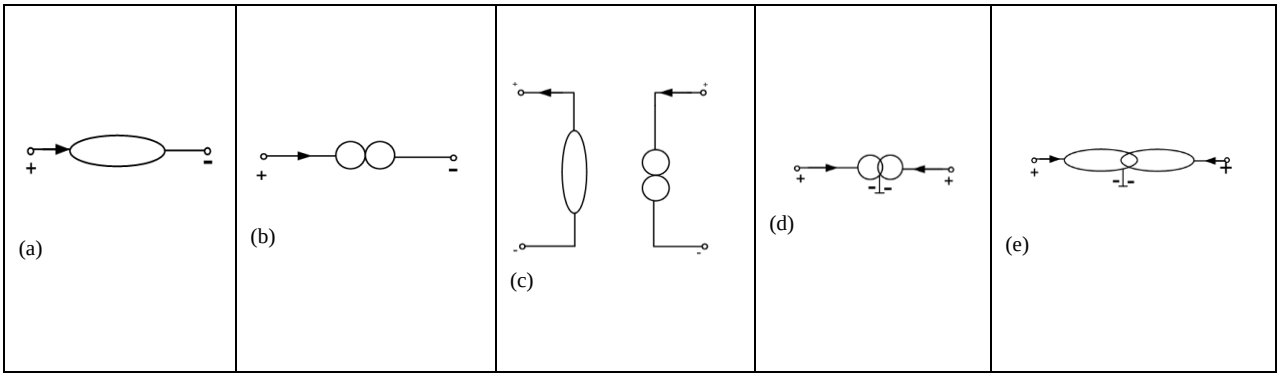
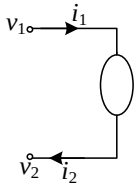
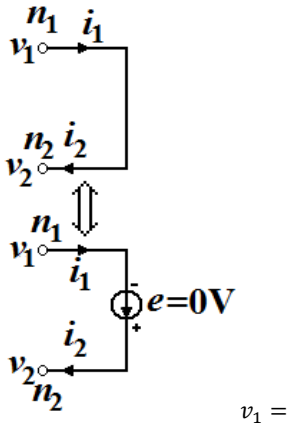
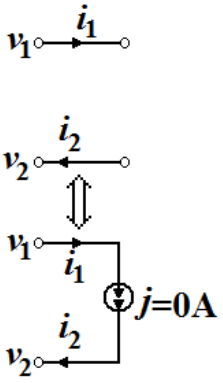
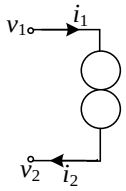
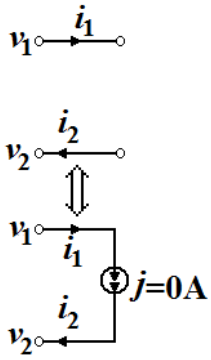
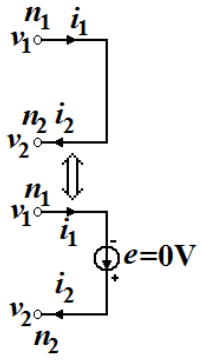
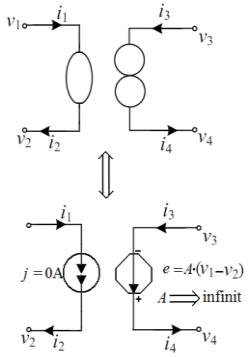
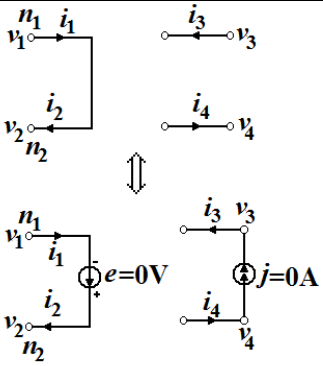
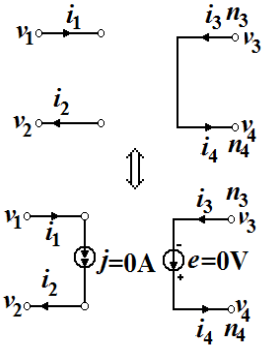


Fig. 2.1. a) The symbol of the nullator; b) The norator symbol; c) The symbol nullor d) Current mirror; e) Voltage mirror.

Table 1 shows the behavior of nullators, norators and nullors in terms of voltage, respectively of current, in G^v - the voltage graph and, respectively, G^i - the current graph.

Tabel 1

S y m b o l	Definitions	Voltage graph G^v	Current graph G^i
Nullator 	$v_1 = v_2$ $i_1 = i_2 = 0$	 $v_1 =$ $v_2 \Rightarrow n_1 \equiv n_2$ any $i_1 = i_2$	 any v_1, v_2 $i_1 = i_2 = 0$
Norator 	any v_1, v_2 any $i_1 = i_2$	 any v_1, v_2 $i_1 = i_2 = 0$	 $v_1 = v_2 \Rightarrow n_1 \equiv n_2$ any $i_1 = i_2$
Nullor 	$i_1 = i_2 = 0$ $v_1 = v_2$ any v_3, v_4 any $i_3 = i_4$	 $v_1 = v_2 = arbitrary \Rightarrow$ $\Rightarrow n_1 \equiv n_2, any\ i_1 = i_2,$ $i_3 = i_4 = 0$, any $v_3 \neq v_4$	 any $v_1 \neq v_2$ v_1, $i_1 = i_2 = 0$; $v_3 = v_4 \Rightarrow n_3 \equiv n_4$ any $i_3 = i_4$

The input port of the nullor is modeled by the nullator which is characterized by two equations:

(2.1)

$$v_1 = v_2 = \text{arbitrary},\ \ i_1 = i_2 = 0.$$

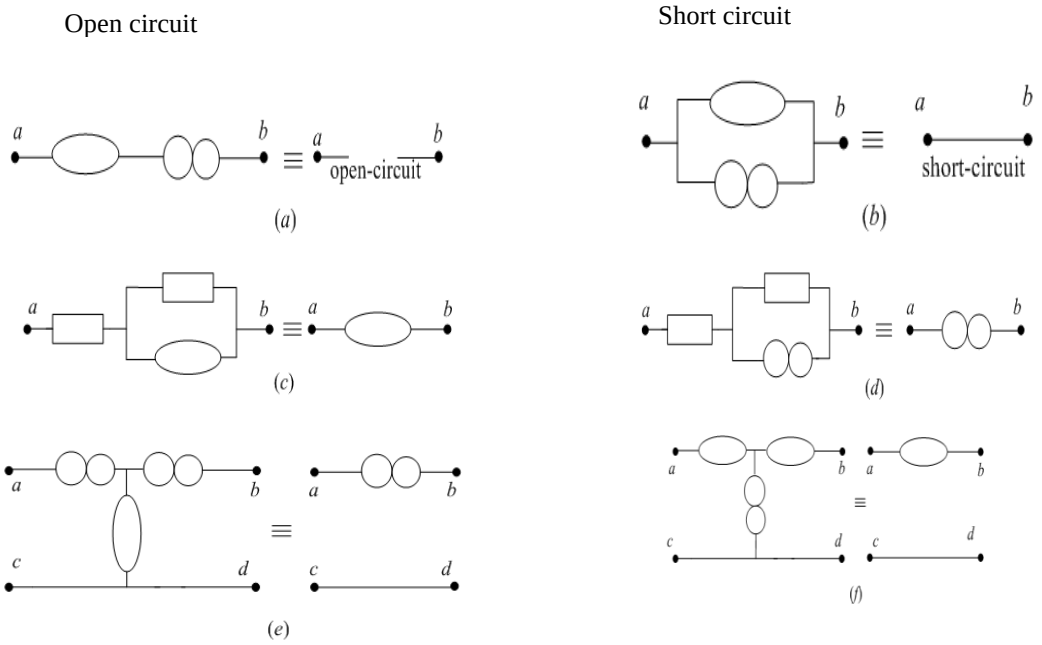
So, the nullator is simultaneously one open in G^i current graph and short-circuit in G^v voltage graph. The output port of the nullor is modeled by the norator where both, the voltage and current can be assumed to have arbitrary values:

$$v_1 \neq v_2 = \text{arbitrary}, \quad i_1 = i_2 = \text{arbitrary}. \tag{2.2}$$

The nullor is a two-port element and it is known as universal active element [20 - 22]. This concept means that the nullor along with capacitors and resistors can be used to design a maximum number of functions with the minimum number of active devices. That is, if a suitable set of linear and nonlinear passive elements is available, then no active element other than nullors are needed to implement any linear or nonlinear circuit function. So, nullators, norators, resistances, along with capacitances can synthesize a complete set of linear or linearized equations.

2.2 EQUIVALENT CIRCUITS WITH NULLORS

The most widely used equivalences of the combinations between nullators and norators for when assembling networks that contain nullors and impedances are shown in figure 2.2. In figure 2.2, a, if the current flows from node a, cannot flow to b, since the current through the nullator is zero. It means that a series connection between a nullator and a norator is equivalent to one open-circuit. In figure 2.2, b, the current flows from a to b through the norator. The voltage between a and b becomes zero, due to the nullator properties, so that a parallel connection of the nullator and norator is equivalent to one short-circuit. The remaining connections have equivalencies according to the nullator and norator i=f(v) characteristics.



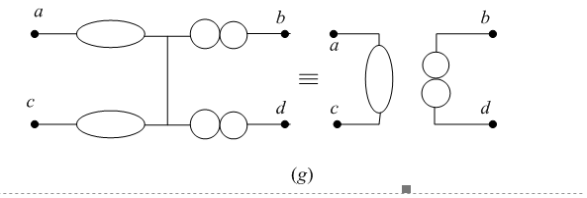


Fig. 2.2. Equivalences between sections of circuits assembled with nullators and norators

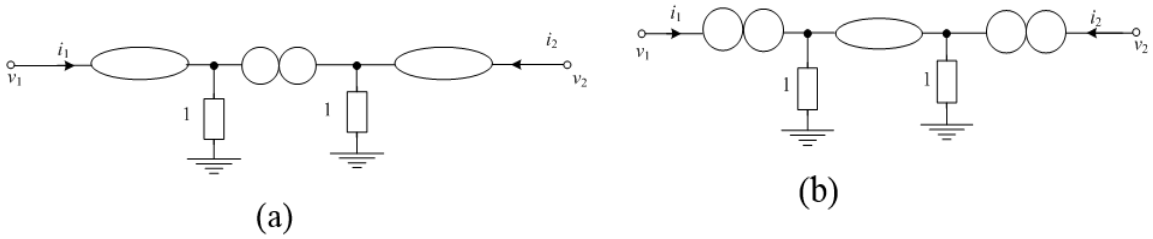


Fig. 2.3. Nullor and grounded resistor-based VM (a) and CM (b).

Furthermore, nullors can be combined with grounded resistors in order to be able to obtain output voltage/current signals with opposite polarity with respect to the input ones. This feature cannot be acquired intrinsically by nullators or norators [11 - 22]. One can mention the ideal *unity-gain* Voltage-Mirror (VM) (fig. 2.3, a) and the Current-Mirror (CM) (fig. X.3, b), as examples of active devices with inverting properties. Each of them can properly modeled utilizing the nullor [1 - 10].

Each of the circuits VM (fig. 2.3, a) and CM (fig. 2.3, b) represented above, with the inverting feature achieved, is described by distinct voltage/current equations, VM by (2.3), respectively CM by (2.4).

$$\begin{aligned} v_2 &= -v_1 = \text{arbitrary}, \\ i_1 &= i_2 = 0. \end{aligned} \tag{2.3}$$

$$\begin{aligned} v_2 &\neq v_1 = \text{arbitrary}, \\ i_1 &= i_2 = \text{arbitrary}. \end{aligned} \tag{2.4}$$

The VM and CM nullor based models may include parasitic elements [1, 30-31]. In such a situation, any possible network can be equaled to a combination of nullators, norators, CMs, VMs and impedances, in the same manner as for the nullor.

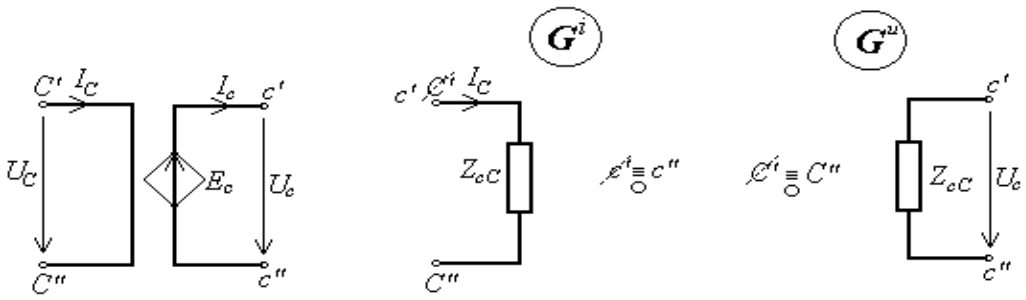
If eventually, one of the v_1 or v_2 terminals from figure 2.3, a is grounded, the application of the equivalences shown in figure 2.2 reduces VM to a nullator. In a similar manner, if any terminal from figure 2.3.b is grounded, the application of the equivalences shown in figure 2.2 converts CM into a norator.

Due to the peculiarities presented by the ordered sources, the extension of the matrix analysis to the study of non-reciprocal electrical circuits requires to associate with the circuit two connection graphs: one of current, G^i and another voltage, G^u. The two graphs contain the same number of independent sides, vertices, and loops. They differ in the positions they occupy within them the command and ordered sides (ports) of the four types of sources ordered by the carrier, simulated by dipole elements.

(Tabel 2).

Tabel 2

CCVS – Current Controlled Voltage Source



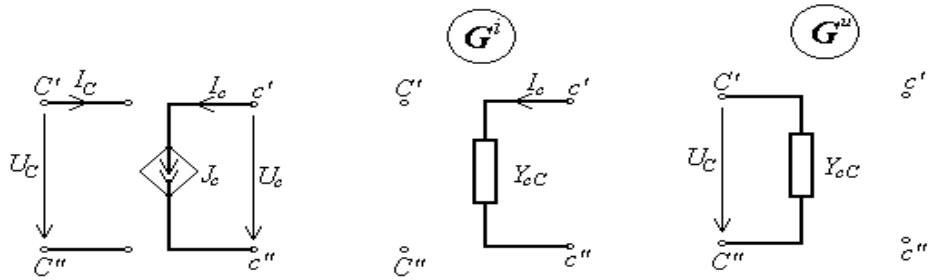
For DC circuits:.

$$U_C = 0 \ \ \forall I_C;\ U_c = E_c = R_{cC} I_C \ \ \text{, in general } R_{cC} = R_c$$

For AC circuits and for operational circuits:

$$U_C = 0 \ \ \forall I_C;\ U_c = E_c = Z_{cC} I_C \ \ \forall I_c;\ \text{in general } Z_{cC} = Z_c .$$

VCCS – Voltage Controlled Current Source



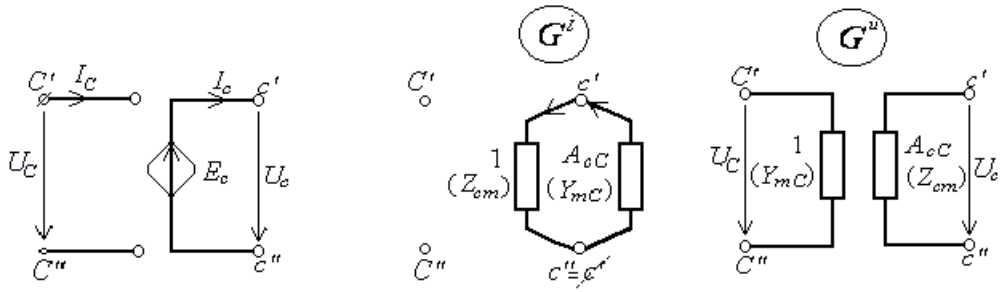
For DC circuits:.

$$I_C = 0 \ \ \forall U_C;\ I_c = J_c = G_{cC} U_C \ \ \forall U_c;\ \text{in general } G_{cC} = G_c$$

For AC circuits and for operational circuits:

$$I_C = 0 \ \ \forall U_C;\ I_c = J_c = Y_{cC} U_C \ \ \forall U_c;\ \text{in general } Y_{cC} = Y_c .$$

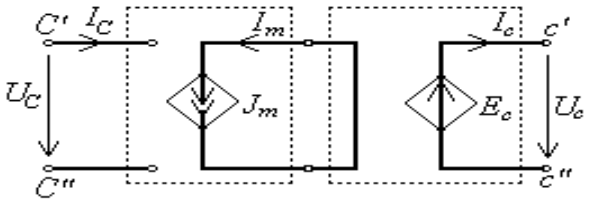
VCVS – Voltage Controlled Voltage Source



$$I_C = 0 \;\; \forall U_C ; U_c = E_c = A_{cC} U_C \;\; \forall I_c$$

The voltage-controlled voltage source can be equated to a voltage-controlled current source connected in cascade with a current-controlled voltage source, as follows:

Equivalent scheme for two inhomogeneous controlled sources connected in cascade



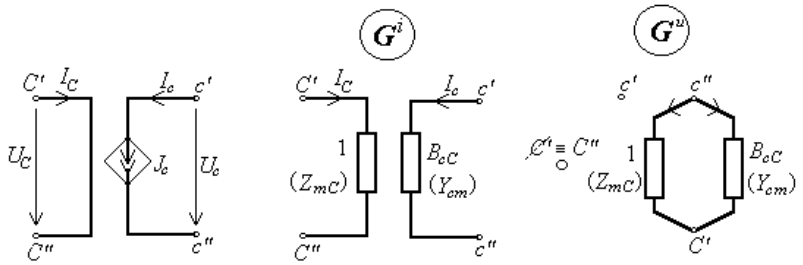
For DC circuits:.

$$J_m = G_{mC} U_C , \;\; I_m = J_m ; E_c = U_c = R_{cm} I_m = R_{cm} G_{mC} U_C \Rightarrow A_{cC} = R_{cm} G_{mC}$$

For AC circuits and for operational circuits:

$$J_m = Y_{mC} U_C , \;\; I_m = J_m ; E_c = U_c = Z_{cm} I_m = Z_{cm} Y_{mC} U_C \Rightarrow A_{cC} = Z_{cm} Y_{mC}$$

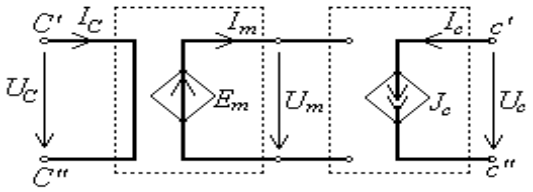
CCCS – Current Controlled Current Source



$$U_C = 0 \;\; \forall I_C , \;\; J_c = B_{cC} I_C \;\; \forall U_c$$

The current-controlled current source can be equated to a current-controlled voltage source connected in cascade with a current source controlled in voltage, as follows:

Scheme equivalent to two inhomogeneous controlled sources connected in cascade



For DC circuits:.

$$E_m = R_{mC}U_C,\ U_m = E_m;\ J_c = I_c = G_{cm}U_m = G_{cm}R_{mC}I_C \Rightarrow B_{cC} = G_{cm}R_{mC}$$

For AC circuits and for operational circuits:

$$E_m = Z_{mC}U_C,\ U_m = E_m;\ J_c = I_c = Y_{cm}U_m = Y_{cm}Z_{mC}I_C \Rightarrow B_{cC} = Y_{cm}Z_{mC}.$$

Observations:

1. Resistors, coils, capacitors and independent sources of voltage and current have the same position in G^i and G^u;
2. To describe graphs G^i and G^u a matrix with 4 lines and *l* columns is used (*l* is the number of graph sides), called the current graph description matrix (CGDM) and voltage graph (VGDM - the voltage graph description matrix). Each column in the CGDM (VGDM) contains the initial node, the final node, the type and weight (in the case of calculating circuit functions) of the side;
3. Because any branch short-circuited in G^i or in G^u causes the elimination of a node, in order to keep the enumeration of the nodes in a natural order (which is advantageous in applications), all the indices larger than the index of the removed node are reduced by a unit;
4. Magnetic couplings are shaped by inductors and CCVS [9];
5. The above modeling technique of the four controlled sources leads to two directed graphs having only conductance branches (admittances);
6. The two graphs have the same number of knots, branches and loops. They differ only in the location of the control and controlled branches of the four types of controlled sources;
7. Since any contraction of the branches in the two graphs causes a node to be removed, the number of vertices in the G^i and G^v is lower than in the initial circuit with the number of CCVS: $n_{G^i} = n_{G^v} = n - n_{CCVS}$.

2.3 *KIRCHHOFF'S LAWS APPLIED TO DC CIRCUITS*

Kirchhoff's theorems can be specified as an array as a matrix as:

$$\boldsymbol{A}^i \boldsymbol{i}_b^i = \boldsymbol{0} \text{ (KCL- TIK),} \tag{2.5}$$

$$\boldsymbol{B}^v \boldsymbol{u}_b^v = \boldsymbol{0} \text{ (KVL-TIIK).} \tag{2.6}$$

Where $\boldsymbol{A}^i$ ($\boldsymbol{B}^v$) is the low-impact matrix at sides-nodes in the current graph (the impact matrix of the sides-loops in the voltage graph, and $\boldsymbol{i}_b^i$ ($\boldsymbol{u}_b^v$) is the vector of currents (voltages) in the current (voltage) graph.
For DC linear circuits, Kirchhoff's laws have the following developed forms:

$$\begin{aligned} &\text{KCL: } \sum_{b_k \in (n_j^i)} I_k^i = - \sum_{b_k \in (n_j^i)} J_k^i \text{ , } j = \overline{1, n^i - 1}; \\ &\text{KVL: } \sum_{b_k \in (l_h^v)} \left(R_k I_k^i + U_{j_k}^v + U_{j_{ck}}^v \right) = \sum_{b_k \in (l_h^v)} \left(E_k^v + E_{ck}^v \right), \; h = \overline{1, l^v}. \end{aligned} \tag{2.7}$$

The Kirchhoff equations have, for AC linear circuits, in harmonic mode in the complex, the form:

$$\begin{aligned} &\text{KCL: } \sum_{b_k \in (n_j^i)} \underline{I}_k^i = - \sum_{b_k \in (n_j^i)} \underline{J}_k^i \text{ , } j = \overline{1, n^i - 1}; \\ &\text{KVL: } \textstyle\sum_{b_k \in (l_h^v)} \left(\underline{Z}_k \underline{I}_k^i + \sum_{\substack{p=1 \\ p \neq k}} j\omega L_{kp} \underline{I}_p^i + \underline{U}_{j_k}^v + \underline{U}_{j_{ck}}^v \right) = \textstyle\sum_{b_k \in (l_h^v)} \left(\underline{E}_k^v + \underline{E}_{ck}^v \right) \text{ , } h = \overline{1, l^v}. \end{aligned} \tag{2.8}$$

The operational form of the Kirchhoff equations have, for linear circuits, the structure:

$$\begin{aligned} &\text{KCL: } \sum_{b_k \in (n_j^i)} I_k^i(s)_k^i = - \sum_{b_k \in (n_j^i)} J_k^i(s), \; j = \overline{1, n^i - 1}; \\ &\text{KVL: } \sum_{b_k \in (l_h^v)} \left(Z_k(s) I_k^i(s) + \sum_{\substack{p=1 \\ p \neq k}}^{b} s L_{kp} I_p^i(s) + U_{j_k}^v(s) + U_{j_{ck}}^v(s) \right) = \sum_{b_k \in (l_h^v)} \left(E_{ek}^v(s) + E_{ck}^v(s) \right), \; h = \overline{1, l^v}. \end{aligned} \tag{2.9}$$

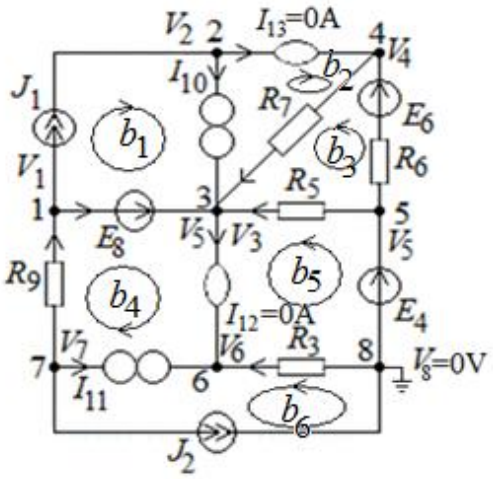
In equations (2.9) the $E_{ek}^v(s)$ includes also the initial conditions at the time of $t_0 = 0$,

$$L_k i_{L_k}^i(0_-) + \sum_{\substack{p=1 \\ p \neq k}}^{b} L_{kp} i_{L_p}^i(0_-) - \frac{u_{C_k}^v(0_-)}{s}.$$

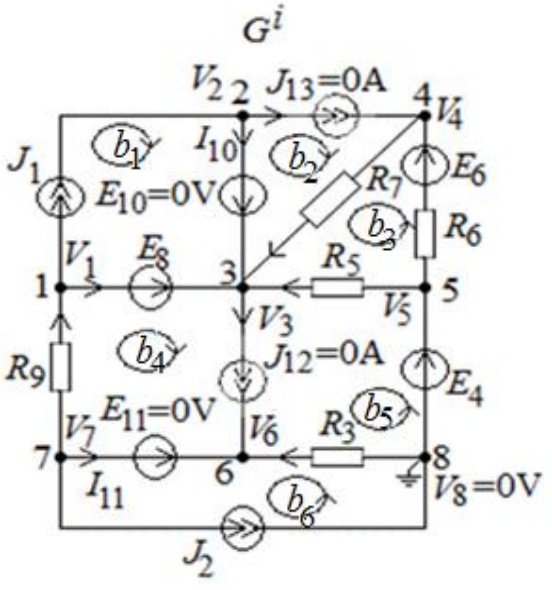
Observation 1

Taking into account the behavior of nulles (see Table 1) from the point of view of current, i.e. voltage, Kirchhoff's theorems, loop current equations, modified nodal equations, semi-state equations, state equations and side constituent equations for linear and/or nonlinear circuits with nulls, regardless of the operating regime of the circuit analysed, they can be formulated directly on the initial scheme of the circuit, without the need to generate the current and voltage graphs respectively (see examples).

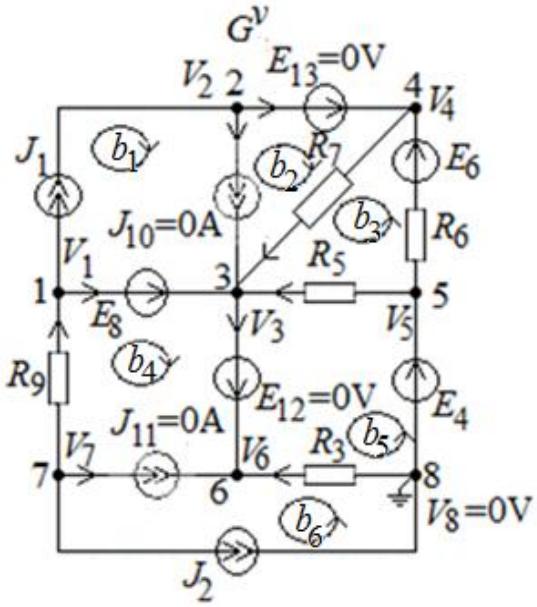
To describe the algorithm for applying Kirchhoff's theorems to null electrical circuits, the continuous current circuit in Figure 2.4(a) is considered.



(a)



(b)



(c)

Fig. 2.4. a) Diagram of the initial circuit; b) Current graph G^i; c)Voltage graph G^v.

Step 1. Taking into account the behavior, from the point of view of current, respectively tensiuns, nulls and clouders respectively (see Table 1), the two graphs are built, the current graph – figure 2.4 (b) and, respectively, the voltage graph – figure 4 (c). The sides of the two graphs shall be oriented in the same direction as the direction of the currents and the independent loops corresponding to the current and voltage graph respectively shall be identified;

Step 2. The first Kirchhoff law is written in the $n^i - 1$ nodes in the current graph:

$$\begin{gathered}(n_1^i):\ I_8^i - I_9^i = -J_1;\ \ (n_2^i):\ I_{10}^i = J_1;\\ (n_3^i):\ -I_5^i - I_7^i - I_8^i - I_{10}^i = 0;\ \ (n_4^i):\ -I_6^i + I_7^i = 0;\\ (n_5^i):\ -I_4^i + I_5^i + I_6^i = 0;\ \ (n_6^i):\ -I_{11}^i - I_3^i = 0;\\ (n_7^i):\ I_9^i + I_{11}^i = -J_2;;\end{gathered} \tag{2.10}$$

Step 3. Equations corresponding to the second Kirchhoff law, written on those l^v Independent loops of the voltage graph, have the structure:

$$\begin{gathered}(l_1^v):\ U_1^v + U_{10}^v = -E_8;\ \ (l_2^v):\ R_7 I_7^v - U_{10}^v = 0;\\ (l_3^v):\ -R_5 I_5^i + R_6 I_6^i + R_7 I_7^i = E_6;\ \ (l_4^v):\ R_9 I_9^i - U_{11}^v = E_8;\\ (l_5^v):\ -R_3 I_3^i + R_5 I_5^i = E_4;\ \ (l_6^v):\ U_2^v + R_3 I_3^i - U_{11}^v = 0.\end{gathered} \tag{2.11}$$

Step 4. Solve, with an appropriate algorithm, the system of equations (2.10) and (2.11) in relation to the unknowns: $I_3^i, I_4^i, I_5^i, I_6^i, I_7^i, I_8^i, I_9^i, I_{10}^i, I_{11}^i, U_1^v, U_2^v, U_{10}^v$, and U_{11}^v. With the characteristic equations of the circuit elements, all currents and all voltages of the circuit sides in Figure 2.4(a) are calculated. Obviously, the sizes associated with the nullators are null I_{12} = 0 A, I_{13} = 0 A, U_{12} = 0 V, şi U_{13} = 0 V;

Step 5. Check the power balance, i.e. the relationship, $P_G = P_R$, where:

$$\begin{aligned}P_G &= -U_1 J_1 - U_2 J_2 + E_4 I_4 + E_6 I_6 + E_8 I_8 - U_{10} I_{10} - U_{11} I_{11};\\ P_R &= R_3 I_3^2 + R_5 I_5^2 + R_6 I_6^2 + R_7 I_7^2 + R_9 I_9^2.\end{aligned} \tag{2.12}$$

Since everywhere the rule of association of the reference meanings from the receivers has been adopted, the powers generated by the current sources, independent and/or ordered, and those given by the norators are calculated with the "minus" sign in front.

Taking into account the definitions of null and norators, the Kirchhoff equations can be formulated directly on the initial circuit in Figure 2.4. (a). These equations have the structure of:

$$\begin{gathered}TIK\\ (n_1): I_8 - I_9 = -J_1;\ (n_2): I_{10} = J_1;\ \ (n_3):\ -I_5 - I_7 - I_8 - I_{10} = 0;\ (n_4): I_7 - I_6 = 0;\\ (n_5):\ -I_4 + I_5 + I_6 = 0;\ (n_6):\ -I_3 - I_{11} = 0;\ \ (n_7): I_9 + I_{11} = -J_2;\\ TIIK\\ (l_1): U_1 + U_{10} = -E_8;\ (b_2): R_7 I_7 - U_{10} = 0;\ \ (b_3):\ -R_5 I_5 + R_6 I_6 + R_7 I_7 = E_6;\\ (l_4): R_9 I_9 - U_{11} = E_8;\ \ (b_5):\ -R_3 I_3 + R_5 I_5 = E_4;\ (b_6): U_2 + R_3 I_3 - U_{11} = 0.\end{gathered} \tag{2.13}$$

For the following numerical values of the circuit in Figure 4. (a): J_1 = 2 A, J_2 = 4 A, R_3 = 100 Ω, E_4 = 200 V, R_5 = 100 Ω, R_6 = 200 Ω, E_6 = 200 V, R_7 = 100 Ω, E_8 = 200 V, R_9 = 100 Ω, the solutions are obtained;

U_1=-342.857143; I_1=2.000000; U_2=-600.000000, I_2=4.000000; I_3=0.285714; I4=3.714286

I_5=2.285714; I_6=1.428571; I_7=1.428571; I_8=-5.714286; I_9=-3.714286;

U_{10}=142.857143; I_{10}=2.000000; U_{11}=-571.428571; I_{11}=-0.285714.

Step 6: A suitable algorithm can correctly solve equation systems (2.10), (2.11) with respect to the variables below: $I_3^i, I_4^i, I_5^i, I_6^i, I_7^i, I_8^i, I_9^i, I_{10}^i, I_{11}^i, U_1^v, U_2^v, U_{10}^v$, şi U_{11}^v. Then all currents and voltages become readily available for all sides of the circuit. Currents and voltages associated with nullators $I_{12}, I_{13}, U_{12}, U_{13}$ have only zero values. In the power balance, the power generated P_G must be equal to the power dissipated by the Joule effect P_R. While adopting the receiver's convention, the DC powers generated by independent and/or controlled current sources, as well as the power transferred by the nulls, appear as negative in (2.12).

$$\begin{aligned} P_G &= -U_1J_1 - U_2J_2 + E_4I_4 + E_6I_6 + E_8I_8 - U_{10}I_{10} - U_{11}I_{11} = 2522.449\ \text{W;} \\ P_R &= R_3I_3^2 + R_5I_5^2 + R_6I_6^2 + R_7I_7^2 + R_9I_9^2 = 2522.449\ \text{W.} \end{aligned} \tag{2.14}$$

2.4 LOOP CURRENT METHOD IN DC CIRCUITS WITH NULLORS

The loop current method is based on the introduction of loop currents as intermediate quantities that satisfy the KCL and that can be determined by applying KVL to the independent loops in the electrical circuit. The constituent equations of all elements of the circuit are written as relationships between currents G^i and voltages G^v. Here's the following algorithm:

Step 1: Electronic devices and multipolar and/or multiport circuit elements are replaced by equivalent intermediate circuits containing only dipole elements and controlled sources. Then the newly obtained circuits are replaced with equivalent schemes based on nullors.

Step 2: The circuit obtained at the previous step, in its final form is associated with two graphs: the current one G^i and the voltage one G^v. Independent loops are selected inside the graphs. For each independent loop, it is assigned a reference direction and a current, called a 'loop current'.

Step 3: Currents in the branches of the current graph G^i are expressed as functions of the loop currents as follows:

$$i_k^i = \sum_{\left(b_h^i\right) \ni l_k^i} i_h^i,\ k = \overline{1,b},\ \text{sau}\ \boldsymbol{i}_b^i = \left(\boldsymbol{B}^i\right)^t \boldsymbol{i}_l^i, \tag{2.15}$$

For the circuit in Figure 2.4, the initial current equations are given by (2.13)

$$\begin{aligned}
&J_1^i = I_{l_1}^i,\ J_2^i = I_{l_2}^i,\ I_3^i = -I_{l_5}^i + I_{l_6}^i,\\
&I_4^i = I_{l_5}^i,\ I_5^i = -I_{l_3}^i + I_{l_5}^i,\ I_6^i = I_{l_3}^i,\\
&I_7^i = I_{l_2}^i + I_{l_3}^i,\ I_8^i = -I_{l_1}^i + I_{l_4}^i,\ I_9^i = I_{l_4}^i,\\
&I_{10}^i = I_{l_1}^i - I_{l_2}^i,\ I_{11}^i = -I_{l_4}^i - I_{l_6}^i;
\end{aligned} \tag{2.16}$$

Step 4: When KVL is applied over the attached loops to G^v, the currents in the branches of G^i are expressed as functions of the loop currents according to (2.15). In order to obtain all the independent equations, the currents in the graph G^i, circulating through independent sources, as well as currents through nullators (that is, all of them are equal to zero) are expressed according to the loop currents of the same G^i. The currents of the controlled sources are expressed as algebraic sums of the loop currents of the current graph G^i, resulting in as many independent equations as the unknown variables.

Step 5: The voltages and currents of the sides are finally determined by applying (2.15) and the characteristic equations of the circuit elements. The equations, in terms of loop currents, for the circuit in Figure 2.4. (a) have the following structure (2.17).

$$\begin{aligned}
&(l_1):\ U_1 + U_{10} = -E_8;\\
&(l_2):\ R_7\left(I_{l_2} + I_{l_3}\right) - U_{10} = 0;\\
&(l_3):\ -R_5\left(-I_{l_3} + I_{l_5}\right) + R_6 I_{l_3} + R_7\left(I_{l_2} + I_{l_3}\right) = E_6;\\
&(l_4):\ R_9 I_{l_4} - U_{11} = E_8;\\
&(l_5):\ -R_3\left(I_{l_6} - I_{l_5}\right) + R_5\left(-I_{l_3} + I_{l_5}\right) = E_4;\\
&(l_6):\ U_2 + R_3\left(I_{l_6} - I_{l_5}\right) - U_{11} = 0;\\
&(b_1):\ I_{l_1} - J_1 = 0;\quad (b_2):\ I_{l_6} - J_2 = 0;\\
&(b_{12}):\ I_{l_4} + I_{l_5} = 0;\quad (b_{13}):\ I_{l_2} = 0.
\end{aligned} \tag{2.17}$$

2.5 MODIFIED NODAL ANALYSIS IN DC CIRCUITS WITH NULLORS

The unknown variables of this method are represented by (n-1) electrical potentials corresponding to the circuit nodes, with the exception of node *n* whose potential is equal to zero (reference). Vector $\boldsymbol{i}_m^i$ which contains the currents of the incompatible elements of the circuit, is expressed with the classical nodal method. It is said that a circuit element is incompatible with the classical nodal method if the current through it cannot be expressed using its parameters and node potentials. A clear example is represented by norators whose currents are treated as independent variables. These unknowns satisfy the TIIK-KVL for any circuit

loop. The calculation of these unknowns is based on writing the TIK-KCL in (n-1) nodes in the current graph and the expression of branch current currents using the constituent equations of the branches. The following algorithm is in place:

Step 1: Absolutely identical to step 1 in the previous section.
Step 2: The circuit obtained at the previous step, in its final form, is associated with two graphs: the current one G^i and the voltage one G^v. The branches of the graphs are oriented in the same direction as the currents crossing them, identifying (n-1) the independent vertices and (l = b – n + 1) independent loops.
Step 3: Tensions of the sides belonging to the graph G^v are expressed according to the potentials of nodes such as:

$$u_k^v = v_k^{v+} - v_k^{v-},\ k = \overline{1,b},\ \text{or}\ \boldsymbol{u}_b^v = \left(\boldsymbol{A}^v\right)^t \boldsymbol{v}_{n-1}^v, \tag{2.18}$$

The voltages of the sides belonging to the graph G^v are expressed according to the potentials of nodes such as:

$$\begin{aligned}
&(n_1):\ J_1 + I_8 - (V_7 - V_1)/R_9 = 0;\\
&(n_2):\ -J_1 + I_{10} = 0;\\
&(n_3):\ -(V_5 - V_3)/R_5 - (V_4 - V_3)/R_7 - I_8 - I_{10} = 0;\\
&(n_4):\ -(V_5 - V_4 + E_6)/R_6 + (V_4 - V_3)/R_7 = 0;\\
&(n_5):\ -I_4 + (V_5 - V_3)/R_5 + (V_5 - V_4 + E_6)/R_6 = 0;\\
&(n_6):\ -I_{11} + V_6/R_3 = 0; (n_7):\ (V_7 - V_1)/R_9 + I_{11} + J_2 = 0;\\
&(b_4):\ -V_5 + E_4 = 0;\ (b_8):\ V_1 - V_3 + E_8 = 0;\\
&(b_{12}):\ V_3 - V_6 = 0;\ (b_{13}):\ V_2 - V_4 = 0.
\end{aligned} \tag{2.19}$$

2.6 KIRCHHOFF'S LAWS APPLIED ON AC CIRCUITS

For linear AC circuits operating in harmonic mode, Kirchhoff's laws show the following general expressions (2.20), (2.21).

$$\sum_{b_k \in (n_j^i)}^{(A)} \underline{I}_k^i = -\sum_{b_k \in (n_j^i)}^{(A)} \underline{J}_k^i\ ,\ j = \overline{1, n^i - 1}\ \text{(TIK-KCL)} \tag{2.20}$$

$$\sum_{b_k \in (l_h^v)} \left(\underline{Z}_k \underline{I}_k^i + \sum_{\substack{p=1 \\ p \neq k}}^{b} j\omega L_{kp} \underline{I}_p^i + \underline{U}_{j_k}^v + \underline{U}_{j_{ck}}^v \right) = \sum_{b_k \in (l_h^v)} \left(\underline{E}_{ek}^v + \underline{E}_{ck}^v \right),\ h = \overline{1, l^v}.\ \text{(TIIK-KVL)} \tag{2.21}$$

O The very simple method for solving the systems of equations represented by (2.20), (2.21) is to convert these equations into operational form. Following the application of the Laplace transformation term by term, the operational form of Kirchhoff's equations can be described according to the relationships (2.22), (2.23) as follows:

$$\sum_{b_k \in \left(n_j^i\right)} I_k^i(s) = -\sum_{b_k \in \left(n_j^i\right)} J_k^i(s),\ j = \overline{1, n^i - 1} \quad \text{(KCL)} \tag{2.22}$$

$$\sum_{b_k \in \left(l_h^v\right)} \left(Z_k(s) I_k^i(s) + \sum_{\substack{p=1 \\ p \neq k}}^{b} sL_{kp} I_p^i(s) + U_{j_k}^v(s) + U_{j_{ck}}^v(s) \right) = \tag{2.23}$$

$$= \sum_{b_k \in \left(l_h^v\right)} \left(E_{ek}^v(s) + E_{ck}^v(s) \right),\ h = \overline{1, l^v}. \quad \text{(KVL)}$$

Equation (2.20) includes the initial conditions, recorded for the time being t_0=0, incorporated inside the term $E_{ek}^v(s)$, and expressed by (2.24):

$$\Delta E_{ek}^v(0) = L_k i_{L_k}^i(0_-) + \sum_{\substack{p=1 \\ p \neq k}}^{b} L_{kp} i_{L_k}^i(0_-) - \frac{u_{Ck}^v(0_-)}{s} \tag{2.24}$$

2.7 MODIFIED NODAL ANALYSIS APPLIED TO ALTERNATING CURRENT CIRCUITS WITH NULLORS

The unknown variables of this method are represented by *(n-1)* electrical potentials corresponding to the circuit nodes, with the exception of node *n* whose potential is equal to zero (reference). Vector $\boldsymbol{i}_m^i$ which contains the currents of the incompatible elements of the circuit, is expressed with the classical nodal method. It is said that a circuit element is incompatible with the classical nodal method if the current through it cannot be expressed using its parameters and node potentials. A clear example is represented by norators whose currents are treated as independent variables. These unknowns satisfy the KVL for any circuit loop. The calculation of these unknowns is based on writing the KCL in (n-1) nodes in the current graph and the expression of branch current currents using the constituent equations of the sides. The following algorithm is in place:

Step 1: Absolutely identical to step 1 in the previous section.

Step 2: The circuit obtained at the previous step, in its final form is associated with two graphs: the current one G^i and the voltage one G^v. The sides of the graphs are oriented in the same direction as the currents crossing them, identifying *(n-1)* the independent vertices and *(l = b – n + 1)* independent loops.

Step 3: Tensions of the sides belonging to the graph G^v are expressed as functions of node potentials as:

$$u_k^v = v_k^{v+} - v_k^{v-},\ k = \overline{1,b},\ \text{or matrix}\ \boldsymbol{u}_b^v = \left(\boldsymbol{A}^v\right)^t \boldsymbol{v}_{n-1}^v, \tag{2.25}$$

Step 4: In G^v, all elements found incompatible with classical NAM are highlighted, while their currents in G^i are considered to be independent variables. Then the KCL is applied to independent nodes (n-1) of the G^i: all the currents of the sides, now compatible with NAM are functions of the parameters of the sides and the potentials of the nodes in G^v. To complete the set of independent equations, it is necessary to add the characteristic equations to the sides in the G^v. These equations refer to circuit elements that are incompatible with NAM. The currents relating to CCVS and CCCS, respectively the electromotor forces relating to VCVS and VCCS, are expressed as functions of the control variables. Latter are themselves expressed as functions of independent variables. The general procedure outlines a number of equations equal to unknowns.

Step 5: Currents and voltages are obtained by the MNAM equations and the characteristic equations of the elements.

2.8 EXAMPLES OF ALTERNATING CURRENT CIRCUITS WITH NULLORS

Example 2: The circuit in Figure 2.7(a), contains two operational amplifiers and two passive elements of the circuit, resistors R_1, R_2 and the capacitor C.

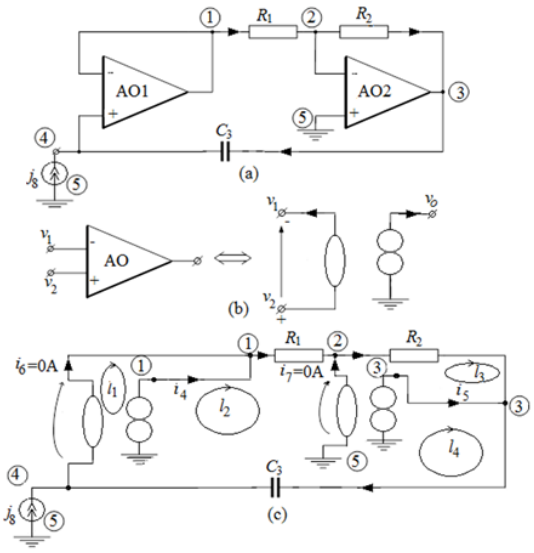


Fig. 2.7. a) Capacitive multiplier, b) Equivalent circuit of the operational amplifier built with nullors, c) Scheme of the capacity multiplier using nullors

In harmonic behavior, this circuit plays the character of a capacitive multiplier relative to the input terminals marked as 4 and 5.

While the replacement of operational amplifiers with nulls (see Figure 2.7(b)), the final circuit representation is shown in Figure 2.7(c).

For the equivalent circuit shown in Figure 2.3(c), KCL was applied for the harmonic mode. Based on the nullity properties of voltage and current, equations can be obtained (2.30.(a-d)).

$$(n_1): \underline{I}_1 - \underline{I}_4 = 0 \tag{2.30,a}$$

$$(n_2): -\underline{I}_1 + \underline{I}_2 = 0 \tag{2.30,b}$$

$$(n_3): -\underline{I}_2 + \underline{I}_3 - \underline{I}_5 = 0 \tag{2.30,c}$$

$$(n_4): -\underline{I}_3 - \underline{J}_8 = 0. \tag{2.30,d}$$

The KVL equations for l=4 have the following form (2.31, a-d) (2.31,a)

$$(l_1) \equiv n_5 - n_1 - n_5 : \ \underline{U}_8 - \underline{U}_4 = 0$$

$$(l_2) \equiv n_5 - n_1 - n_2 - n_5 : \ R_1\underline{I}_1 + \underline{U}_4 = 0 \tag{2.31,b}$$

$$(l_3) \equiv n_5 - n_2 - n_3 - n_5 : \ R_2\underline{I}_2 - \underline{U}_5 = 0 \tag{2.31,c}$$

$$(l_4) \equiv n_5 - n_2 - n_3 - n_5 : \underline{I}_3 / (j\omega C_3) + \underline{U}_5 - \underline{U}_8 = 0 \tag{2.31,d}$$

The complete solution once the equation systems (2.30 (a-d)) and (2.31) have been solved, respectively. a-d))) is given in (2.32 (a-j)).

$$\underline{I}_1 = -\frac{j\underline{J}_8}{\omega C_3(R_1 + R_2)}, \tag{2.32,a}$$

$$\underline{I}_2 = -\frac{j\underline{J}_8}{\omega C_3(R_1 + R_2)}; \ \underline{I}_3 = -\underline{J}_8, \tag{2.32,b}$$

$$\underline{I}_4 = -\frac{j\underline{J}_8}{\omega C_3(R_1 + R_2)}, \tag{2.32,c}$$

$$\underline{I}_5 = -\frac{\underline{J}_8(R_1\omega C_3 + R_2\omega C_3 - j)}{\omega C_3(R_1 + R_2)}, \tag{2.32,d}$$

$$\underline{U}_1 = -\frac{jR_1\underline{J}_8}{\omega C_3(R_1 + R_2)}, \tag{2.32,e}$$

$$\underline{U}_2 = -\frac{j\underline{J}_8R_2}{\omega C_3(R_1 + R_2)}, \tag{2.32,f}$$

$$\underline{U}_3 = \frac{j\underline{J}_8}{\omega C_3}, \tag{2.32,g}$$

$$\underline{U}_4 = -\frac{j\underline{J}_8 R_1}{\omega C_3 (R_1 + R_2)}, \tag{2.32,h}$$

$$\underline{U}_5 = -\frac{j\underline{J}_8 R_2}{\omega C_3 (R_1 + R_2)}, \tag{2.32,i}$$

$$\underline{U}_8 = \frac{j\underline{J}_8 R_1}{\omega C_3 (R_1 + R_2)}. \tag{2.32,j}$$

The complex input impedance is given by the relation (2.16):

$$\underline{Z}_{ii}(\omega) = -\frac{\underline{U}_8^v}{\underline{J}_8} = -\frac{j}{\omega C_3 \left(1 + \frac{R_2}{R_1}\right)} = \frac{G_2}{j\omega C_3 (G_1 + G_2)}. \tag{2.33}$$

A sensitivity to input impedance in relation to the conductance G_1 is:

$$S_{G_1}^{\underline{Z}_{ii}(\omega)} = -\frac{G_1}{G_1 + G_2}. \tag{2.34}$$

For pasive elements with values C_3 = 10 pF, R_1 = 100 **Ω** si R_2 = 100 k**Ω**, the result is equivalent capacity: (2.35)

$$C_e = C_3 \left(1 + \frac{R_2}{R_1}\right) = 10.10^{-12} \left(1 + \frac{10^5}{10^2}\right) = 10{,}01\,\text{nF}.$$

This value representing the equivalent capacity is about a thousand times the capacity C_3. This circuit is used in integrated circuit technology to obtain high values for capacities. Due to miniaturization, integrated circuit technology usually produces capacitors with low capacity values. The capacity multiplier effect is called *the Miller Effect* for Capacities, [4, 14, 21].

2.9 CONCLUSIONS

In this chapter, the concepts of nullator, norator and nullor have been introduced along with well-defined properties. Next, a few DC models based on nullors have been introduced. A DC circuit is equivalent to three circuits based on nullors, applying the laws of Kirchhoff, the loop current method, respectively the modified nodal analysis method (MNAM): three modes of solving the initial DC circuit are suggested in the paper.

Many models of circuits based on nullors have been generated. MNAM itwas applied to solve ordinary AC circuits with multiple sources, using nullors. Current and voltage graphs were used to formulate the set of equations that characterize the operation of the ac circuit in

harmonic mode. The proposed modeling procedure applied to the controlled sources in the two graphs is simple, straightforward and based on the properties of the nullors. Equivalent circuits based on the functional schemes with nullsmodel both the control port and the controlled port by admitting placed in different positions in the two graphs. The two graphs obtained in this way contain the same number of branches, knots and loops. Moreover, the MNAM was used to determine the performance of two circuits based on operational amplifiers: the capacity multiplier, respectively the universal filter. In general, equations describing analog circuits can be generated directly, starting from the initial circuit configurations. This last statement applies to all types of operating regimes.

This chapter describes a new modeling of active devices based on nullors at the abstraction circuit level. After a brief description of the concepts of nullator, norator and nullor and their properties, we proceed to the modeling of active devices not only to the voltage mode, but also to the current mode and to the mixed mode of operation from the point of view of the circuit with two ports and four terminals are described in some details.

In general, for the simulation of the four biport-controlled sources with nullors and, in general, for the modeling of multiport circuit elements with equivalent circuit circuits formed by bipolar circuit elements and taking into account the behavior of nullors in terms of current and voltages, two graphs of current are associated, for the systematic formulation of Kirchhoff laws, two graphs one of current G^i and another voltage G^u. The two graphs have the same topology (the same number of: sides, knots and independent loops) and the sides are characterized by identical parameters, they differ in the positions of bipolar circuit elements (sides) simulating the four sources ordered by the carrier. Kirchhoff's first theorem and the equations of bubble currents are formulated on the current graph G^i, Kirchhoff's second theorem and nodal equations (modified) are formulated on the voltage graph G^u, and in the characteristic equations (constituents) the currents (voltages) from the sides of the current (voltage) graph are used.

By simulating the nullators by ideal current-independent sources with the current intensity $j = 0$ A and the norators with ideal voltage-controlled sources $e_c(u_C)$ with the transfer factor (amplification) in voltage A with very high values (theoretically infinite), all types of equations, in any operating regime, can be formulated directly on the circuit with the nullors without the need for the current and voltage graphs. The voltage control voltages of the voltage-controlled voltage sources are those at the norator terminals – the nullors are biport circuit elements with the input side formed by a nullator, and the output side consists of a norator.

Numerous models of circuits based on nullors have been generated. The current and voltage graphs were used to systematically generate, in completely symbolic, partial-symbolic and numerical form, all the transfer functions with the help of generalized topological formulas with homogeneous parameters, based on the enumeration of the common sides in the two graphs. For the analysis of linear and/or nonlinear analog circuits linearized on portions with nulli, all methods of analysis of normal electronic circuits have been successfully used (method based on Kirchhoff's laws, loop currents method, classical nodal method, modified nodal method, state equation method and semi-state equation method). The variety as a structure of analog circuits with the analyzed nullors confirms the special usefulness of using nullors models of complex electronic devices.

The examples presented in detail validate the described models for analog circuits with nullors.

3. THÉVENIN, NORTON AND HYBRID EQUIVALENT CIRCUITS

3.1. *INTRODUCTION*

In current high-speed technology, analog and mixed signal integrated circuit technology occupies an important and decisive place in communication and signal processing. In particular, with CMOS technology quickly embracing the field, designing analog circuits has become more difficult than ever [1–11]. Other technological developments, such as: lower supply voltages, lower power consumption, complexity and performance, and large number of transistors, have substantially increased the demand for new design methodologies and techniques.

A major difficulty in treating analog circuits is the polarization of DC - obtaining the desired operating points (operation) with rapid convergence; and the problem is getting worse with the advancement of technology, which is due to the increase in the size and complexity of the circuit. The analysis can even lead to several operating points in DC or instability at operating points caused by positive feedbacks [3, 12, 13]..

The objective of this chapter is to introduce such a guided design procedure for polarization. Our strategy separates the linear and nonlinear portions of an analog circuit and takes more control over the nonlinear portions. This separation of portions (components) within the circuit is achieved by introducing a new modeling of ports (gates) that cancels the ports of nonlinear devices. This, in turn, leads to a new polarization technique for nonlinear components. The result is the replacement of ordinary DC sources with alternative sources that are attached directly to nonlinear devices. It is shown that a unique and very strong additive property is engaged in carrying out this operation of polarization of components. Another useful property that uses this strategy is the elimination of nonlinearity in the design of the polarization process. This is achieved because, being locally polarized, nonlinear components can be replaced by their linear models operating at those Q points; therefore, the design of the polarization of the circuit is completely linear.

Paragraph 3.2 defines the equivalent Thévenin and Norton circuits, specifying the conditions necessary and sufficient that a linear uni-port circuit (one port) can be substituted by an equivalent Thévenin or Norton circuit. Paragraph 3.3 sets out the necessary and sufficient conditions for a linear uni-port circuit to be replaced by an equivalent hybrid circuit.

Thévenin, Norton, and hybrid equivalent circuits are used in the construction of Nullified Hybrid equivalent circuits (Nullified Hybrid equivalent circuits). Thévenin, Norton, hybrid and zero hybrid equivalent circuits are used for local polarization of analog circuits, [1 - 15]. Several illustrative examples are presented that highlight the veracity of the preocedies elaborated.

3.2 THÉVENIN AND NORTON EQUIVALENT CIRCUITS

Un uni-port *N* with a single port (with a single gate) is *well defined,* in relation to that gate, unless it contains any circuit element that is *connected,* electrically or non-electrically, to a physical variable outside N: for example, controlled sources that depend on an external

variable of N , transformer windings magnetically coupled to an external winding, a photoresistor coupled to an external light source, etc.

Any resistive, linear, time-invariant, *well-defined* uni-port N which meets the following *single solvency* condition may be replaced by an equivalent uni-port without affecting the solution of any external circuit (not necessarily linear or resistive) connected to uni-port N.

3.2.1 Thévenin N_{eq} equivalent circuit for a uni-port

Figure 3.1(a) represents a linear resistive circuit with two terminals, N, with both independent and internally dependent sources.

Unique solvency condition for a uni-port Thévenin circuit equivalent to N_{eq}. A uni-port circuit N (fig. 3.1 (a)) obtained by connecting an ideal source independent of current j to terminals A, B of N (oriented from node B to node A) has a unique solution for any current value j.

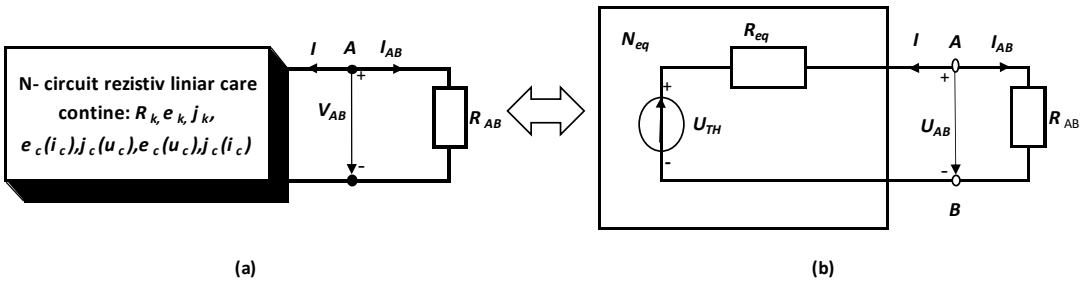


Fig. 3.1. a) A linear resistive circuit with two access terminals to which the resistor is connected R_{AB}; b) Thévenin equivalent circuit.

If the N circuit in figure 3.1(a) satisfies the single solvency condition above, then the N circuit may be substituted by the equivalent voltage generator with $E_e = U_{Th} = U_{AB0}$ and $R_i = R_{eq} = R_{AB0}$ - *called uni-port equivalent circuit Thévenin N_{eq}* (fig. 3.1 (b)). If between terminals A, B connects the resistor with the resistance R_{AB}, then the current I_{AB} has the expression:

$$I_{AB} = -I = \frac{U_{Th}}{R_{eq} + R_{AB}}, \tag{3.1}$$

where: $R_{eq} = R_{AB0}$ is the equivalent resistance in relation to terminals A, B (when $R_{AB} = \infty$) of the passivated N circuit (all t.e.m. e (all currents j) of (ai) voltage-independent sources (current equal to zero) – called *Thévenin equivalent resistance*; $U_{Th} = U_{AB0}$ represents the voltage between terminals A and B when idling (when $R_{AB} = \infty$).

3.2.2 Norton N_{eq} *equivalent circuit* for one-port

Unique solvency condition for a Norton uni-port circuit equivalent to N_{eq}. A uni-port circuit N (fig. 3.2 (a)) obtained by connecting an ideal voltage-independent source e to

terminals A, B of *N* (oriented from node B to node A) has a unique solution for any value of t.e.m. *e*.

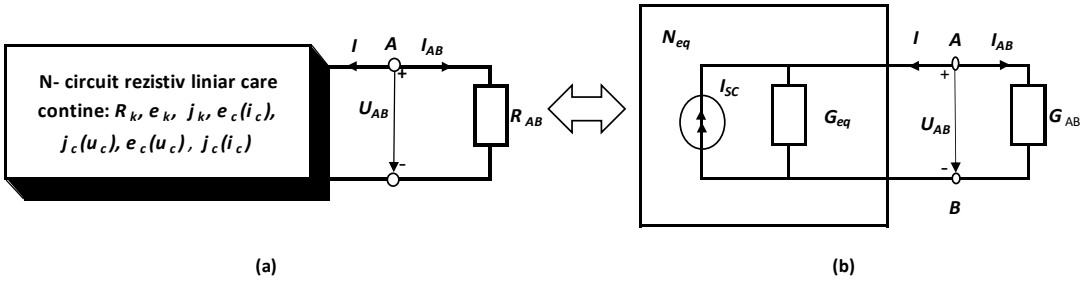


Fig. 3.2. a) A biport linear resistive circuit; b) Circuitul echivalent Norton.

When the *N* circuit in Figure 3.2(a) satisfies the unique solvency condition corresponding to the Norton equivalent circuit, then the *circuit N* can be substituted by the equivalent current generator with $J_e = I_{sc}$ and $G_i = G_{eq}$ *called the equivalent uni-port circuit Norton* N_{eq} (Fig.3.2(b)). If between terminals A, B connects the resistor with the conductance G_{AB}, then the voltage U_{AB} can be calculated with the formula:

$$U_{AB} = \frac{I_{sc}}{G_{eq} + G_{AB}}, \tag{3.2}$$

where: $G_{eq} = G_{AB0}$ is the equivalent conductance in relation to terminals A, B (when) of the $R_{AB} = \infty$ passivized N circuit (all t.e.m. *e* (all currents *j*) of voltage-independent sources (current equal to zero) – called *Norton equivalent conductance*; $I_{sc} = I_{ABsc}$ is *the short circuit current* between terminals A and B when a resistance $R_{AB} = 0\ \Omega$ is connected between these terminals.

Before demonstrating the above theorems, let's first consider some interpretations and applications of these theorems:

1. The main value of Thévenin's theorem, as well as the Norton theorem, is that it allows us to replace *any* part of a circuit that forms a single *linear resistive port* (but which is of no interest in a given situation) with only two circuit elements, without affecting the solution of the rest of the circuit;

2. Either , $R_{eq} \neq 0$. If we short-circuit the equivalent Thévenin Neq circuit and solve the circuit thus obtained in relation to current I, it is obtained (see fig. 3.1):

$$I_{sc} = -I_{sc} = I_{ABsc} = \frac{U_{Th}}{R_{eq}} \tag{3.3}$$

3. When $R_{eq} \neq 0$ şi $G_{eq} \neq 0$, the uni-port *N* circuit has, according to the independent real source equivalence theorem, a Thévenin equivalent circuit as well as a Norton equivalent circuit. Equivalence relationships have the expressions:

$$\text{Thévenin parameters: } \begin{cases} R_{eq} \\ U_{AB0} = U_{Th} \end{cases} \Rightarrow \text{parameters Norton : } \begin{cases} G_{eq} = \dfrac{1}{R_{eq}} \\ I_{sc} = I_{Absc} = \dfrac{U_{Th}}{R_{eq}} \end{cases}; \tag{3.4}$$

$$\text{Norton parameters: } \begin{cases} G_{eq} \\ I_{sc} = I_{ABsc} \end{cases} \Rightarrow \text{parameters Thévenin : } \begin{cases} R_{eq} = \dfrac{1}{G_{eq}} \\ U_{Th} = \dfrac{I_{sc}}{G_{eq}} \end{cases}.$$

4. When a uni-port *N* is equivalent in relation to two access terminals A, B to both a Thévenin equivalent circuit and a Norton equivalent circuit, *its input characteristic* (*of the operating point*) is defined by the relationships:

$$U_{AB} = R_{eq}I + U_{Th} = -R_{eq}I_{AB} + U_{Th} \text{ sau } I = G_{eq}U_{AB} - I_{sc}. \tag{3.5}$$

This feature of the operating point (input) consists of a *straight line with a slope* G_{eq} and the intersection with the ordinate in the plane $U_{AB} – I$ is I_{sc}, as shown in figure 3.3, a, or with a slope R_{eq} and the intersection U_{Th} in plane I-U_{AB}.

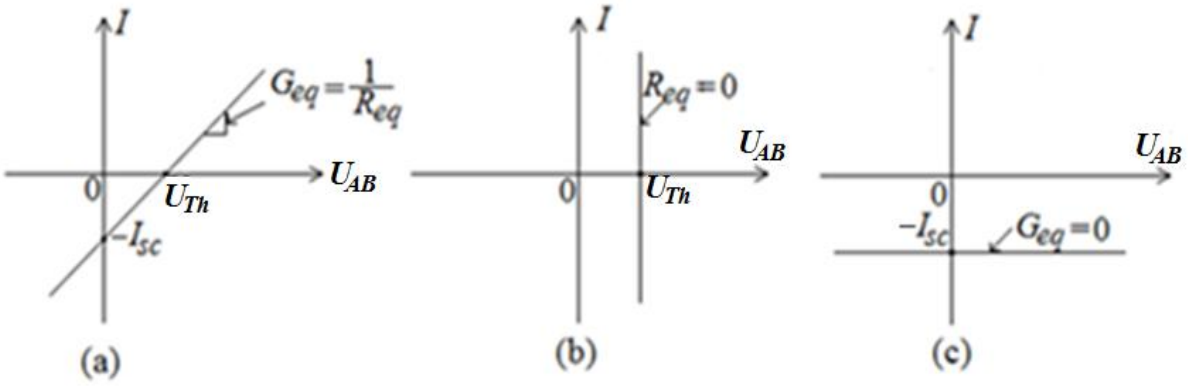


Fig. 3.3. a) Characteristic of the triggering (input) point of N with $U_{bone} = U_{Th} > 0$ and $G_{eq} > 0$; b) Function point (input) feature with $U_{AB} = U_{Th}$ and $R_{eq} = 0$; c) Function point (input) characteristic with $I = -I_{sc}$ and $G_{eq} = 0$.

The feature of the operating point in Figure 3.3(a) is drawn for the case where $G_{eq} > 0$, $U_{oc} = U_{Th} > 0$ and $Isc > 0$.

5. The limiting case $R_{eq} = 0$ is shown in Figure 3.3(b). A Thévenin equivalent circuit in this case consists only of an ideal independent battery voltage source of $U_{oc} = U_{Th}$ volts. A corresponding Norton equivalent circuit does not exist because $G_{eq} =\infty$. Indeed, the single solvency condition fails in this case – the Kirchhoff second theorem (TIIK) is not valid when a voltage source is applied. The limit case "dual" $G_{eq} = 0$ is shown in Figure 3.3 (c). A Thévenin equivalent circuit does not exist in this case,

while the Norton equivalent circuit degenerates into an ideal current-independent source with a current intensity equal to I_{sc};

6. A uni-port *N* which does not allow, in relation to terminals A, B, any Thévenin equivalent circuit or a Norton equivalent circuit is shown in Figure 3.4(a). The characteristic $U_{AB} - I_{AB}$ is defined by the equations

$$U_{AB} = 0 \quad I_{AB} = 0, \tag{3.6}$$

and therefore consists only of a point located in the origin. We must bear in mind that the "virtual short circuit" that characterizes the entrance gate of an ideal operational amplifier, which works in the linear region, has this property. Such a gate is called a nullator.

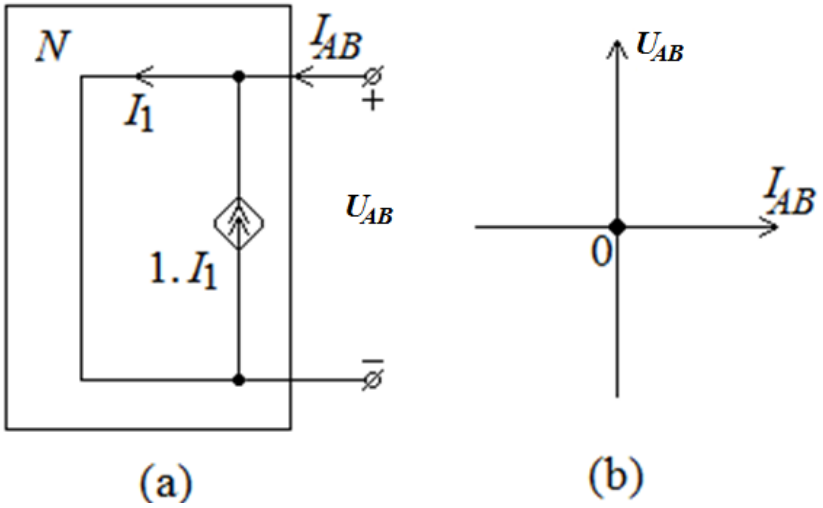


Fig. 3.4. A uni-port characterized by a point in plane U_{AB}-I_{AB} - origin.

Because the function point feature for both the equivalent ports of Thévenin and Norton consists of a straight line, it is clear that the null does not have a single port equivalent to Thévenin or Norton. Indeed, both "unique solubility conditions" are violated by this single port. We note that we can only drive *N* with a 0-V voltage source or a 0-A current source.

From the above observations it can be found that if the biport *N* is not controlled in the current, then this circuit does *not* possess an equivalent Thévenin circuit. Dual, if *N* is not voltage controlled, then the *N* circuit does not possess an equivalent Norton circuit. So, in applying the Thévenin or Norton theorem, one can ignore the verification of the "single solvency condition – unique solvability condition" because this generally makes checking the determinant of the associated T-array matrix a difficult test. Instead, one can simply proceed to calculate R_{eq} or G_{eq}. Failure to obtain a single value for R_{eq} (respectively, G_{eq}) could imply that the *N* circuit does not have an equivalent Thévenin (respectively, Norton) circuit.

Examples 3.1: Determine the Thévenin and Norton equivalent circuits for the bipolar circuit shown in Figure 3.5(a). To calculate the parameters R_{eq} and G_{eq} , the simplified circuit in Figure 3.5 (b) is used. For any voltage *U* applied to terminals A, B, current $I_1 = U/R$, and from the first theorem Kirchhof results $I_1 = -4I_1$. So, $I = -(4V)/R$.

Hence

$$R_{eq} = \frac{1}{G_{eq}} = -\frac{R}{4}. \tag{3.7}$$

Since both R_{eq} and G_{eq} are finite numbers, we can conclude that the circuit N in Figure 2.5, a has a bipolar circuit (one-port) equivalent to Thévenin and Norton respectively.

Analyzing the circuits in figures 3.5(c) and 3.5(d) with the SCAP program [3] we obtain:

$$V_{Th} = V_{os} = \frac{4E + J \cdot R}{4} \text{ si } I_{sc} = -\frac{R \cdot J + 4 \cdot E}{R}. \tag{3.8}$$

Therefore $R_{eq} = 1/G_{eq} = U_{Th}/I_{sc} = -R/4$. So, the same results are achieved as above.

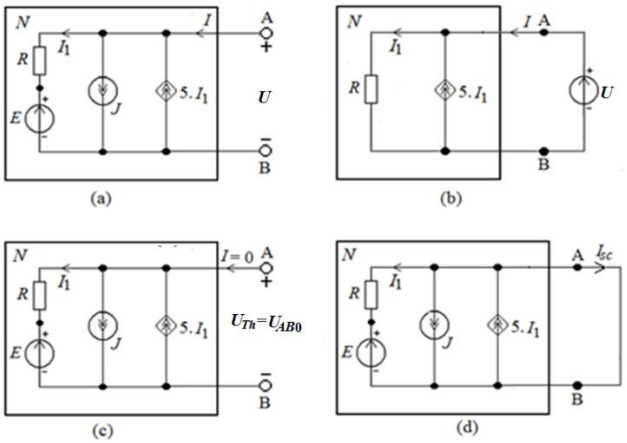


Fig. 3.5. a) Uni – port *N*; b) Uni – port *N* simplified with a single port, obtained by passivation of all independent sources inside the uni-port *N*; c) Circuit used to calculate the voltage $U_{Th} = U_{AB0}$; d) Circuit used to calculate the current I_{sc}.

3.2.3 Thévenin and Norton theorems demonstration

Only the Thévenin theorem will be demonstrated, as the Norton theorem can also be demonstrated. The *N* circuit is discovered in two subcircuits connected in cascade (see Fig. 3.6 (a)), one denoted *N*, purely resistive, contains linear resistors invariant invariant in time and all types of independent and/or controlled sources, and the other denoted N_L which can be linear or nonlinear resistive.

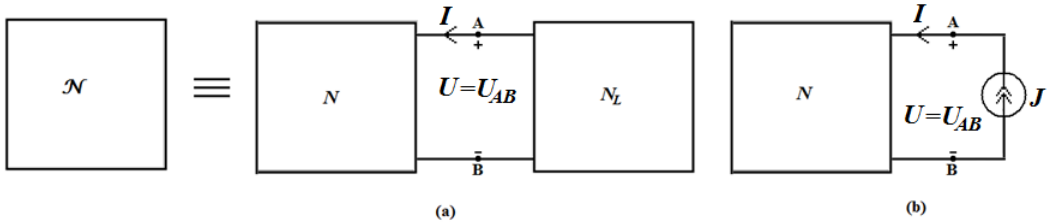


Fig. 3.6. a) Partitioning of the arbitrary circuit N into a linear resistive uni-port *N* and a uni-port circuit N_L which does not necessarily have to be linear or resistive; b) The circuit N is fed through the terminalel A and B with an ideal source independent of current, having the intensity *J* of the current.

Since the *N* circuit is purely resistive, it is completely specified by the operating point characteristic at each moment of time, in relation to terminals A and B. Therefore, with regard to the N_L circuit, its solution depends only on this feature of the operating point. It is therefore sufficient to demonstrate that the circuit *N* is equivalent, in relation to terminals A and B, to a Thévenin circuit that has the same operating characteristic.

Supply the *N* circuit with an ideal source independent of current, having the intensity $J = I$ of the current (fig. 3.6 (b)). The N circuit is considered to have within *it* n_E *voltage independent sources with* voltage.E_1, E_2, ..., E_{nE} and n_J *independent current sources* J_1, J_2, ..., J_{nJ}. It follows from the 'single solvency condition' that the resistive circuit in Figure 3.6(b) has *a unique solution* for all values of independent sources. So, the *superposition theorem* can be applied and according to this theorem the voltage $U = U_{AB}$ from terminals A, B of the circuit *N* has the expression

$$U = U_{AB} = R_{AB\_AB}J + \sum_{k=1}^{n_E} A_{AB\_k}E_k + \sum_{k=1}^{n_J} R_{AB\_k}J_k \,, \tag{3.9}$$

Where $R_{AB\_AB} = \frac{V_{UAB}}{J}\Big|_{\substack{E_k=0 \text{ for all } k \\ J_k=0 \text{ for all } k}} = R_{AB0} = R_{eq}$ is the equivalent resistance in relation to terminals A, B (when) of the $R_{AB} = \infty$ passivized N circuit (all t.e.m. *e* (all currents *j*) of (ai) sources independent of voltage (current) within the interor of the circuit *N* – called *the equivalent resistance Thévenin*; $U_{Th} = U_{AB0}$ is the voltage between terminals A and B when idling (when). $R_{AB} = \infty$ is the starting point or resistance to entry into *N* according to all independent sources on the insided *N*; $A_{AB\_k} = \frac{U_{AB}}{E_k}\Big|_{\substack{E_m=0 \text{ for all } m\neq k \\ J_k=0 \text{ for all } k, \text{and } J=0}}$ represents the transfer factor (amplification) in the voltage from the side l_k to the voltage U_{AB} și $R_{AB\_k} = \frac{U_{AB}}{J_k}\Big|_{\substack{E_k=0 \\ J_m=0 \ m\neq k, \text{și } J=0}}$ is the transfer resistance from side l_k to side l_{AB}.

If $J = 0$, the voltage *U* is, by definition, $U = U_{AB0} = U_{Th}$. So, the last two sums in equation (3.9) represent the voltage $U_{AB0} = U_{Th}$. In accordance with the above arguments equation (3.9) can be written in the form:

$$V = R_{Th}I + U_{Th} \,. \tag{3.10}$$

calculate the current *I*.

Example 3.2: Figure 3.7(a) shows a simplified small signal equivalent circuit of a single-storey BJT amplifier with virtual polarization sources included. The Thévenin model for the amplifier viewed from the output port is shown in Figure 3.7(b). Figure 3.7(c) shows the characteristic port curve (one line), indicating the linearity of the circuit. The figure also shows how we can

move from the Thévenin model, specified by the point T(2.5V, 0), to the Norton model, given as a point N(0, 1.25mA) on the characteristic line.

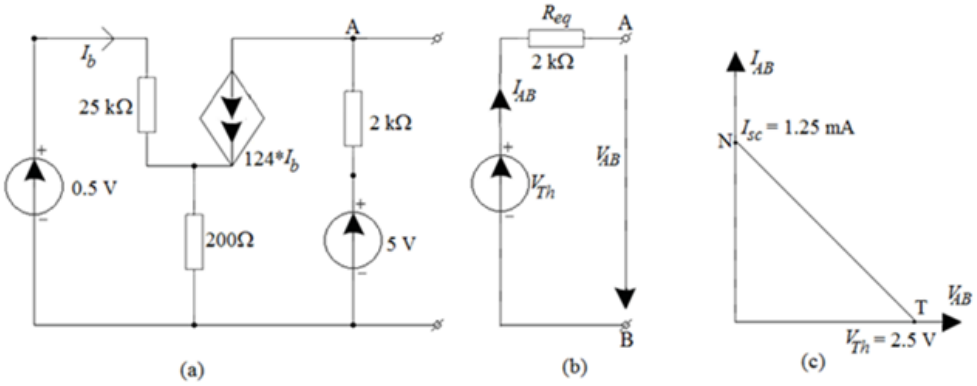


Fig. 3.7. a) An equivalent simplified small signal circuit of a single-storey BJT amplifier; b) The Thévenin equivalent circuit; c) The characteristic curve of the port, indicating the linearity.

However, despite their simplicity, there is a rigidity involved in the representation of the port by either the Thévenin equivalent circuitry or the Norton circuits. As shown in Figure 3.7(c) the Thévenin or Norton model occupies only one point on the characteristic line, where the line meets one of the axes.

The complexity of the circuit created in this way may not be so obvious for a single-port connection, but for several ports the complexity can become quite significant. There are other cases in which circuits on both sides of a port have to engage in some exchanges (sources or components); therefore, a more dynamic port modeling may be required. Examples can be found in the transformation of the source, the modeling of the noise source and the cases of power transport. Port cancellation is another example that uses hybrid modeling, as discussed below.

3.3 HYBRID EQUIVALENT CIRCUIT

Either a linear resistive circuit containing resistors, independent sources of voltage and/or current and all four types of biport-controlled sources. We extract from the terminals (nodes) A and B of the circuit the resistor with the resistance R_{AB}, as in figure 3.8. The circuit to the left of vertices A, B in Figure 3.8 shall satisfy the conditions for the equivalence of this circuit to the Thévenin equivalent circuit and the Norton equivalent circuit respectively. In order for a linear resistive circuit to be substituted, in relation to terminals (vertices) A, B, with an equivalent Thévenin circuit, voltage U_{AB} must exist and be unique to any *value J* of the current of an ideal source independent of current, when the resistor R_{AB} is replaced by such a source. Similarly, if the resistor R_{AB} in Figure 3.8, is substituted by an ideal voltage-independent source with t.e.m. *E*, the resistive linear circuit to the left of terminals A, B can be replaced by a Norton equivalent circuit if the current I_{AB} exists and is uniquely determined for any *E* value of t.e.m. of the ideal independent voltage source.

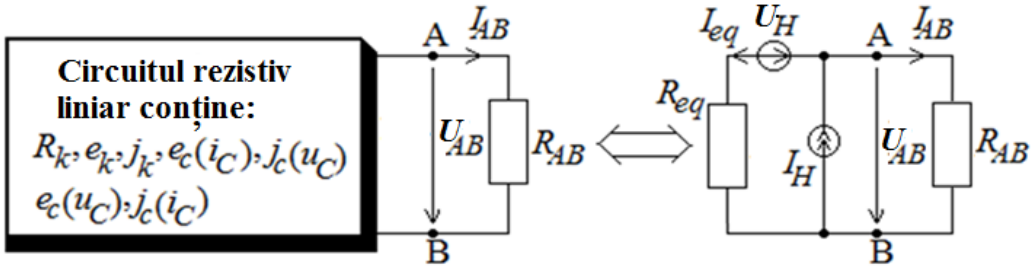


Fig. 3.8. Hybrid equivalent circuit.

A hybrid equivalent circuit, or simply an H~ model, of a two-terminal network is a generalized version of the equivalent Thevenin or Norton circuit; for resistive circuits it consists of a voltage source U_H, a current source I_H and an equivalent resistance, R_{eq}, which is identical to that of the Thévenin or Norton model (Fig. 3.8). It turns out that here one source, V_H or I_H, can be selected arbitrarily, and the other source is determined by the equation (3.12).

We assume that the circuit to the left of the *resistor* R_{AB} in Figure 3.8 satisfies the conditions for the existence of the equivalent ciruites Thévenin and Norton. According to the Thévenin theorem, *the current* I_{AB} has the expression:

$$I_{AB} = \frac{U_{Th}}{R_{AB} + R_{eq}}, \tag{3.10}$$

where $U_{Th} = U_{AB0} = U_{AB}|_{I_{AB}=0}$ is the voltage at terminals A, B of the active circuit, when $I_{AB} = 0$, and $R_{eq} = R_{AB0} = \frac{U_{Th}}{I_{ABsc}}$ the equivalent resistance of the passivated circuit in relation to terminals A, B ($I_{AB} = 0$). Applying the Kirchhoff theorems to the hybrid equivalent circuit in Figure 3.8, the result is:

$$\text{KCL: } I_{eq} = I_H - I_{AB} = I_H - \frac{U_{Th}}{R_{AB} + R_{eq}},$$

$$\text{KVL: } U_H = R_{AB}I_{AB} - R_{eq}I_{eq} = R_{AB}\frac{U_{Th}}{R_{AB} + R_{eq}} - R_{eq}\left(I_H - \frac{U_{Th}}{R_{AB} + R_{eq}}\right) \tag{3.11}$$

From equations (3.11) it follows:

$$I_H = I_{sc} - \frac{V_H}{R_{eq}} \text{ sau } U_H = U_{Th} - R_{eq} \cdot I_H, \tag{3.12}$$

where $I_{sc} = I_{ABsc} = \frac{U_{Th}}{R_{eq}}$. It turns out that here one source, U_H or I_H, can be selected arbitrarily, and the other source is determined by equations (3.12).

We must bear in mind that, like the Thévenin or Norton models, only two measurements are needed here to obtain all the parameters of the H~ model. For example, for

a selective value of current I_H and two measurements of voltage U_{Th} and current $I_N = I_{sc}$, equations $R_{eq} = U_{Th}/I_{sc}$ și (3.12) can be used to obtain the *resistance* R_{eq} and the voltage V_H for the model. Now, we consider two circuits (networks) N_1 and N_2 connected by port j (U_j, I_j), as shown in Figure 3.9 [1]. There are two types of H~ models for the linear (linear) circuit (network) with two terminals N_1. Model H~ of type 1 is shown in Figure 3.10 (a). To find this pattern, first open the port where $I_j = 0$. If we refer to Figure 3.10, a and consider the equation (3.12) is obtained:

$$U_j = U_H + R_{eq} I_N = U_{Th} \tag{3.13}$$

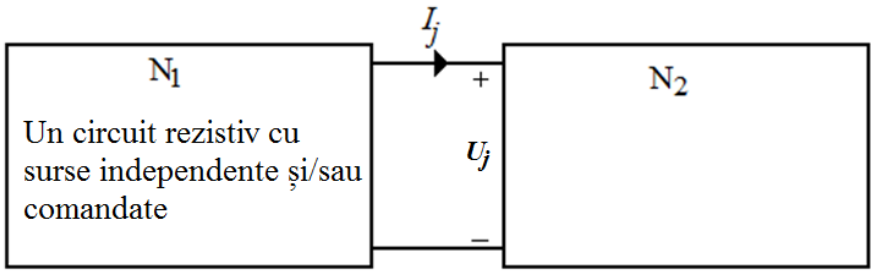


Fig. 3.9. Two circuits (networks) N_1 and N_2 connected by a port j (U_j, I_j).

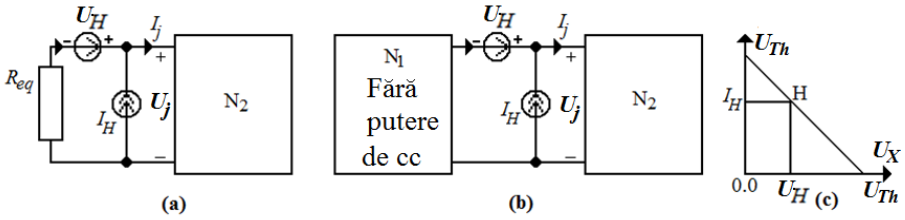


Fig. 3.10. A hybrid equivalent circuit with two terminals for circuit N_1:

a) Type 1 representation; b) Type 2 representation; c) Location on the characteristic curve of the port.

From equation (3.12) it follows:

$$U_H = U_{Th} - R_{eq} I_N = U_{Th} - R_{eq} I_{sc}. \tag{3.14}$$

However, the sources of model H~ of type 2 remain the same as those of type 1, but instead of calculating the equivalent resistance R_{eq}, we leave the N_1 circuit to remain unadulterated, except that all its DC sources are removed, as shown in Figure 3.10(b). The term "*DC power removed*" means that all dc-independent sources are removed from the N_1 circuit, including the charges on the capacitors and the currents through the coils. The type 2 H~ model is useful in a number of applications, such as moving DC sources from a circuit to its port-type terminals, without disrupting the internal structure (topology) of the circuit (network).

We must bear in mind that, due to the fact that it has two sources instead of one, an H~ model represents an axis of freedom that acts as a tool in the dynamic modeling of a port. As shown in Figure 3.10(c), a model H~- covers a full and continuous range of equivalent

circuits for a network with two terminals. It is evident from equation (3.12) and Figure 3.10 (c) that both the Thévenin and Norton models are two special cases of an H~ model.

3.3.1. Nullified hybrid equivalent circuit

A null (cancelled) hybrid equivalent circuit, called the H-model, is a special case of an H~-model; where, the values of the voltage and current sources in the model are identical to the corresponding values of the port voltage and current. This means that the sources in an H-model represent the polarization situation of the corresponding port. For example, we take the case from Figure 3.9, where the circuit (network) N_1 provides the voltage U_j and the current I_j to polarize the circuit (network) N_2. The two models for this example are shown in Figure 3. 18, (a) and 3.18, (b). Note that figures 3.18, (a) and 3.18, (b) are identical to figures 3.10, (a) and 3.10, (b), unless the model sources represent port values. We also note from figure 3.18 it is obtained, as a result of the modeling H, another port, *k* (U_k, I_k), is created on N_1, where both U_k and I_k are zero. Port *k* (U_k, I_k) is called *a "nullified" port*, and the process of creating it is called "port cancellation", as will be discussed below.

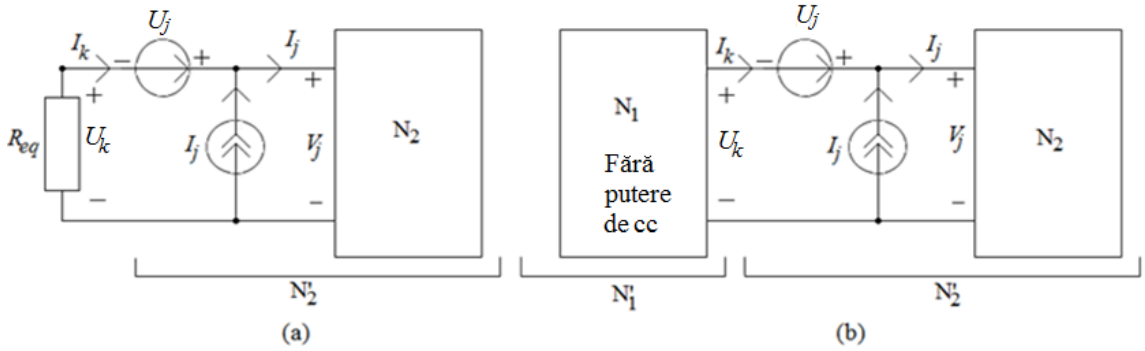


Fig. 3.18. An H model for a terminal N_1 with two terminals; a) Representation of type 1; b) Representation type 2, [1, 2, 15].

Theorem 1 introduces an important property of an H model that deals with the distribution of power in a network [1, 2, 15]. It adds additional dimension to the analysis and segmentation of power in a network.

Theorem 1: We consider a circuit (a network) N_2 connected (connected) to another circuit (to another network) N_1 through a port *j* (V_j, I_j), as in Figure 3.9. Replacing N_1 with model H of type 1 or type 2 reduces energy consumption to zero, while energy consumption in N_2 remains unchanged, [1, 2].

Demo: Consider the H~ model in Fig. 3.10, (a) or 3.10, (b). Both sources, I_H and V_H, provide power to the networks N_1 and N_2. The power delivered to the subcircuit N_2 is fixed and is calculated with the ratio $P_2 = U_j * I_j$; while in model H~ of type 1 the power consumed in subcircuit N*1* (Fig. 3.10, a) is $P_1 = R_{eq}(I_H - I_j)^2$. Therefore, the power P_1 in the subcircuit N_1 becomes zero if $I_H = I_j$, which also results in equality $V_H = V_j$. However, for model H type 2, we note from figure 3.14, (b) that the N'1 subcircuit has no DC source from which to obtain power, in addition its port is also nullified. Therefore, all currents and voltages inside the N'1 subcircuit must be zero, resulting in zero energy consumption.

Port cancellation: A circuit (network) N_2 connected to another circuit (to another network) N_1 via a port *j* (V_j, I_j) is taken into account, as shown in Figure 3.19. One way to cancel port *j* is to increase the port from both sides (N_1 and N_2) with current sources. I_j and voltage sources U_j as shown in Figure 3.18. The result is the creation of another port *k* (U_k, I_k) which, by definition, is a null port, i.e. both I_k and U_k are zero, [1, 2].

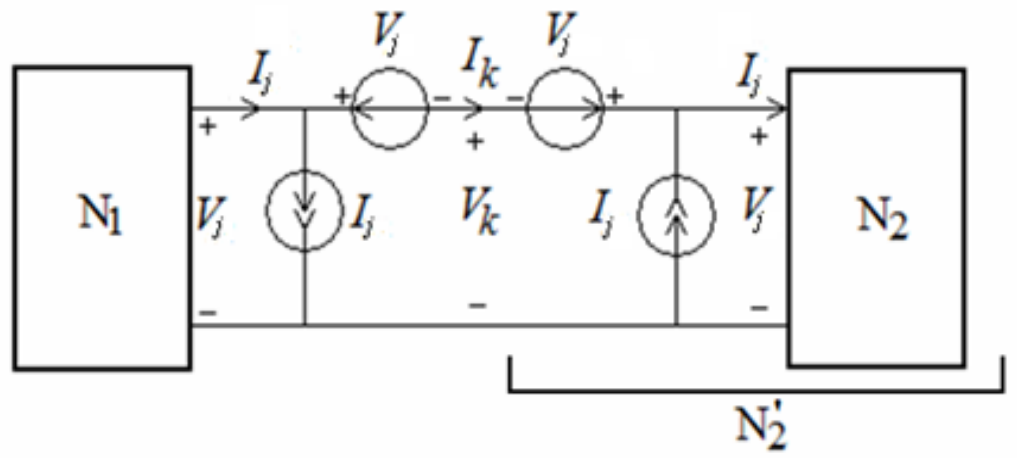


Fig. 3.19. A simple port cancellation procedure without any changes required N_1 or N_2, [1- 8,15].

However, there is an alternative method of creating a null port when two circuits (networks) N_1 and N_2 are connected by a port (through a gate) *j* (U_j, I_j), shown in Figure 3. 9. Here we can simply replace the N_1 circuit with its model H Type 1 or Type 2 and create the null port *k* (U_k, I_k), as shown in Figure 3.18. As a result of the nullified port procedure, shown in Figures 3.18 and 3.19, an extensive network, N'_2, is created, which contains the N_2 circuit and in addition contains the sources belonging to the model H. Similarly, another N'_1 network is created, on the left side, when the model H loses its sources. As we can see later, these extensive networks are of particular importance in the polarization of circuits. It should be noted that the characteristic curves of gates (ports) *j* and *k* are identical, with the exception of the displacements of *U* and *I*, the coordinate axes, from the origin to the point Q_j (U_j, I_j). This causes the operating point Q_j (U_j, ***Ij***) to move to the origin, creating a new operating point $Q_k(0,0)$ for port *k*, shown in Figure 3.20. This simply means that for any pair of networks, N_1 and N_2, connected by a j port, it is always possible to cancel the port and change the N_1 and N_2 circuits to the N'_1 and N'_2 circuits, where N'_1 and N'_2 are identical to N_1 and N_2 , with the exception of the coordinates axes *U* and *I* which are at the point of operation (operation of the port). This is mentioned in Property 1.

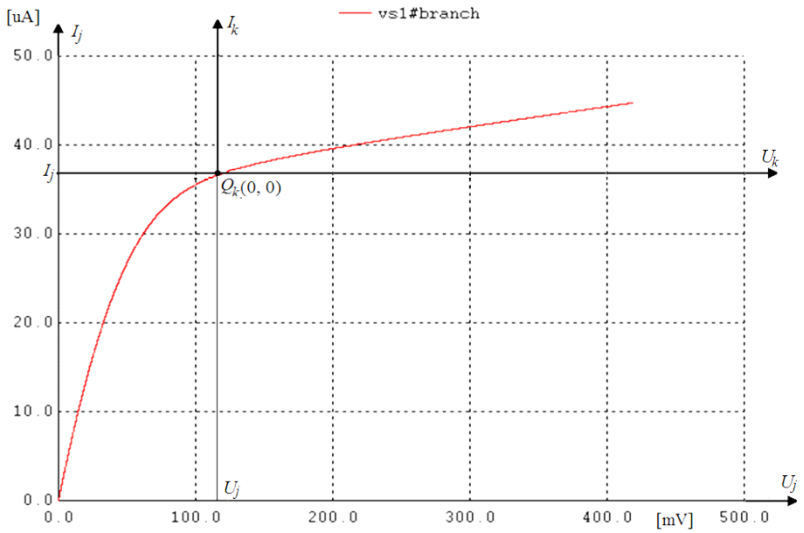


Fig. 3.20. The *I-U* coordinate axis has moved from (0, 0) for port *j* to a new position, Q*j*(U_j, I_j), for port *k*, [15].

Property 1: Either two circuits (two networks) N_1 and N_2 connected via a port *j*, as shown in Figure 3.9. If the port j is null, then the characteristic curve *I - U* of the port, viewed in relation to either of the two networks, passes through the origin, and the origin is the operating point of the port. If port *j* is not null, it is always possible to cancel the port in order to obtain the corresponding networks N'_1 and N'_2 with a zero port *k*, as shown in Figure 3.18, [1, 2].

Although the characteristic *I-U* curve of the port *j* (associated with both networks) does not pass through the origin, the one that port *k* does (property 1). In addition, point Q of port *k* is located at the origin, as expected. Note that: i) the N'_1 network, on the left, is still linear and ii) the new port *k* has a characteristic curve *I - U* passing through the origin, and the origin is also the point Q for the port. This simply means that the Thévenin equivalent circuit of N'_1, looking from port *k*, must be a resistance with no source attached.

4. CONCLUSIONS

The chapter presents the necessary and sufficient conditions to be satisfied by one-port linear circuits to be substituted for Thévenin, Norton, and Hybrid equivalent circuits. These circuits are widely used in the analysis of analog circuits. It is simply demonstrated, based on the superposition theorems, the Thévenin and Norton theorems.

The main value of Thévenin's theorem, as well as the Norton theorem, is that it allows us to replace any part of a circuit that forms a linear resistive port, a linear circuit in synnosoidal mode, or a linear circuit in operation (but not of interest in a given situation) with only two circuit elements without affecting the solution of the rest of the circuit.

A new modeling technique, called H~, is introduced for single-port networks. It is shown that H~ models are more dynamic compared to Thévenin or Norton equivalent circuits and have the ability to describe port behavior more accurately

Thévenin, Norton, and hybrid equivalent circuits are used in the construction of Nullified Hybrid equivalent circuits. Thévenin, Norton, hybrid, and zero hybrid equivalent circuits are used to locally polarize analog circuits.

Another objective of this work is to introduce a guided design procedure for polarization. Our strategy separates the linear and nonlinear portions of an analog circuit and takes more control over the nonlinear portions. This separation of portions (components) within the circuit is achieved by introducing a new port modeling that cancels the ports of nonlinear devices. This, in turn, leads to a new polarization technique for nonlinear components.

The use of Thévenin and Norton equivalent circuits in the simulation of nonlinear circuits with a small number of nonlinear circuit elements leads to a reduction in the calculation time and an increase in the accuracy of the results obtained.

The main value of Thévenin's theorem, as well as the Norton theorem, is that it allows us to replace any part of a circuit that forms a linear resistive port, a linear circuit in synnosoidal mode, or a linear circuit in operation (but not of interest in a given situation) with only two circuit elements without affecting the solution of the rest of the circuit.

4. NETWORK SWITCHING ANALYSIS WITH INCONSISTENT INITIAL CONDITIONS

4.1. INTRODUCTION

Circuits with topology controlled by switches containing semiconductor elements are of great interest in power electronics and communications. This domain includes both externally controlled circuits (i.e. by clock) and internally controlled circuits (i.e., by state). The modeling of switching circuits (circuits with switched capacitors or with switched circuits in current, DC-DC converters, switched modulators, etc.) with idealized models (elements in short circuit or in open circuit), very often leads to discontinuities of variables at switching times.

The details of the rapid changes of the signal during switching, provided by the complete models, are not relevant for circuit analysis, since the integration operations in those moments consume most of the calculation time [9, 10]. Accordingly, many tools for analyzing switching circuits consider idealized models of switches (short circuit or open circuit - empty) and treat the switch itself as an instantaneous event.

It is well known that this approach leads to circuits with excess storage elements and inconsistent initial conditions (CIIs) that in turn determine the discontinuity of network variables at times of switching. If we use ideal switches, we can overcome such a transition, but there are problems that arise from initial inconsistent conditions.

Modeling of switching circuits often leads to discontinuities of circuit variables at times when the switch changes state. This phenomenon is called with *initially inconsistent conditions* (CII), [1 – 13, 18, 19, 24].

The problem of the initial inconsistent conditions arises only for ideal circuit breakers, when, after switching, the circuit contains excess elements (loops consisting of independent and/or voltage-controlled capacitors or sources; nodes in which coils or independent and/or current-controlled sources meet), [1-17].

It is necessary to solve two major problems arising in connection with the initial inconsistent conditions, namely:

1. Find consistent initial conditions after switching to $\boldsymbol{t = t_{0+}}$, knowing the initial inconsistent conditions before switching to $\boldsymbol{t = t_{0\_}}$;
2. Calculation of the surfaces of Dirac pulses that occur at the time of switching.

Numerical, symbolic, and numerical-symbolic methods are used to find the correct initial conditions and to calculate the areas of impulses. For large circuits, the method of state variables [5] is not recommended.

If after switching the circuit has no excess elements and if the parameters of independent sources are known at any time in the time interval of interest, the condenser voltages and coil currents are continuous time functions. Therefore, the values of the state variables at t_{0-} and t_{0+} are the same and there is no inconsistency.

Recently, considerable attention has been devoted to the development of methods that conveniently deal with the problem of initial inconsistent conditions, [1-9, 12, 17]. Numerical, symbolic, or mixed analyses are used to find the correct initial conditions and to calculate the

areas of dirac pulses. Although the most commonly used method in the simulation of switching circuits is modified nodal analysis, the array method brings smaller numerical errors, while the method of state variables is considered less suitable for large circuits.

In the symbolic analysis of switching circuits, these problems were recognized and solved using the analytical approach, both in the time domain and using the Laplace transform.

In this chapter is presented a simple method for analyzing complex networks with switches considering that the ideal switch avoids these problems. This approach is based on the modified nodal analysis, when time-varying resistors are used to model ideal circuit breakers, as shown in Figure 4.1.. Switching duration $(t' - t_0)$ is considered less than or equal to the pitch size,[18].

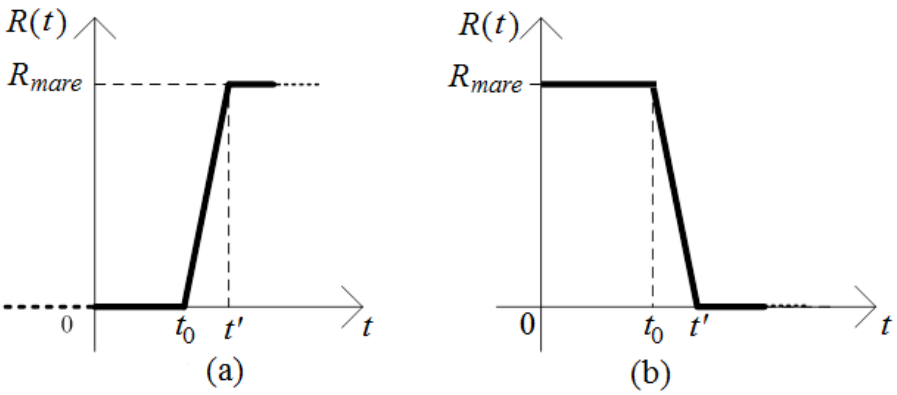


Fig. 4.1. Modeling of ideal switches by variable resistors:
a) Circuit breaker open at $t = t_0$; b) Circuit breaker closed at $t = t_0$.

For time analysis of electrical switching circuits, the default Euler medota can also be used. The switching time is considered to be t_0. In this way, the initial consistent conditions at t_{0_+} are automatically set in accordance with the initial inconsistent conditions at t_{0_-}. In order to calculate the dirac pulse areas for the condenser currents and/or the coil voltages, we have to multiply these variables by the size of the integration step *h*, at the times when the switches change their state.

The main topic of this chapter is related to well-formulated, but improperly excited circuits. This type of circuit has one of the following equivalent characteristics:

– They are not *excited per se*, not having classical solutions, for any classical excitation (their solutions contain distributions, generalized functions, such as Dirac impulses, when the excitations have discontinuities of time);

– Have *excess reactive elements* (first kind): C loops of capacitors and possible independent and/or controlled ideal sources of voltage and/or Lj inductor sets and possible independent and/or current sources;

– *Pathological circuits*, in which the state variables (inducing currents) and the voltages of the capacitors have jumps at the initial moment of time and, therefore, the energy balance is not observed.

The explanation for this behavior is the switching that occurs at the initial moment of time, which changes the topology of the circuit, causing the initial conditions not to conform to the Kirchhoff equations.

Before presenting the procedures used for the analysis of pathological circuits with inconsistent initial conditions, the essential elements for the analysis of analog circuits in the dynamic state are briefly presented.

4.2 SOME KEY ISSUES CONCERNING THE ANALYSIS OF ANALOG CIRCUITS IN THE TIME DOMAIN

4.2.1 Introduction

The state of operation in which the electrical circuit reaches a certain state of equilibrium, that is, its response has the same shape and variation in time as the applied excitation (input) quantities, is called *the stationary state*. Unlike resistors, coils and linear capacitors have characteristic time-dependent equations, so they are referred to as dynamic circuit elements. In circuits containing such elements, the stationary state is not established instantly, since it would involve a finite transfer of energy (accumulated in coils and/or capacitors) in a nil time, which is obviously impossible to achieve.

The operating equations of these dynamically elemental electrical circuits are obtained using Kirchhoff's theorems and the characteristic equations of the circuit elements that completely describe the behavior of the circuit. The presence of coils and capacitors in the circuit introduces into these equations terms containing derivatives from time, respectively integrals in relation to time:

$$i_C(t) = \frac{dq_C}{dt} = C \cdot \frac{du_C}{dt}, u_L(t) = \frac{d\phi_L}{dt} = L \cdot \frac{di_L}{dt}. \tag{4.1}$$

Therefore, the behavior of the circuit will be described by a system of integro-differential equations that are linear, inhomogeneous, with constant coefficients. This system can still be processed as a system consisting only of differential equations. By successive eliminations, this system can be reduced to a single differential equation of order *n*. Since only the coils and capacitors each introduce a differential element, and if the circuit does not contain excess elements [30] it follows that the *n-order* of the equivalent equation is equal to the sum of the number of coils*e* n_L and the number of capacitors n_C in the circuit. The solution of the differential equation of order *n* has the form:

$$x(t) = x_p(t) + x_t(t), \tag{4.2}$$

where: $x_t(t)$ is the general solution of the homogeneous equation (corresponding to the passivation of sources) and contains a number of constants of integration equal to the order of the equation. These constants are determined on the basis of initial conditions (values at the time t_0=0 or different from zero) which must be met by the complete solution and which refers to the initial values of the currents through the coils and to the voltages at the terminals of the

capacitors. This component is due solely to the accumulation of electromagnetic energy in the dynamic elements of the circuit and, consequently, its duration corresponds to the time interval necessary for the irreversible transformation of this energy into heat in the elements of the dissipator circuit. Since it is independent of the sources of excitation and its duration is limited, this component is called *a free* component or *a transient* component of the solution, and $x_p(t)$ it represents a particular solution of the inhomogeneous equation. Its corresponding expression is determined by the mode of variation in time of the function that represents the free term of the equation, corresponding to the excitation quantities that give this component; that is why this solution is also called *a forced* or *permanent component.*

The transient state occurs at the time *of* t_0 and is greatly influenced by the previous operating conditions of the circuit. In this state the free solution has important values in relation to the values corresponding to the forced solution.

Formulating the problem of initial conditions is necessary to determine the n integration constants of the transitional component. These constants are determined on the basis of the values at moment t_0 of some of the characteristic dimensions of the circuit, values that represent the initial conditions of the transient state.

Since it is the dynamic elements of the circuit that determine the integro-differential nature of the circuit equations, and the currents of the coils, respectively, the condenser voltages can be expressed using the following relationships:

$$i_L(t) = \frac{1}{L}\int u_L(t)\,dt = \frac{1}{L}\int_{t_0}^{t} u_L(\tau)\,d\tau + i_L(t_0), \tag{4.3}$$

respectively

$$u_C(t) = \frac{1}{C}\int i_C(t)dt = \frac{1}{C}\int_{t_0}^{t} i_C(\tau)d\tau + u_C(t_0), \tag{4.4}$$

it follows that these initial conditions refer to the initial values of the coil current and the condenser voltage. As a consequence, we have a total number of n_L+n_C initial conditions, necessary to determine all n constants of integration, it follows that these initial conditions refer to the initial values of the inductor and the capacitor. Consequently, we have a total number of n_L+n_C initial conditions, necessary to determine all n constants of integration.

For the case of real circuits, the values $i_L(t_0)$, respectively $u_C(t_0)$ are obtained from the state of continuity of the inducing currents and of the capacitor at the moment t_0:

$$\begin{aligned} &i_L(t_{0\_}) = i_L(t_{0+}), \text{ respectively } u_C(t_{0\_}) = u_C(t_{0+}) \text{ - for linear circuits,} \\ &\phi_L(t_{0\_}) = \phi_L(t_{0+}), \text{ respectively } q_C(t_{0\_}) = q_C(t_{0+}) \text{ for nonlinear circuits} \end{aligned} \tag{4.5}$$

If the needleis not imposed, at the time t_0, infinite variations in the coil voltages andcondensate currents will appear in the circuit.

Values $i_L(t_{0\_})$, Respectively $u_C(t_{0\_})$, are calculated from the stationary state prior to the transient state. For the case of idealized circuits with finite energy, used to emphasize only a

few important aspects of the behavior of such circuits, one can also imagine an ideal switching that can produce steep variations in the sizes i_L and u_C, thus infinite variations of the currents through the capacitors andof the voltages at the terminals of the coils . In this situation, the initial conditions are determined using the general total magnetic flux preservation theorem for each loop that does not contain any ideal independent and/or controlled current source and the total electric charge preservation theorem for each section (section surface) that does not contain any ideal source of independent and/or controlled voltage:

$$\sum_{l_k \in (b_h)}^{(A)} \left(L_k i_k(t_{0-}) + \sum_{\substack{s=1 \\ s \neq k}}^{l} L_{ks} i_s(t_{0-}) \right) = \sum_{l_k \in (b_h)}^{(A)} \left(L_k i_k(t_{0+}) + \sum_{\substack{s=1 \\ s \neq k}}^{l} L_{ks} i_s(t_{0+}) \right), \quad h = \overline{1,b'} \tag{4.6}$$

respectively,

$$\sum_{l_k \in (\Sigma_j)}^{(A)} C_k u_{Ck}(t_{0-}) = \sum_{l_k \in (\Sigma_j)}^{(A)} C_k u_{Ck}(t_{0+}) \quad j = \overline{1,n'}, \tag{4.7}$$

where b' - represents the number of loops that do not contain any ideal independent and/or controlled current source, and n' is the number of independent sections that do not contain any ideal independent and/or controlled voltage source.

These relationships result from the condition that the magnetic energy (electrical energy) accumulated in the magnetic field of the coils (in the electric field of condensatotheirs) has only finite variations.

4.2.2 Operational equations of linear electrical circuits

In order to formulate the equations of the circuit directly in algebraic form, avoidingthe formulation of the integro-differential equations, one can use, for the analysis of the electriccircuits e lineare in transient regime (in the time domain), the symbolic method of the Laplace transformation [11 – 13, 18, 30]. Next, it will be studied how transfomata Laplace affects the constituent relationships of the elements of the circuit.

For the linear resistor, the characteristic equation is $u_R(t) = R \cdot i_R(t)$. By applying the Laplace transform, the following relationship is obtained:

$$U_R(s) = R \cdot I_R(s). \tag{4.8}$$

The constitutive equation (characteristic), in variable mode, of a linear coil is $u_L(t) = L \frac{\mathrm{d}i_L(t)}{\mathrm{d}t}$ and by applying the derivative theorem in operational, the following are obtained:

$$U_L(s) = sL \cdot I_L(s) - Li_L(0_-), \tag{4.9}$$

suggesting a model in the field *of s* - consisting of an operational impedance sL in series with a voltage source of c onected value $Li_L(0_-)$as shown in Figure 4. 2. If the Laplace transform of the current is extracted from equation (4.9), it follows:

$$\boldsymbol{I_L(s) = \frac{U_L(s)}{sL} + \frac{i_L(0_-)}{s}},\tag{4.10}$$

suggesting a Laplace circuit equivalent to the current source connected in parallel with the operational admitance 1/ $i_L(0_-)/s$ sL (fig. 4.2).

For a linear capacitor, the variable-mode constituent equation is$i_C(t) = C \cdot \frac{du_C(t)}{dt}$. By applying the Laplace transform to this equation, one obtains:

$$I_C(s) = sC \cdot U_C(s) - Cu_C(0_-),\tag{4.11}$$

corresponding to the operational model in Figure 4. 3, with the current source in parallel with $Cu_C(0_-)$

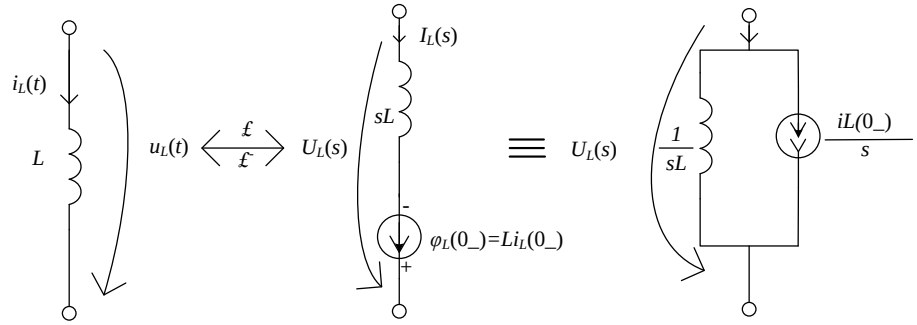


Fig. 4.2. Laplace models equivalent for an ideal linear coil.

$$\boldsymbol{U_C(s) = \frac{I_C(s)}{sC} + \frac{u_C(0_-)}{s}},\tag{4.12}$$

suggesting the alternating pattern with the voltage source in series with impedance $u_C(0_-)/s$ $1/sC$

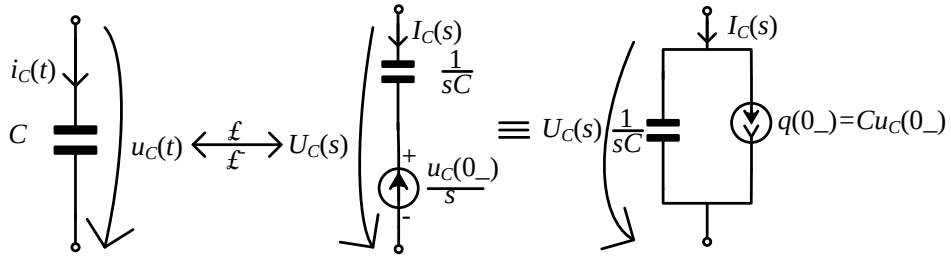


Fig. 4.3. Laplace models equivalent to an ideal linear capacitor.

For two magnetically coupled linear coils, the variable equations have the structure:

$$\begin{aligned} u_1(t) &= L_1 \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} + L_{12} \frac{\mathrm{d}i_2(t)}{\mathrm{d}t} \\ u_2(t) &= L_{21} \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} + L_2 \frac{\mathrm{d}i_2(t)}{\mathrm{d}t} \end{aligned}.\tag{4.13}$$

Applying the Laplace transform to equations (4.13) results:

$$\begin{cases} U_1(s) = sL_1I_1(s) + sL_{12}I_2(s) - (L_1i_1(0\_) + L_{12}i_2(0\_)) \\ U_2(s) = sL_2I_2(s) + sL_{21}I_2(s) - (L_2i_2(0\_) + L_{21}i_1(0\_)) \end{cases}. \tag{4.14}$$

4.2.3 Dirac impulse

Function defined by relationship $\gamma(t)$:

$$\gamma(t) = \begin{cases} 0 & for \quad t < 0 \\ 1 & for \quad t \geq 0 \end{cases}, \tag{4.15}$$

it is called *the unit step function* (*Heaviside function*). This relationship is the mathematical model of a signal that changes suddenly, for example by turning off a switch, and that is equivalent to the sudden application of a continuous signal. For a circuit with zero initial conditions $(u_C(0\_) = 0$ sau $i_L(0\_) = 0)$, the effect of applying the signal consists in introducing the response of the circuit to a continuous excitement to $\gamma(t)$sell the value equal to the unit.

If the signal is applied at the time $\tau > 0$, the following function is defined:

$$\gamma(t-\tau) = \begin{cases} 0 & for \quad t < \tau \\ 1 & for \quad t \geq \tau \end{cases}, \tag{4.16}$$

called *the phased unit step function (offset) with* τ. Functions $\gamma(t)$ and $\gamma(t-\tau)$ can be used for mathematical modeling of other discontinuous functions, such as impulses.

For example, the pulse function applied at the time $t = 0$ is obtained prin the overlap of a positive unit step function $\gamma(t)$ with a phase unit step function with τ negative $-\gamma(t-\tau)$, and the impulse function applied at the time $t = \tau$ results from overlapping the function $\gamma(t-\tau)$ with function $\gamma(t-\xi)$..

For $\tau \to 0\ (\xi \to \tau)$, so that the pulse area is equal to the unit, a *unitary pulse* is obtained or *the Dirac impulse*, denoted by $\delta(t)$.

Function $\delta(t)$ has a singularity in $t = 0\ (t = \tau)$, being zero for the rest of the range, i.e.:

$$\delta(t) = \begin{cases} 0 & for \quad t < 0 \\ \infty & for \quad t = 0 \\ 0 & for \quad t > 0 \end{cases}, \tag{4.17}$$

respectively

$$\delta(t-\tau)=\begin{cases}0 & for \quad t<\tau\\ \infty & for \quad t=\tau\\ 0 & for \quad t>\tau\end{cases}. \tag{4.18}$$

The function thus defined originates from the (in $t=\tau$) an infinite value, which is symbolized by an arrow, but is infinitely narrow, so as to ensure an area equal to the unit, so:

$$A_\delta=\int_{0_-}^{\infty}\delta(t)dt=\int_{0_-}^{0_+}\delta(t)dt=1. \tag{4.19}$$

At the same time, for everything $\tau\in[t_1,t_2]$, $0<t_1<t_2$

$$\int_{t_1}^{t_2}\delta(t-\tau)dt=\int_{\tau_-}^{\tau_+}\delta(t-\tau)dt=1, \tag{4.20}$$

changing the integration limits is possible because $\delta(t-\tau)$ is zero for all this range except for the moment $t=\tau$.

Taking into account the last relationship, it follows that for everything $\tau\in[t_1,t_2]$, $0<t_1<t_2$

$$\int_{t_1}^{t_2}f(t)\delta(t-\tau)dt=f(\tau). \tag{4.21}$$

Between the unit hatch function and the Dirac momentum there is the following relationship:

$$\delta(t)=\frac{d\gamma(t)}{dt}. \tag{4.22}$$

Therefore, the response of the linear circuit to impulse excitation can be determined by its response to stepped excitation, by derivation. The physical effect of signal application $\delta(t)$ consists in injecting an energy that induces the natural response of the circuit. The duration of the Dirac pulse occurs instantaneously in relation to the time constant of the circuit.

The two functions introduced in this paragraph allow the analysis in the time domain of a circuit in case the excitation signal has a variation in step or momentum time or, being determined experimentally, can be expressed by overlapping simple distributions. The circuit response is determined using the superposition theorem, by breaking down the input semnal into the ptaor momentum functions and knowing the circuit's response to such excitations.

4.3. DESCRIPTION OF THE METHOD

4.3.1 Introduction

In order to find the correct initial conditions and to calculate the pulse areas for the analysis of analog switching circuits (in switching), numerical, symbolic and numerical-

symbolic (mixed) methods are used. These methods allow to find the correct initial conditions and can calculate the areas of momentum. For large circuits, the methods of state variables are not recommended.

Numerical methods that preserve magnetic flux and electric charge, for example the default Euler Formula (EBF), are used to integrate equations of switching circuits, but the problem is given by how the integration stage should be controlled. The error of the EBF method increases as the integration time increases. When the step is too small, due to inconsistent initial conditions, the error may increase prohibitively. Modified nodal equations are commonly used to simulate switching circuits, but the array method brings in smaller numerical errors [1 – 29].

In this paragraph, the methods of numerical-symbolic analysis are introduced. The size of the integration pitch *h* is only a symbolic variable. This allows to detect the exact values of the Dirac pulses and calculates the initial conditions after switching avoiding errors of pure numerical methods. The algorithm, at all its stages, consistently processes only polynomials in *h*.

In practice, it has been found that the most effective method of modeling the states of circuits in the switch is their modeling by using open circuits (open state) and short circuits (closed state).

If the switch occurs to $t_0 = 0$, then, due to a possible change in the topology of the circuit, the values of the circuit variables at $t_0 = 0_+$, required by numerical procedures, may be different from those corresponding to the moment $t_0 = 0_-$. In this case, Impulses Dirac appear. A general solution for the circuit *x*(*t*) variable for $t \geq 0$, is as follows:

$$x(t) = \chi(t) + \alpha_0\delta(t) + \alpha_1\delta^{(1)}(t) + \cdots + \alpha_k\delta^{(k)}(t). \tag{4.23}$$

where $\chi(t)$ is *x*(*t*) for $t > 0$, and $\delta^{(l)}(t)$ is the derivative of the order *l* of the Dirac impulse.
It is assumed that the switching time is zero. The analysis of the time domain is valid. Two conditions are required that need to be solved for a correct integration of the circuit equations:

1. Determine whether or not pulses occur during switching;
2. Dermination of the initial conditions immediately after switching.

To meet these conditions apply semi-symbolic analysis. In circuit theory, the term semi-symbolic usually refers to the analysis in the frequency domain, when all the parameters of the circuit have numerical values except for the frequency which is considered to be the only symbol.

In the following, the word *semi-symbolic* refers to the analysis in the time domain when it is considered as a symbol only the step of integration *h*. The size of the time step by the nature of the analyzed circuit and the standard simulators of symbolic analysis have difficulties in solving the problems mentioned above.

For symbolic analysis, a general mathematical program can be used, but for the control of the solving process we must develop dedicated software.

The result of semi-symbolic analysis is a rational function of *h*. Semi-symbolic analysis would allow the detection of pulses in the circuit response (coefficients α_i from the equation 4.23), determination of the highest order *k* of the terms that depend on the impulse δ and the calculation of the initial condition at $t = 0_+$.

Unlike pure numerical methods, the semi-symbolic method is accurate and the only errors are due to the finite accuracy of the computer.

The switched circuits change their topology during switching and the previous results cannot be used to continue the calculation process. So, it is necessary to find a method of numerical integration that will restart during switching. Furthermore, the formula should be able to cope with inconsistent initial conditions. Two numerical methods are useful for this purpose. One of them - the Euler formula (EBF) is the simplest integration formula in the categories of the inverse method. The order of integration of this method is one and, accordingly, special precautions should be taken to cover all possible situations that may arise for switched networks. The advantage of EBF is that it can be used for both linear and nonlinear circuits. The second method is the Laplace numerical inversion, which is equivalent to a high-order integration method.

To calculate linear circuits with inconsistent initial conditions, one can use the modified nodal equation in the dynamic state (semi-state equations) in operational [11 – 13, 30], given the initial conditions of the moment.

The modified nodal equations have, operationally, the following matrix form, [12 – 30]:

where: $\boldsymbol{X}(s) = \begin{bmatrix} \boldsymbol{V}_{n-1}(s) \\ \boldsymbol{I}_m(s) \end{bmatrix}$- is the vector of independent variables in; *W* and *G* – have matrices with the dimensions (*n*-1+*m*)x(*n*-1+*m*) and $\boldsymbol{U}(s)$ represents the Laplace transforms (images) of the input size vector (excitation) $\boldsymbol{U}(s) = \begin{bmatrix} \boldsymbol{E}_{n_e}(s) \\ \boldsymbol{J}_{n_j}(s) \end{bmatrix}$. Matrix *B* is a selection matrix that has as elements (inputs) the numbers 1, 0 or 1.–

$$(\boldsymbol{W}s + \boldsymbol{G})\boldsymbol{X}(s) = \boldsymbol{B}\boldsymbol{U}(s) + \boldsymbol{W}\boldsymbol{x}(0_-) \tag{4.24}$$

According to the regressive Euler formula (with the default Euler algorithm) the first-order derivative in relation to time of the variable *x*, at the time $t_{j+1} = t_j + h$ (*h* being the step of integration), has the expression:

$$\dot{x}_{j+1} = \frac{x_{j+1} - x_j}{h}. \tag{4.25}$$

By replacing the first-order derivatives with the formula (4.25), with respect to time, the semi-state equations of a linear circuit are obtained from the semi-state equations of a linear circuit:

$$\left(\frac{\boldsymbol{W}}{h}+\boldsymbol{G}\right)\boldsymbol{x}_{j+1}=\boldsymbol{B}\boldsymbol{u}_{j+1}+\frac{\boldsymbol{W}}{h}\boldsymbol{x}_{j}. \tag{4.26}$$

The matrices corresponding to equation (4.26) are identical to those in equation (4.24), in which the variable *s* was substituted by the variable 1/*h*. If the formula (4.25) is applied to the calculation of the derivative of the unit step function for the circuit in Figure 4.5 (a), considering the time step consisted, h, the results shown in Table 1 are obtained.

Tabel 1

Time *t*	*h*	2 *h*	3 *h*	4 *h*	5 *h*	6 *h*
$v_1=\frac{\mathrm{d}\gamma(t)}{\mathrm{d}t}=\delta(\mathrm{t})$	1/*h*	0	0	0	0	0
$v_2=\delta^{(1)}(\mathrm{t})$	$1/h^2$	$-1/h^2$	0	0	0	0
$v_3=\delta^{(2)}(\mathrm{t})$	$1/h^3$	$-2/h^3$	$1/h^3$	0	0	0
$v_4=\delta^{(3)}(\mathrm{t})$	$1/h^4$	$-3/h^4$	$3/h^4$	$-1/h^4$	0	0
$v_5=\delta^{(4)}(\mathrm{t})$	$1/h^5$	$-4/h^5$	$6/h^5$	$-4/h^5$	$1/h^5$	0

The first derivative of the unitary step function, the Dirac pulse, is represented by an impulse of height of 1/*h* and the area equal to the unit. All derivatives of the high order have alternating signs. The coefficients of these derivatives have values such that the sum of their corresponding areas is always zero, and the numerical values of these coefficients are given by its coefficients $(1-x)^j$, where *j* is the order of the derivative. It is important to emphasize that after a number of steps, depending on the order of the derivative, the EBF (AEI) gives correct results. This value is not affected by consecutive steps. It implies that the even derivatives of Dirac pulses are treated correctly.

In certain situations, the initial conditions are required after switching. In principle, for these, there are two possibilities.

The first possibility is based on the observation that the Dirac impulse influences the result only at the moment *t* = 0. So, we can make the following assumption:

$$r_1=x(h)+\frac{a}{h};\ r_2=x(2h);\ r_3=x(3h), \tag{4.27}$$

where the contribution due to the Dirac impulse is expressed by the *a/h* function and the normal part of the result is marked by *x*(*ih*). The normal part can be further developed in taylor series, like this:

$$r(h+\tau)=x(h)+\tau x^{(1)}(h)+O(\tau^2). \tag{4.28}$$

Putting $\tau=h$ and keeping the first two terms from Taylor's series development, one can write:

$$r_1 = x(h) + \frac{a}{h};\ r_2 = x(h) + hx^{(1)}(h);\ r_3 = x(h) + 2hx^{(1)}(h)..\tag{4.29}$$

The value of unknowns at $t = 0_+$ is estimated as a Taylor series development with a nonnegative step out of the solution at the moment $t = h$.

$$x(0_+) = x(h) - hx^{(1)}(h) = 3r_1 - 2r_3.\tag{4.30}$$

The second possibility is given by the consideration of a progressive step, followed by the same regressive step that uses a negative step *h*. For small values of *h*, this method gives better results than the previous procedure.

Numerical methods use BEF at the same time as the Taylor series to find the initial conditions after switching. When using the first term in the Taylor series, the precision obtained is $O(h^2)$ and values $\hat{x}(jh),\ j = 1,\ldots,(k+2)$ are required to execute the algorithm. The method error is a function in *h* that is monotonous but has a fixed minimum. This behavior can be explained using network terms. The method uses a final generalization in the Taylor series and the sum of the currents for Kirchhoff's first theorem (TIK) or the sum of the voltages for Kirchhoff's second theorem (TIIK) are equal to the corresponding residual, but is not zero. The error of the method is: $\varepsilon/h + \gamma h^2$, with a minimum of $h = \sqrt[3]{\varepsilon/2\gamma}$. Constants ε,γ depend on the structure of the circuit, the type of equations and the type of variables. The calculation effort required to estimate these constants is too great for any practical purpose.

4.3.2 Semi-symbolic analysis of circuits with inconsistent initial conditions

Circuit elements such as linear resistors, linear coils, linear capacitors, current sources and voltage-controlled current sources that can enter directly into the formulation of the analysis are called circuit elements compatible with nodal analysis. When the circuit contains circuit elements that are not compatible with the nodal analysis, such as the ideal voltage independent sources, the voltage-controlled sources, the voltage controlled sources, the current controlled current sources, the magnetic couplings, these elements will be transformed into equivalent models that can be manipulated in the modified nodal analysis method [10,11-15].

The advantage of consistently using the same simple nodal formulation is affected by the need to transform the models efficiently. A different approach in solving the problem of admitting all the desired circuit elements is the modified nodal method. In this approach, the variables of the currents in the branches are introduced in addition to the variables of the voltages in the nodes. The basic principle regarding this approach is the use of the matrix of nodal conductances (admitances) for the circuit elements compatible with the nodal analysis and the magnification of this matrix with an extra line and column for each circuit element that is incompatible with the classical nodal analysis.

By replacing each capacitor, respectively each coil (magnetically coupled or not) by a discrete resistive circuit model associated with a previously chosen implicit numerical integration algorithm, the transient analysis of the linear dynamic circuit can be reduced to the analysis of a sequence of linear circuits, [14, 16].

For a linear circuit containing any type of independent or coupled circuit elements, the discrete resistive circuit equations associated with the regressive Euler formula at

$t_{k+1} = t_k + h$ (where *h* is the time step that does not have to be uniform) corresponding to the modified nodal analysis method, have the following form:

$$\begin{bmatrix} \boldsymbol{G}_{n-1,n-1}^{(k+1)} & \boldsymbol{B}_{n-1,m}^{(k+1)} \\ \boldsymbol{A}_{m,n-1}^{(k+1)} & \boldsymbol{R}_{m,m}^{(k+1)} \end{bmatrix} \begin{bmatrix} \boldsymbol{v}_{n-1}^{(k+1)} \\ \boldsymbol{i}_{m}^{(k+1)} \end{bmatrix} = \begin{bmatrix} \boldsymbol{i}_{sc,n-1}^{(k+1)} \\ \boldsymbol{e}_{m}^{(k+1)} \end{bmatrix}, \tag{4.31}$$

where: $\boldsymbol{G}_{n-1,n-1}^{(k+1)}$ represents the matrix of nodal conductances, including the conductors corresponding to the discrete resistive models of the dynamic circuit elements, corresponding to the *n*–1 independent nodes of the circuit;$\boldsymbol{B}_{n-1,m}^{(k+1)}$ is a matrix size (*n*-1)x*m* whose elements are: 1, 0, +1 and the current transfer factors (amplification) of current-controlled current sources– $\hat{j}_c(i_C)$; $\boldsymbol{A}_{m,n-1}^{(k+1)}$ represents a matrix size $m \times (n-1)$ containing the elements –1, 0, +1 and the voltage transfer factors (amplification) of the voltage-controlled voltage sources $\hat{e}_c(u_C)$; $\boldsymbol{R}_{m,m}^{(k+1)}$ is the square matrix *m*x*m* having the elements composed of: the transfer resistances of the current-controlled voltage sources $\hat{e}_c(i_C)$ and the resistances of the discrete models of the magnetically coupled coils; $\boldsymbol{v}_{n-1}^{(k+1)}$ is the vector of nodal voltages corresponding to the *n-1* independent knots; $\boldsymbol{i}_{m}^{(k+1)}$ represents the vector of the currents of the circuit elements (sides) incompatible with the classical nodal method and has, at the moment $t_{k+1} = t_k + 1$, the following structure:

$$\boldsymbol{i}_{m}^{(k+1)} = \left[\left(\boldsymbol{i}_{E}^{(k+1)} \right)^t, \left(\boldsymbol{i}_{E_c}^{(k+1)} \right)^t, \left(\boldsymbol{i}_{E_C}^{(k+1)} \right)^t, \left(\boldsymbol{i}_{j_C}^{(k+1)} \right)^t, \left(\boldsymbol{i}_{L}^{(k+1)} \right)^t \right]^t, \tag{4.32}$$

where: $\boldsymbol{i}_{E}^{(k+1)}$ is the vector of the currents of ideal sources independent of voltage; $\boldsymbol{i}_{E_c}^{(k+1)}$ is the vector of the currents of the controlled sides of all controlled voltage sources; $\boldsymbol{i}_{E_C}^{(k+1)}$ is the vector of the currents of the control sides of the voltage sources controlled in the current; $\boldsymbol{i}_{j_C}^{(k+1)}$ represents the vector of the currents of the control sides of the current controlled current sources; $\boldsymbol{i}_{L}^{(k+1)}$ is the vector of the currents of the magnetically coupled coils.

Vector $\boldsymbol{i}_{sc,n-1}^{(k+1)}$ - is the vector of the injected short-circuit currents at the time t_{k+1}, in those $n-1$ independent circuit nodes (including currents resulting from the simulation of coils and capacitors with discrete resistive circuit models), and $\boldsymbol{e}_{m}^{(k+1)}$– represents the vector corresponding to the t.e.m. of the sides formed only from ideal sources independent of voltage, at the time t_{k+1}.

In equation (4.31) the upper index represents the order of the time step.

For the numerical calculation of switching circuits, nodal equations modified in dynamic mode (semi-state equations) can also be used [10 13, 30]. If the default Euler algorithm is used for the numerical integration of the semi-state equations, with the integration step *h*, then the matrix form of these equations, corresponding to the moment $t_{k+1} = t_k + h$, has the structure of:

$$\begin{cases} \boldsymbol{W} \cdot \dfrac{\boldsymbol{x}^{(k+1)} - \boldsymbol{x}^{(k)}}{h} + \boldsymbol{G}\boldsymbol{x}^{(k+1)} = \boldsymbol{B}\boldsymbol{u}^{(k+1)} \\ \boldsymbol{y}^{(k+1)} = \boldsymbol{L}^t \boldsymbol{x}^{(k+1)} \end{cases} \tag{4.33}$$

in which: $\boldsymbol{x}^{(k+1)} = \begin{bmatrix} \boldsymbol{v}_{n-1}^{(k+1)} \\ \boldsymbol{i}_m^{(k+1)} \end{bmatrix}$- is the vector of independent variables at the time $t_{k+1} = t_k + h$ with the initial conditions $\boldsymbol{x}(0) = \boldsymbol{x}_0$; W and G - are array size (n-1+m)x(n-1+m), and $\boldsymbol{u}^{(k+1)}$ represents the vector of input quantities (excitation) $\boldsymbol{u}^{(k+1)} = \begin{bmatrix} \boldsymbol{e}_{n_e}^{(k+1)} \\ \boldsymbol{j}_{n_j}^{(k+1)} \end{bmatrix}$. Arrays B and L are selection matrices that have as elements the numbers: -1, 0 or 1.

Este evident că metoda nodală modificată, prezentată mai sus, acceptă și rezistențele variabile în timp care modelează întrerupătoarele ideale (fig. 4.1). Metoda nodală modificată a fost implementată într-un program de calcul numit ACAP - Analogue Circuit Analysis Program. Software-ul ACAP permite analiza circuitelor analogice liniare/neliniare, [10 13, 30].

4.3.3 *Examples*

Example 4.1*:* It is considered the circuit in the figure 4.4, (a) where $L_1 = 2$ mH, $L_2 = 1$ mH, $R_3 = R_5 = 1\ k\Omega$ și $E_4 = 2$ V. At the initial phase $t = 0$ currents i_1 and i_2 are: $i_1(0) = 0$, $i_2(0) = 0$. Then the circuit switches to phase 1, when the switch S_6 is closed (short circuit) and the switch S_7 it is open (open circuit). At the time $t_0 = 20\ \mu s$, the circuit switches to phase 2, the switch changing its state as in figure 4.4 (b). We will study the dynamic behavior of the circuit.

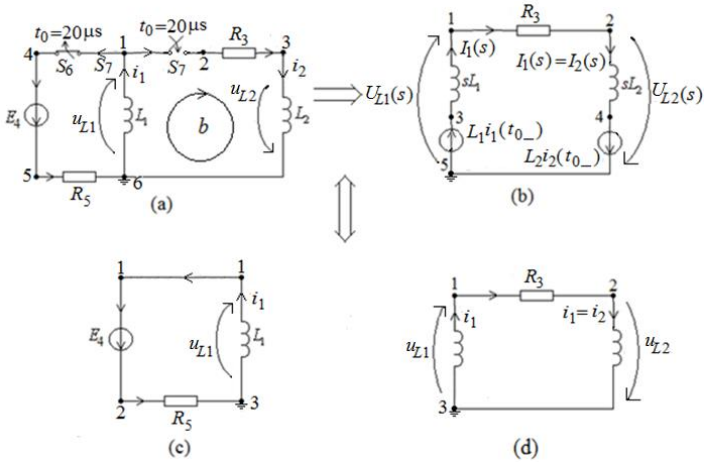


Fig. 4.4. a) The initial scheme of the circuit; b) Operational scheme of the circuit after the start of the transitional regime ($t \geq t_0$); c) Diagram of the circuit to the left of the circuit in figure 4.4, a with the intercartor S_6 closed and the circuit breaker S_7 open to be numerically analyzed for $t \in [0, 20\mu s]$; d) Diagram of the circuit on the right of the circuit in figure 3.4, with the intercarder S_6 open and the intercarrier S_7 closed, when considering the initial conditions at the time t_{0+}, to be numerically analyzed for $t \in [20\mu s, 40\mu s]$.

Numerical analysis:

Modified nodal equations corresponding to the step $t_{k+1} = t_k + h$ for this circuit are:

$$(n_1): \left[\frac{h}{L_1} + G_6(t_{k+1}) + G_7(t_{k+1})\right] v_1^{(k+1)} - G_7(t_{k+1}) v_2^{(k+1)} - G_6(t_k + 1) v_4^{(k+1)} = i_1^{(k)} \quad (4.34)$$

$$(n_2): \; -G_7(t_{k+1}) v_1^{(k+1)} + [G_3 + G_7(t_{k+1})] v_2^{(k+1)} - G_3 v_3^{(k+1)} = 0 \quad (4.35)$$

$$(n_3) \; -G_3 v_2^{(k+1)} + \left(\frac{h}{L_2} + G_3\right) v_3^{(k+1)} = -i_2^{(k)} \quad (4.36)$$

$$(n_4): \; -G_6(t_{k+1}) v_1^{(k+1)} + G_6(t_k + 1) v_4^{(k+1)} + i_4^{(k+1)} = 0 \quad (4.37)$$

$$(n_5): \; -i_4^{(k+1)} + G_5 v_5^{(k+1)} = 0 \quad (4.38)$$

$$(b_4): \; v_4^{(k+1)} - v_5^{(k+1)} = -E_4 . \quad (4.39)$$

By opening the switch and closing the switch at the time of S_6 S_7 $t_0 = 20\ \mu s$. The area of type *L* section, composed of coils and appears (figure 3.4, (b)). So the initial inconsistent conditions at L_1 L_2 $t_{0\_}$ are:

$$i_1(t_{0\_}) = \frac{E_4}{R_5} = \frac{2}{1} = 2 \text{ mA}, \qquad i_2(t_{0\_}) = 0 \text{ mA} \quad (4.40)$$

şi condiţiile iniţiale consistente the t_{0_+} they can be obtained by preserving the magnetic flux on the surface resting on the loop *b* (fig. 4.4 (a)).

$$L_1 i_1(t_{0\_}) + L_2 i_2(t_{0\_}) = L_1 i_1(t_{0_+}) + L_2 i_2(t_{0_+}) \quad (4.41)$$

with

$$i_1(t_{0_+}) = i_2(t_{0_+}) \quad (4.42)$$

From the relationships (4.11) and (4.12)

$$i_1(t_{0_+}) = i_2(t_{0_+}) = \frac{E_4}{R_5}\frac{L_1}{L_1 + L_2} = \frac{2}{1}\frac{2}{2+1} = \frac{4}{3} \text{ mA} . \quad (4.43)$$

First for the integration of equations (4.34) - (4.39), using the program ACAP (Analogue Circuit Analysis Program), [12, 30], for $t \in [0{,}40\ \mu s]$ with uniform pitch size $h = 0.2\ \mu s$, replace the two circuit breakers S_6 and S_7 with the models shown in figure 4.1 and considering $R_{ON} = 0\,\Omega$ and $R_{OFF} = 50\ \text{M}\Omega$. In Figure 4.5, the variations in voltages over time are obtained $u_{L_1\_1}(t) = u_1(t)$, $u_{L_2\_1}(t) = u_2(t)$ şi in Figure 4.6 variations in currents with time $i_{L_1\_1}(t) = i_1(t)$, $i_{L_2\_1}(t) = i_2(t)$.

Also, the circuit in figure 4.4(a) can be analyzed numerically, using the ACAP program, in two stages, as follows:

1. In the first step, numerically analyze, with the modified nodal equations method, the circuit in figure 4.4 (c), on the interval $t \in [0, 20\mu s]$;

1. Considering the initial conditions at the time t_{0_+} (relations (4.12)), calculate numerically the circuit in figure 4.4 (d).

Figure 4.5 shows the variations in voltages over time $u_{L_1}(t) = u_1(t),\ u_{L_2}(t) = u_2(t)$ and in figure 4.6 variations in currents in time $i_{L_1}(t) = i_1(t),\ i_{L_2}(t) = i_2(t)$.

Using the initial conditions at the time $t_{0\_}$, the circuit in Figure 4.4(a) can be analysed analytically, after triggering the transitional regime, and with the Laplace transform method. For this, the operational equivalent scheme in Figure 4.4(b) shall be used.

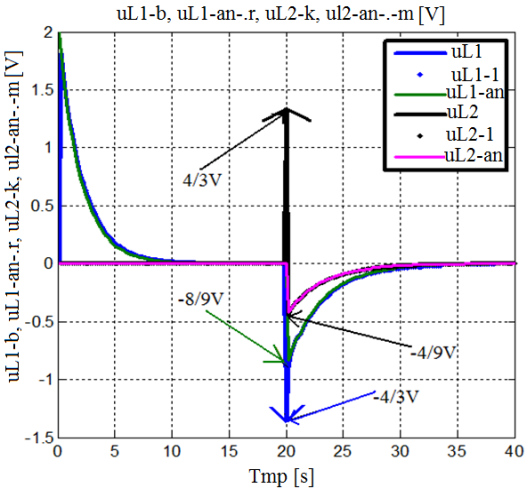


Fig. 4.5. Variations in voltages over time v_{L1} and v_{L2} (R_3 = 1kΩ).

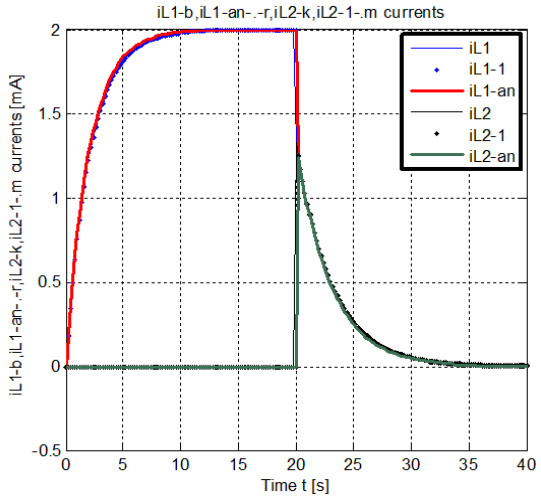


Fig. 4.6. Variations in currents over time $i_1 = i_1 = i_{L1}$ and $i_2 = i_{L2}$ (R_3 = 1kΩ).

Analytical solutions for coil currents and voltages for $t \geq t_0$ are:

$$i_{1\_an}(t) = i_{2\_an}(t) = \frac{4}{3}e^{-\frac{t-20}{3}}\text{mA}, \quad t \geq 20\ \mu\text{s} \tag{4.44}$$

$$u_{L_{1\_an}}(t) = u_{1\_an}(t) = -\frac{4}{3}\delta(t-20) - \frac{8}{9}e^{-\frac{t-20}{3}}V, \quad t \geq 20\ \mu\text{s} \tag{4.45}$$

$$u_{L_{2\_an}}(t) = u_{2\_an}(t) = \frac{4}{3}\delta(t-20) - \frac{4}{9}e^{-\frac{t-20}{3}}V, \quad t \geq 20\ \mu\text{s}. \tag{4.46}$$

For the three switching circuit analysis procedure in Figure 4.3, (a) variations in time of coil currents $i_{L_1}(t) = i_1(t),\ i_{L_2}(t) = i_2(t)$ and coil tensions $u_{L_1}(t) = u_1(t),\ u_{L_2}(t) = u_2(t)$ shown in Figure 4.5 and Figure 4.6 respectively.

It can be seen in figures 4.5 and 4.6 that the values of the coil currents obtained numerically are identical to those obtained analytically (4.14), and the coil voltages of the coils $t_{0_+}u_{L_1}(t),\ u_{L_2}(t)$ at the t_0 Dirac impulse in the range $-4/3\ V$ and $4/3\ V$, respectively the equations (4.15) and (4.16).

The energy balance of the circuit during its transition is checked:

$$W_{1_{10us}} = \frac{L_1\left(i_1(t_{0_+})\right)^2}{2} = \frac{16}{9}\mu J; \quad W_{2_{20us}} = \frac{L_2\left((t_{0_+})\right)^2}{2} = \frac{8}{9}\mu \text{J};$$
$$W_{1_{40us}} = \frac{L_1 i_{1_{40us}}^2}{2} = 0\text{J}; W_{2_{40us}} = \frac{L_1 i_{2_{40us}}^2}{2} = 0\ \mu\text{J}; \tag{4.47}$$

$$W_{R_3} = \int_{20}^{40} R_3\left(i_1(t)\right)^2 dt = -\left[1 \cdot \frac{16}{9} \cdot \frac{3}{1} e^{-\frac{(t-20.0)}{3}}\right]_0^{\infty} = \frac{8}{3}\ \mu\text{J};$$

$$W_{1\_20us} + W_{2\_20us} = W_{1\_40us} + W_{1\_40us} + W_{R_3} = 8/3\ \mu J.$$

The simple circuit in figure 4.4(a) after the moment $t \geq t_0$, it can be analyzed without any difficulty, both in the field of frequency and time. However, the difficulties have increased when the resistance *of* R_3 tends towards zero.

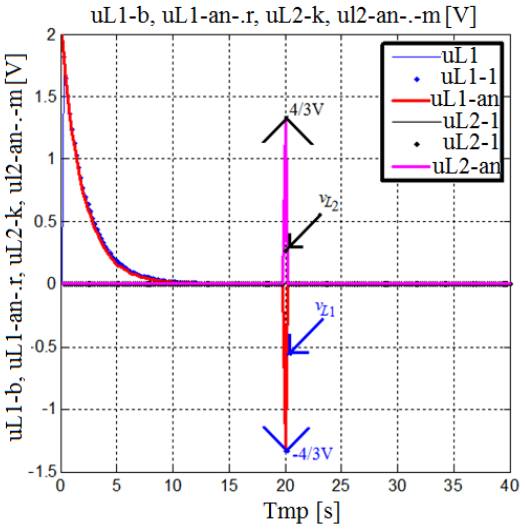


Fig. 4.7. Variations in voltages over time v_{L1} and v_{L2} ($R_3 = 0\Omega$).

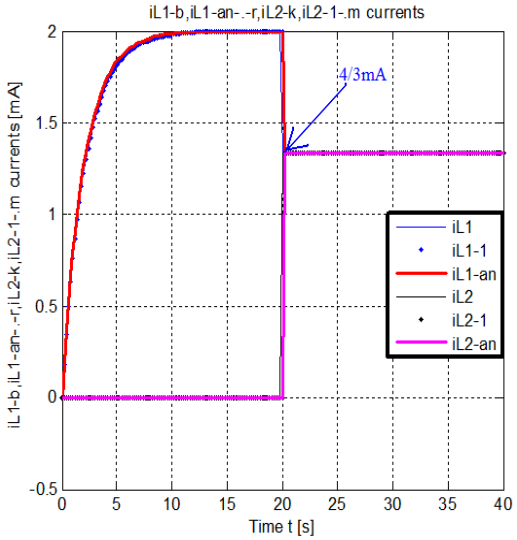


Fig. 4.8. Variations in currents over time i1 = i1 = iL1 and i2 = iL2 (R3 = 0Ω).

At the limit, a pathological circuit is obtained, having the coils connected both in series and in parallel, which means that they are in excess of both the first and second orders, [12, 13]. Operational equations, when $R_3 = 0.0\Omega$, of this circuit have the following solution:

$$I_1(s) = I_2(s) = \frac{L_1 i_1(t_{0-})}{s(L_1 + L_2)};$$
$$U_{L_1}(s) = I_1(s) \cdot (sL_1) - L_1 i_1(t_{0-}) = -\frac{L_1 L_2 i_1(t_{0-})}{L_1 + L_2}; \tag{4.48}$$
$$U_{L_2}(s) = I_2(s) \cdot sL_2 = \frac{L_1 L_2 i_1(t_{0-})}{L_1 + L_2}.$$

Asymptotic values have the following expressions:

$$\begin{aligned} &i_1(0_+): sI_1(s) = sI_2(s) \xrightarrow{s\to\infty} L_1 i_1(0_-)/(L_1+L_2) = -4/3\text{A}; i_{1\infty}: sI_1(s) \xrightarrow{s\to 0} 0; \\ &u_{1\infty}: sV_1(s) \xrightarrow{s\to 0} 0\text{ V}; \\ &u_{2\infty}: sV_2(s) \xrightarrow{s\to 0} 0\text{ V}. \end{aligned} \tag{4.49}$$

The solution in symbolic form, in the time domain, of the circuit in Figure 4.4(b) is:

$$\begin{aligned} &i_1(t) = i_2(t) = \frac{L_1 i_1(0_-)}{L_1+L_2} e^{-t/\tau};\ u_1(t) = -\frac{L_1 L_2 i_1(0_-)}{L_1+L_2}\delta(t) - \\ &-\frac{L_1^2 i_1(0_-)}{G(L_1+L_2)^2} e^{-t/\tau};\ u_2(t) = -\frac{L_1 L_2 i_1(0_-)}{L_1+L_2}\delta(t) + \frac{L_1 L_2 i_1(0_-)}{G(L_1+L_2)^2} e^{-t/\tau}, \end{aligned} \tag{4.50}$$

with $\tau = G(L_1+L_2)$ and $G = 1/R5$.

Considering the numerical values of the circuit parameters, the expressions (4.50) become:

$$i_1(t) = i_2(t) = -\frac{4}{3}e^{-t/3};\ u_1(t) = \frac{4}{3}\delta(t) + \frac{8}{9}e^{-t/3}; u_2(t) = \frac{4}{3}\delta(t) - \frac{4}{9}e^{-t/3}. \tag{4.51}$$

From the expression (4.51) we can note that at $t = 0_+$, both voltages $u_1(t)$ and $u_2(t)$ have Dirac pulses with areas of 4/3, while the currents are without such impulses. At $t = 0_+$, $u_1(0_+)$ = 8/9 V and drops exponentially to zero for high t , while $u_2(0_+)$ = -4/9 V and grows exponentially to zero.

This time, the energy balance(s) shall also be checked:

$$\begin{aligned} &W_{10} = L_1\left(i_1(0_+)\right)^2/2 = 16/9\text{ J};\quad W_{20} = L_2\left(i_2(0_+)\right)^2/2 = 8/9\text{J}; \\ &W_{1\infty} = L_1 i_{1\infty}^2/2 = 16/9\text{J}; W_{2\infty} = L_2 i_{1\infty}^2/2 = 8/9\text{J}; \\ &W_{10} + W_{20} = W_{1\infty} + W_{1\infty} = 8/3\text{ J}. \end{aligned} \tag{4.52}$$

The higher-order derivatives of the Dirac pulses can be generated using the circuit in Figure 4.9. If the capacitor capacities and transresistances corresponding to the current-controlled voltage sources are equal to the unit, then each voltage u^j is derived from the previous potential. If the input signal is the unit step function $\gamma(t)$, then $u_1(t) = \delta(t)$ - Dirac impulse, $u_2(t) = \delta^{(1)}(t)$ is derived by the order 1 of the Dirac impulse, and in general, $u_j(t) = \delta^{(j-1)}(t)$. Consequently, the circuit in Figure 4.9 can be used to calculate the higher-order derivatives of the Dirac momentum.

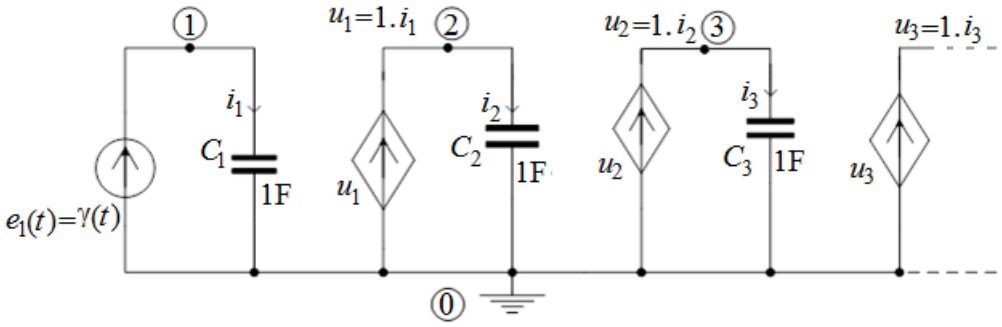


Fig. 4.9. The circuit that generates the sequences of the derivatives.

4.4 CONCLUSIONS

A very simple and very precise method of analyzing dynamic circuits with inconsistent initial conditions is presented. This approach is based on the modified nodal method, modeling the ideal circuit breakers through time-varying resistors having R_{ON} zero and R_{OFF} very high (much higher than the lowest resistance in the circuit).

Time-varying resistors have linear variation during switching $(t' - t_0)$ considered less than or equal to the size of the pitch.

The regressive Euler formula is used to integrate switching circuit equations. The switching time is assumed to be t_0 . In this way, the initial consistent conditions at t_{0_+} are automatically set in accordance with the initial inconsistent conditions at $t_{0\_}$. For the calculation of the dirac pulse areas for the condenser currents and/or the coil voltages, we must multiply these variables by the size of the integration step *h* at the time when the circuit breakers change their state, and after the switching the initial inconsistent conditions appear.

The analyzed circuit can be linear or nonlinear. In the case of a circuit with nonlinear elements there is a restriction: the circuit equations with nonlinear elements must be algebraic and the variables of these equations must not depend on impulses.

The described algorithm was implemented in the general program for rapid analysis of real switching circuits.

This chapter presents a simple and very precise method of analyzing dynamic circuits with inconsistent initial conditions (CII). The approach is based on modified nodal analysis, modeling the ideal switches through time-varying resistors with R_{ON} zero and R_{OFF} very high (much higher than the lowest resistance in the circuit).

Time-varying resistors have a linear variation during switching, and the duration of switching $(t' - t_0)$ is less than or equal to the size of the integration step. The Euler Regressive Formula (FRE) (the default Euler integration algorithm) is used to integrate equations of switching circuits. It is assumed that the switching time is t_0. In this way, the consistent initial conditions (CIC) at t_{0_+} are automatically set in accordance with the initial inconsistent conditions at $t_{0\_}$. For the calculation of the dirac pulse areas for the condenser currents and/or the coil voltages, we must multiply these variables by the size of the integration step *h* at the time when the circuit breakers change their state, and after the switching the initial inconsistent conditions appear.

The easiest method of analyzing linear circuits with excess elements and CII is based on the Laplace transform. This procedure has the advantage that it converts integro-differential equations into algebraic equations (in which the coefficients of algebraic equations contain the symbolic variable *s* (complex frequency)) and includes the initial conditions in the equations to be solved, implicitly treating them as independent sources. For the calculation of the dirac pulse areas for the condenser currents and/or the coil voltages, we must multiply these variables by the size of the integration step *h* at the time when the circuit breakers change their state, and after the switching the initial inconsistent conditions appear.

The easiest method of analyzing linear circuits with excess elements and CII is based on the Laplace transform. This procedure has the advantage that it converts integro-differential equations into algebraic equations (in which the coefficients of algebraic equations contain the symbolic variable *s* (complex frequency)) and includes the initial conditions in the equations to be solved, implicitly treating them as independent sources. Therefore, in the operational method, the circuit is considered not only in its transition over the time interval $(0, \infty)$, but also in its transition in (0-, 0+), in the vicinity of origin. Implicitly take into account the singularities that appear at t = 0.

As shown in work [1], if for the voltages of linear capacitors and for the currents of linear coils, the initial conditions at the time of the CII are considered to be automatically regularized. Therefore, the correct use of the initial conditions in the Laplace equivalent schemes of linear electrical circuits leads to minor risks in the analysis of these transient circuits. Because inconsistent initial conditions automatically adjust with this method, the risk of errors is generated by the wrong initial conditions. The operational representation of electrical circuits allows transient analysis, without any difficulty in both the (semi-)symbolic and numerical approaches.

For the analysis of static power converters, the technique of mediation of the state space was briefly presented.

The validity and effectiveness of methods for the analysis of CII pathological circuits and switching circuits are proven by the variety of circuits given as examples.

5. APPLICATION OF FIXATOR-NORATOR PAIRS IN THE DESIGN OF ANALOG CIRCUITS

This chapter describes a new theory of null modeling, based on active devices, from a circuit point of view. After a brief introduction about the concept of nulls and its properties, the modeling of active devices is presented not only for the voltage mode, but also for the current mode and for the mixed mode of operation using the topologies of circuits with two ports and four terminals. By simulating nullors through voltage-controlled voltage sources, $e_c = A_{c\_C}\, u_C$, with the control port an ideal independent power source, $j_C = i_C = 0.0$ A, and with the transfer factor (amplification) in voltage (voltage gain) A_{c_C} very high (theoretically infinite), analog circuits with nullors can be analyzed by using any of the existing simulation programs. Thus, all types of equations, which describe the behaviors of the circuit, can be formulated simply, regardless of whether the analyzed circuit contains nullors or not.

For the polarization of analog circuits, a different strategy was introduced. This paper introduces a new circuit element concept, the Fixator-Norator (PFN) pairs, which is the center of our strategy for designing the polarization of electronic circuits. Nullators and norators are used in pairs and are effective tools to perform effective polarization of electrical circuits. It is shown that these pairs are very useful in matching the critical polarization specifications with the input DC power.

These procedures can be easily implemented in dedicated programs for simulating complex analog circuits with nullors. We present some important examples that prove the validity of models for nullors.

5.1. INTRODUCTION

When using circuit models in the analysis of analog circuits, high-precision requirements can lead to complicated calculations, and therefore compact models are preferred during this process, mainly for the use of much simpler equations, [1 – 12]. These models are more efficient for optimizing the modeling and simulation time during the analysis process. From this point of view, nullors has already proven its effectiveness in modeling active devices. Also, in models based on the nullor element, all parasitic elements can be included to analyze their contribution to the analog circuit response [12 -21]. Nullors are very useful for modeling analog circuits because the topology of the circuit can be represented with components with two terminals, such as resistors (resistors), capacitors, nullators, norators and independent sources of voltage and/or current. It can also be pointed out that all controlled sources can be represented with equivalent circuits using nullors (nullor elements), [1 – 15]. Therefore, the system of equations, for the equivalent circuit based on the nullors (nullor elements), will be developed according to the classical method of nodal analysis. Nullor will be one of the basic components for models of active devices, given that the model must be developed in the simplest way, and the accuracy of the simulation of the circuit behavior must be within acceptable limits, [6, 11 – 17]. According to this approach, this chapter will present the problems related to the small signal models of the active devices that have been developed with nullors.

The nullator can be defined as an ideal two-terminal circuit, which is characterized by zero values for current and voltage, at the terminals. The symbol used for its graphic representation is shown in Figure 5.1,(a). For this type of circuits can be defined two relationships. The norator can be defined as an ideal circuit with two terminals (fig. 5.1(b)), which is characterized by random (arbitrary) values for current (i) and voltage (u) at terminals. Strictly speaking, the norator has no defined relationship. The current and voltage have values that are only affected by the external circuit that controls the norator.

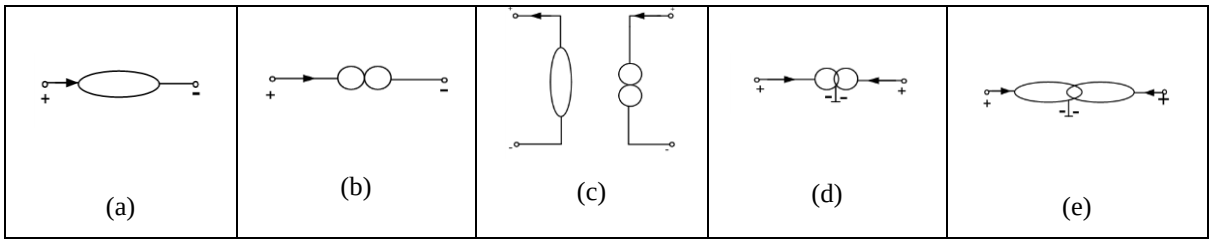


Fig. 5.1. a) The nullator symbol; b) The norator symbol; c) The symbol of the nullor; d) Current mirror; e) Voltage mirror, [1,2].

A nullator and a norator together form a deport circuit called nullor (fig. 5.1, (c)), which has the number of definition relationships equal to the number of gates.

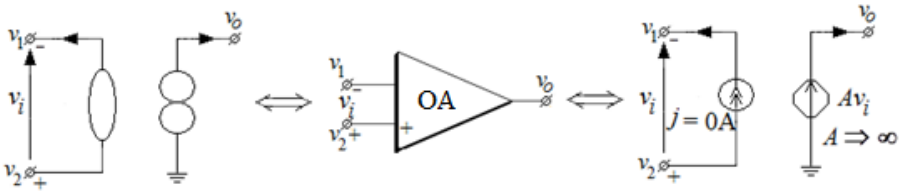


Fig. 5.2. Simulation of nullor by an ideal operational amplifier, [1,2].

The nullor is a two-gate circuit comprising a **nullator** as input **and** a **norator as** an output (fig. 5.1, (c))). The number of definition relationships for this circuit is the same as the number of its gates. Also, this type of circuits can be assimilated with an ideal operational amplifier for which the current is zero (an ideal independent source of current with $j = 0A$) and the output gate is simulated with an ideal source of voltage controlled by the input voltage with a very high (theoretically infinite) transfer factor (amplification) (fig. 5.2).

Theoretically, a **nullor** is just a two-gate circuit comprising a **nullator as** input and a **norator** as output (fig. 5.1, (c)).

The analysis and development of linear and/or nonlinear circuit (linearized in portions) were performed using the nullator and norator as active theoretical devices, [1 – 13]. Tellegen was the first to present the theory of the ideal operational amplifier, and later, in 1964, Carlin attempted to consider the nullators and norators as unique active devices in circuit analysis, [3, 4]. He believed that these active devices could not be physically built. Tellegen also took into account that these devices should only be regarded as mathematical models without any physical support. Again, Carlin proposed the combination of nullator and norator, which resulted in a useful physical device, nullor [4 - 21].

In [1, 2, 12] the behavior of nullators, norators and nullors in terms of voltage and current is presented, in G^u – voltage graph and, respectively, G^i - the graph of the current.
The input gate of the nullor is modeled by a nullator which is characterized by two equations:

$$u_1 = u_2 = \text{arbitrary}, \; i_1 = i_2 = 0. \tag{5.1}$$

So, the nullator is simultaneously an open circuit in the current graphG^i and a short circuit in the tension graph G^u. The output port of the nullor is shaped by a nullator, where it can be assumed that both voltage and current have arbitrary values:

$$u_1 \neq u_2 = \textit{arbitrary}, \; i_1 = i^2 = \textit{arbitrary}. \tag{5.2}$$

Fixator-norator (NFP) pairs are pathological components that help design analog circuits for a given specification set. It is important to note, however, that NFPs are temporary and do not remain in the circuit after the circuit is designed. Before we go through the design methodologies, we need to enter the NFP and its properties.

Fixator: A *fixator* is similar to a nullator, the difference lies in the fact that a fixator represents a fixed current source, respectively a fixed voltage source. In fact, a nullator can be considered as a special case of a fixator, when both current and tense are void. Figure 5.3 shows two versions of a fixator that depend on: (1) whether the voltage source U_j consumes (or supplies) power in the fixator and the current source I_j remains at rest or (2) when the power source I_j consumes (or provides) power in the fixator and the voltage source U_j remains at rest. In Figure 5.3, (a) the voltage source consumes energy and its symbolic representation is shown in Figure

5.3, (b). In Figure 5.3, (c) the power-consuming source is eliminated (omitted), and $Fx(0, I_j)$ is a *current fixator.* Figures 5.3, (d), (e) and (f) are similar to Figures 5.3, (a), (b) and (c), the difference is that the current source now consumes power and $Fx(U_j, 0)$ represents a *voltage fixator*.

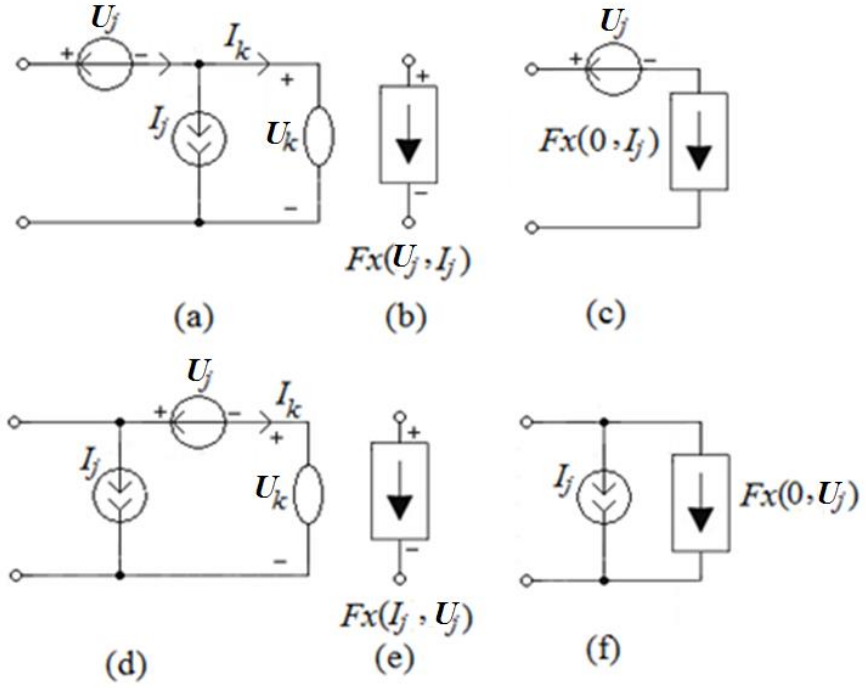


Fig. 5.3.Fixators: (a) and (b) The voltage-supplied fixator and its symbol; (c) The current fixator; (d) and (e) The current-supplied fixator and its symbol; (f) Voltage fixator, [3.5,13,22].

In a circuit, a fixator must always be paired (coupled) with a norator, since the fixator sets both port variables according to the design specifications, while the paired norator provides the required conditions for the fixator to work.

A fixator is a combination of a current source and a voltage source; therefore, the rules must be satisfied by both sources. For example, a serial current source with a fixator violates Kirchhoff's first theorem, a section of fixators with or without current sources can violate Kirchhoff's first theorem (TIK), and a loop of fixators with or without voltage sources can violate Kirchhoff's second theorem (TIIK). In a section of norators with or without current sources and fixators not all section elements are independent and on a loop of norators with or without voltage sources and fixators not all loop elements are independent.

From the above you can also deduce the following properties of fixators:

- A fixator $Fx(U, I)$ consumes power, and the power consumed has expresia $P = U*I$;
- An R resistance in series with a $Fx(U, I)$ is absorbed by the fixator and the fixator becomes $Fx(U_1, I)$; where $U_1 = U + R*I$. An R resistance in parallel with a $Fx(U, I)$ is absorbed by the fixator and the fixator becomes $Fx(U, I_1)$; where $I_1 = I + U/R$;
- A power source I_S in parallel with a fixatorr $Fx(U, I)$ is absorbed by the fixator and the fixator becomes $Fx(U, I_1)$; where $I_1 = I + I_S$;
- A voltage source U_S in series with a fixator $Fx(U, I)$ is absorbed by the fixator and the fixator becomes $Fx(U_1, I)$; where $U_1 = U + U_S$;
- A serial current source with a norator absorbs the norator without any change (modification); and a voltage source in parallel with a norator absorbs the norator without any change (modification). Additionally, a current source parallel to a norator is absorbed by the norator, and a voltage source with a norator is absorbed by the norator;
- A resistance in series or in parallel with a norator is absorbed by the norator;

- A serial norator with a fixator *Fx*(*U, I*) becomes a power source *I*; and a clouder in parallel with a fixator *Fx*(*U, I*) becomes a source of voltage *U*.

Now we have to show that a fixator cannot exist alone in a circuit. In general, any element (component) of the circuit is identified by its two variables, current and voltage. As a rule, a circuit element (component) specifies one of its two variables, the other variable is deduced from Kirchhoff's theorems (TIK and TIIK) in a circuit analysis. However, this is not the case with a fixator. Here, both variables are specified and the only way to be able to include them in a circuit is to find a component that does not have any of its variables specified. This component is a norator. This is why a fixator, like a nullator, must always be accompanied by a norator. We can think of this pair as an ideal controlled source, but there are major differences between the two. The gain or degree of dependence in a PFN is unlimited while in an ordered source it is limited.

The second major difference between the two is that in the case of multi-ordered sources, each pair of command source and commanded source must be specified in the circuit analysis, but this situation does not happen in the case of multi-fixator and multi-norator pairs. In the latter case, any pair works as long as the dependence (sensitivity) is valid.

As shown in [3-Esteban], in a related circuit a bipolar component is based on one of its two variables, and the other variable (voltage or current) results from the characteristic of the component. However, in the case of both variables of a fixator are specified by itself, and in the case of a norator both variables rely on the circuit to be specified. So, any pair of a fixator and a norator, as long as they are mutually sensitive, they satisfy the conditions for circuit analysis, it does not matter how they mate. It is summarised as follows:

The number of fixator must be equal to that of the norators; a norator must be sensitive (coupled) with at least one fixator and vice versa.

The following will show how the fixator-norator pairs are used in the correct polarization of electronic devices. The fixator will always be modeled in with the equivalent circuits shown in figures 5.3, (a) and (d), since the circuit elements existing in these circuits are accepted by most analog circuit simulation programs.

Next, we focus on designing polarization, focusing on individual devices. It shows how nonlinear devices, mainly diodes, BJT and MOS transistors, are linearly and nonlinearly shaped by fixators.

We will then cover the application of the NFP in the design of gains, input impedances and output impedances. One of the problems that we commonly face is when both polarization (cc) and performance (ca) models conflict with the values of some components of the circuit, usually resistances. The problem is how to assign two different values to a single component in two different cases. In integrated circuits the problem is solved by using current mirrors and active loads. Fixators and norators are used for the design of active tasks and current mirrors. These components are classified into three types, which are the types L, R and H for MOS transistors, as well as the same types for BJT in this paragraph. Design for analog VLSI circuits are also discussed. Again, PFNs are very essential in this app. The difference between the design for concentrated circuits and integrated circuits is clarified here. In circuits with concentrated parameters, polarization design and performance design is possible by using coupling capacitors and bypasses to separate the power and signal paths. Since this is not allowed in the design of integrated circuits (IC). The way we manage the separation of the two here is to use active tasks and current mirrors.

The following analysis is dedicated to the use of nullors in the design of bandwidth amplifiers. Because of the complexity and frequency dependency of the results, such projects should always be guided by a model circuit. It is assumed that this circuit model is given or built

synthetically to produce the desired output feature and the required bandwidth. The role played by a nullor here is double; one to make the circuit response follow the response in the model circuit and two, to make the necessary changes to adequately respond to the desired output feature. Since model circuits are for simulation purposes only, they can be built from ideal components such as ideal controlled sources and can even be built quite modularly.

There are numerous examples developed and simulated to support the theory.

5.2 FIXATOR-NORATOR PAIRS

Taking in considaration two circuits N_1 and N_2, connected by gate (U_m, I_m), as shown in Figure 5.4, (a). To cancel (repeal) the gate *m* (U_m, I_m), add to both sides of the two circuits sources of current and voltage with equal values, according to figure 5.4, (b), so that the gate *k* is a void gate. Now, since gate *k* is a void gate ($U_k = 0$ and $I_k = 0$) we can separate the two circuits and connect to each circuit a nullator, as shown in Figure 5.5. Obviously this operation does not affect (does not change) any current and no voltage inside the two circuits. In addition, the operating point of the *m* gate (I_m and U_m) was fixed so that whatever the internal changes inside the two circuits N_1 and N_2 were, a change in the Q operating point of the gate (the operating point of a device, also known as the polarization point). The operating point of a device, also known as a polarization point, quiet point, or Q point, is a stationary state (of DC) of the voltage or current of a specified terminal of an active device, such as a transitor to which no signal is applied. This allows us to substitute the m gate with a fixator.

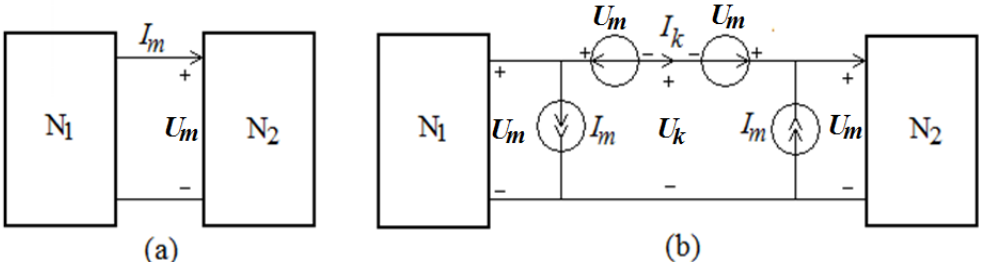


Fig. 5.4. Procedure to nullifie a gate, [12,13,22].

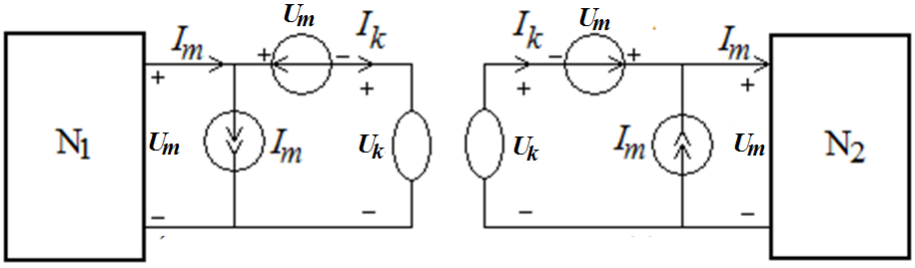


Fig. 5.5. Two circuits (networks) N_1 and N_2 disjointed at port k (U_k, I_k) and each completed by a nullator, [12,22].

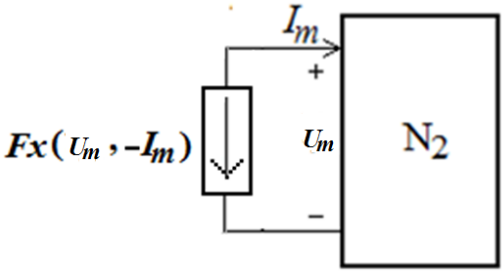


Fig. 5.6. Substitution of a fixator for the N_1 polarization circuit, [13, 22].

Property 1: A bipolar component, linear or nonlinear, in a circuit that is polarized by a current I and exposed to a voltage at terminals U can be replaced by an $F_x(I, U)$ fixator without causing any change in the currents and voltages inside the rest of the circuit.

An important conclusion from Property 1 is that fixators not only help to fix the technical specifications for polarization purposes, they also linearize a circuit by replacing all nonlinear components with fixators that are constructed of linear components. In addition, fixators increase the stability of the project by conducting a controlled approach (research) on design criterias.

Using fixators for the design and stability of the gate, we notice that for each fixator used we must have a norator in the circuit as a pair. It follows that fixator-norator pairs are an effective tool to perform the polarization procedure. This method shows how, by using fixator-norator pairs, we can solve the problem of distributed feeds, generated due to local polarization. In fact, it shows how a pair can be used to solve the design of polarization with a support power supply, and if the power supply is already specified in the project, the solution is an energy-conducting component. We must bear in mind that a fixator provides a solution and its norator pair finds, through analysis, the necessary resource for the solution. In this way, when used together, the pair will perform Kirchhoff's theorems. In short, when a polarization condition is required in a project, a fixator maintains this fixed condition and a norator provides, given in an arbitrary location, the source necessary for the requirement. This is, of course, only possible if the fixator can control the norator, and conversely, the fixator also has to react to changes in the norator. If a designated current source is already installed for the design, the norator can be placed at a designated location for a power-conducting component, for example a resistor, and then find the value by numerical resolution.

There is also another important interpretation of the fixator-norator pair. In general, each component of the circuit is identified by two variables, voltage and current. Of these, usually a single variable is specified, such as voltage in a voltage source or current in a current source; alternatively, the two can be linked as is the case with a resistor. This indicates that one of the two variables must be found from the Kirchhoff theorems, applied to the analyzed circuit. On the contrary, fixators and norators are different, that is, in a fixator both component variables are specified, but in a norator neither is specified. Therefore, none of them can be alone in a circuit; that is, when paired they complement each other; that is, in general, the two carry two specified variables and two are left for the circuit to find them. This behavior of the fixator-norator pairs suggests that the pair is no longer limited to DC operations and can be used in any operating mode of the circuit, including linear and AC circuits. So, we can conclude that in any type of circuit (linear or nonlinear) and in any mode of operation (DC or AC) some circuit variables can be fixed in exchange for values of the components. We can conclude that fixator-norator pairs change a circuit analysis procedure into a design procedure that meets certain design specifications, if possible. The reason is that in circuit analysis we are generally given all the values of the components and resources necessary to analyze a circuit; Whereas in a design procedure there are certain component values or resources to be determined in exchange for obtaining design specifications;

5.3 EXAMPLES

Example 5.1: To show how the process works, we start with a simple diode circuit shown in Figure 5.7, (a) with an unspecified supply voltage U_1. Suppose that the design requirement in this example is to find the value for U_1 so that the diode current is 1 mA.

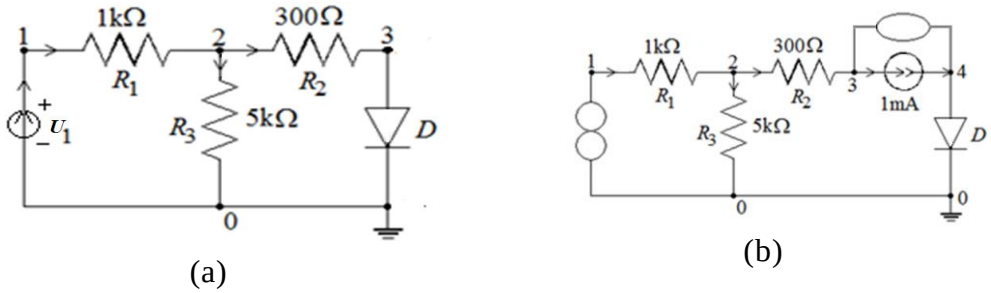


Fig. 5.7. a) A diode circuit with an unspecified supply voltage U_1; b) Arrangement of the circuit with diodes using a null to meet the design criteria I_D = 1 mA, [3, 5, 22].

Figure 5.7, (b) shows the circuit arrangement for this project using a fixator-norator pair to meet the design conditions. The added fixator - a current source I_D = 1 mA in parallel with a nullator forces the current assigned through the diode. Since the voltage on the current source is kept at zero, the added fixator has no effect on the overall operation of the circuit. A nullator is replaced by the unknown supply voltage U_1. We simulate the circuit and obtain a voltage of U_1 = 2.2 V on the norator with a current I_1 = 1.2 mA through it. This shows that although we have aimed for the voltage source U_1 to replace the norator, we still have two options to do: 1) we replace the norator with a current source I_1 = 1.2 mA, or 2) we replace the norator with a resistor $R_1 = -U_1/I_1 = -2.2/1.2 = -1.8$ kΩ. However, the last choice of a negative (active) resistance is not possible for the design.

We can observe that if we replace the power supply U_1 = 2.2V (or the current source I_1 = 1.2 mA) with a norator, the fixator-norator pair is removed from the circuit without influencing any changes in the operation of the circuit, that is, the current through the diode remains I_D = 1 mA. We note that in the case of replacing the norator with a current source I_1 = 1.2 mA, the operation of the circuit is not changed, but the circuit structure (topology) can be changed. For example, the resistance of 1 kΩ in series with the source becomes redundant and can be removed.

Next, we shall examine a third option. Suppose that the power supply in the original circuit, Figure 5.7, (a), is already assigned to U_1 = 2.5 V, but it is still necessary to have I_D = 1 mA, as a design requirement. This is the case that we have to decide on the value of a "power conductor" device. To continue, let's assume that the resistance R_2 is the "power conductor" device that we must adjust. We replace R_2 with a norator, figure 5.8, and simulate the circuit. As usual, we replace the norator with a voltage-controlled voltage source with the very high voltage transfer (gain) factor (STCT), which is controlled by the fixator. From the simulated results we get a voltage of U_2 = 1.0 V on the norator and a current of I_2 = 0.485 mA through it. This simply means that the choice is to replace the norator with a resistor $R_2 = U_2/I_2 = 2.09$ kΩ.

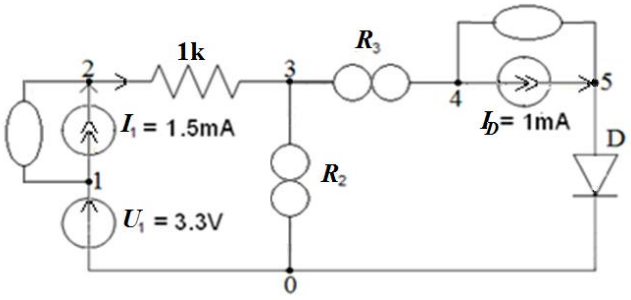


Fig. 5.8. Arrangement of the diode circuit using two pairs of nullors to meet the design criteria I_1 = 1.5 mA and I_D = 1 mA, [3, 5, 22].

Often, in a circuit, a norator with the calculated voltage U_1 and current I_1 can be replaced by: 1) a voltage source of U_1 volts, 2) a current source of I_1 amperes or 3) a component such as a resistor $R = U_1/ I_1$.

Before proceeding, we must realize that although our main use of fixator-norator pairs here is for polarization purposes, their application goes even further.

5.3 DESIGNING THE ORIENTATION OF ANALOG CIRCUITS

5.4.1 Introduction

A major step in the design of analog circuits is finding polarization points[1 – 3 – Esteban]. In large and complex circuits, polarization has always been a great challenge for designers. The problems are normally divided into two areas: firstly, in order to minimise the number of iterations and to make convergence possible and rapid; secondly, move to the correct operating regions for active components (transistors) so as to achieve acceptable performance and the output signals are far from distorted or cut during AC operation. Both problems increase in complexity as the number of transistors increases, the design requirements become stricter or more effective projects are in demand. A difficulty in the traditional approach seems to be the lack of separation between linear and nonlinear components, as well as between the nonlinear components themselves during the polarization process. Typical polarization techniques deal with the entire circuit as a whole, without classification or partitioning of the circuit; therefore, the complexity increases rapidly as the size of the circuit increases. In the case of analog integrated circuits, where almost all the components of the circuit are nonlinear, the distinction between linear and nonlinear components becomes meaningless. Instead, we can classify the components into two categories: 1) drivers and 2) support components. In the usual methods used for the analysis and simulation of analog circuits, all nonlinear components, regardless of their categories and functionalities, are included in a global polarization (cc) analysis. While, in more advanced methods, we can distinguish between drivers and those supporting components, such as current sources, current mirrors and active loads [4 - 6- Esteban]. Drivers are usually located along the path of the signal directly modeling the waveforms at the output. They strongly influence design specifications and are more sensitive to signal conditionings. Consequently, drivers must be biased with more care and accuracy compared to the supporting components in a circuit.

5.4.2 Application of fixator-norator pairs in the design of analog circuits

As can be seen from the previous paragraph, a fixator can model a device with two terminals for a fixed polarization condition. For example, for a diode polarized to (I_D, U_D), the fixator that replaces it is $F_x(I_D, U_D)$, where for positive I_D and U_D, the diode absorbs power. However, due to the fact that the device is not locally polarized (as discussed in the previous paragraph), it must receive energy from the sources in the circuit, that is, the global polarization. Property 1 can also be extended to include devices with multiple ports, such as bipolar transistors and MOS. In this case, for a polarization of a fixed component, the original component can be removed from the circuit and replaced with fixators that mimic the same polarization; therefore, it does not impose any changes for the rest of the circuit. In general, there are two types of fixator modeling for nonlinear devices. In the first type, called complete modeling, the component is removed entirely from the circuit and replaced by one or more fixators that represent the component with their intended polarization. In the second method, called partial

modeling, the component remains in the circuit, but one or more fixators maintain their fixed polarization to the specified values. We will discuss each type separately.

From Property 1 we can see that a device (or a circuit (a network)) with two terminals can be modeled by a single fixator. Similarly, for a device or network with several ports we can model each port separately with a fixator [19-Esteban]. In this way, an n-port device can be removed from a circuit and replaced by n fixators with the same currents and polarization voltages, without causing changes in the rest of the circuit. For example, a MOS device can be modeled completely using three fixators. Figure 5.9 shows the complete fixator patterns for nMOS and pMOS transistors, neglecting the substrate effects. Similarly, Figure 5.10 illustrates the complete fixator models for **npn** and **pnp** transistors.

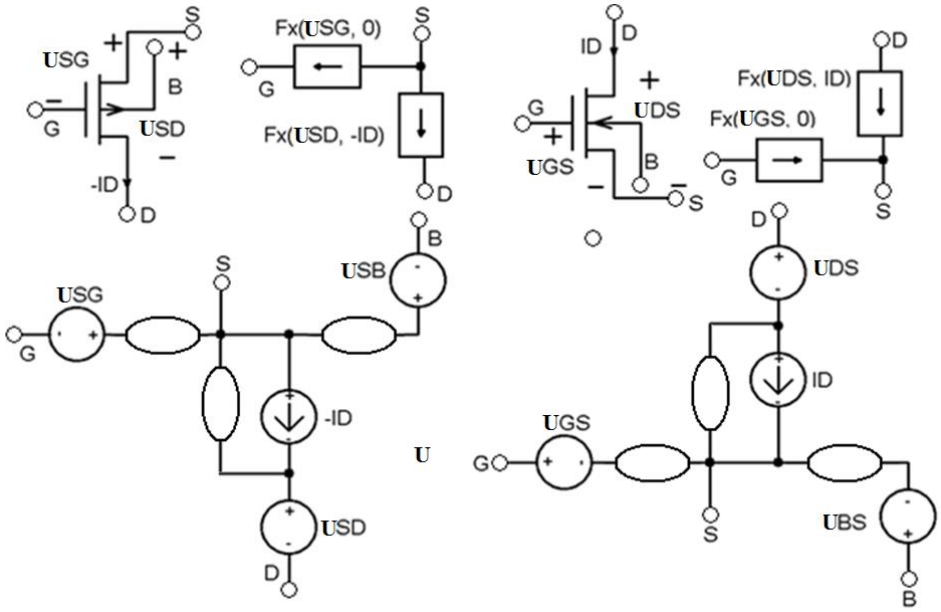


Fig. 5.9. Models with transistors fixators nMOS (a) and pMOS (b) when polarized globally for UGS, [12].

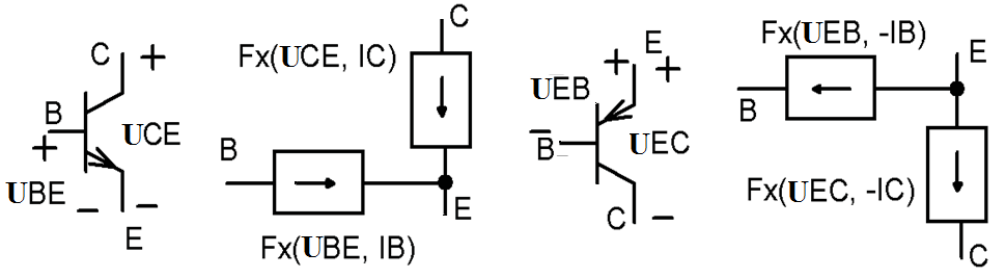


Fig. 5.10. Models with fixator for npn and PNP transistors when polarised globally for the UBE (UEB), THECE (UEC) and the IC [13].

Once again, the models represent devices with the same voltages (USG), UDS (USD), ID and UBS (USB). Both symbolic and developed (extended) versions are displayed, as well as the currents they need to be polarized at the specified Q points. Note that two changes occur in the circuit after the modeling is made: i) the resulting circuit becomes linear and ii) the circuit is frozen in direct current under fixed polarization conditions. What this means is that adding (or removing) any source or signal to the circuit may change the conditions of the signal in the circuit, but no change is required on the modeled transistors. Therefore, circuits with components modeled by fixators are not prepared for analysis in AC. An important property of a fixator is to keep the values fixed in DC (voltage and current) when assigned to a port in the circuit. We can use this property to polarize transistors in a circuit according to a specified operating point (Q). Figure 5.11 shows the polarization patterns of diodes, BJT transistors and

MOS using fixators. There are two types of models for each. Figures 5.11, (a), (c) and (e) show linearized patterns, while Figures. 5.11, (b), (d) and (f) show the current models with fixators. There are some important differences between the two. In the linearized model, we assume that both the voltage and the current for each port are known and correspond to the characteristics of the transistor. In this situation we are stuck with the type of transistor that is specified for the design, and if this transistor is replaced by another, with different characteristics, then the fixator model is no longer exact. On the contrary, the current transistor model specifies only one variable (voltage or current) for each port, and the other variable is found by the operation of the transistor and according to its characteristics. Therefore, any modification of the components of the circuit (including different transistors) will keep the polarization intact. However, the price we have to pay for using the real model is its non-linearity, which means that we must go through iterations when simulating the circuit.

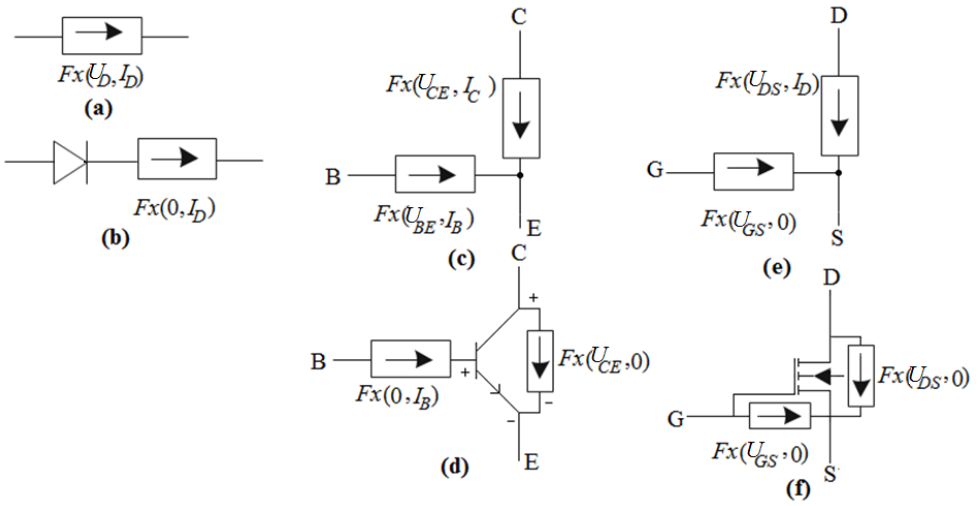


Fig. 5.11. Two types of polarization patterns; diodes a and b; c and d BJT transistors; e and f MOS transistors, [22].

Example 5.3: taking in consideration a three-levels BJT amplifier with reaction (feedback), shown in Figure 5.12, (a). The amplifier is broadband known as MC1553 [4-Fakfak]. It is assumed that all components of the amplifier are given, with the exception of resistors R_1 and R_7, which are kept unknown for polarization design purposes. There are two project (design) specifications to consider here. First of all, for proper operation of the amplifier with U_{CC} = 9 V, we must obtain a maximum variation in the output voltage close to 8 V; therefore, we assign U_{CE3} = 4 V. This is for the collector-emitter voltage of Q3. Secondly, we select to limit to I_{B1} = 10 μA, which is the base current of Q1. This current is almost half of the current passing through R_8 and is enough to provide a stable polarization condition for the first and critical stage of the amplifier. Figure 5.12, (b) shows the design configuration using two NFPs. Notice that the norators replace the unknown resistors R_1 and R_7.

In Figure 5.12,(c), the fasteners were replaced by their equivalent models in Figure 5.3 because the circuit components of these circuits are recognized by most simulation software.

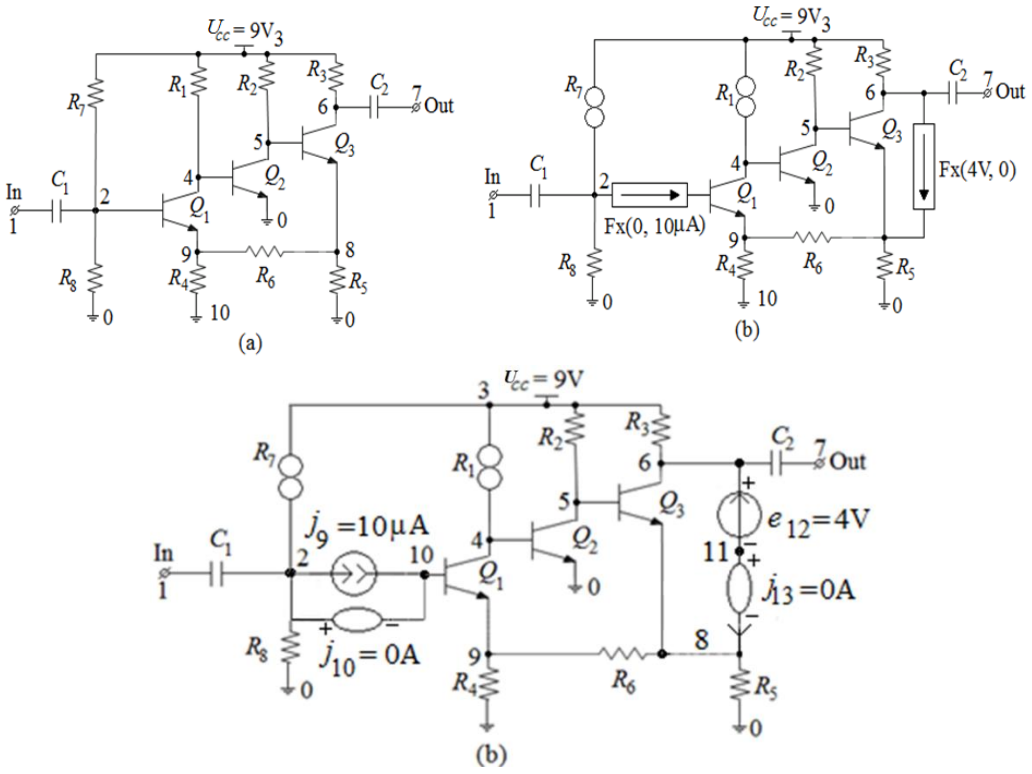


Fig. 5.12. BJT amplifier in three levels (steps) with reaction (feedback), known as MC1553: a) The original amplifier; b) Polarization design using PFN; (c) PFN are replaced by their equivalent schemes in Figure 5.3., [22].

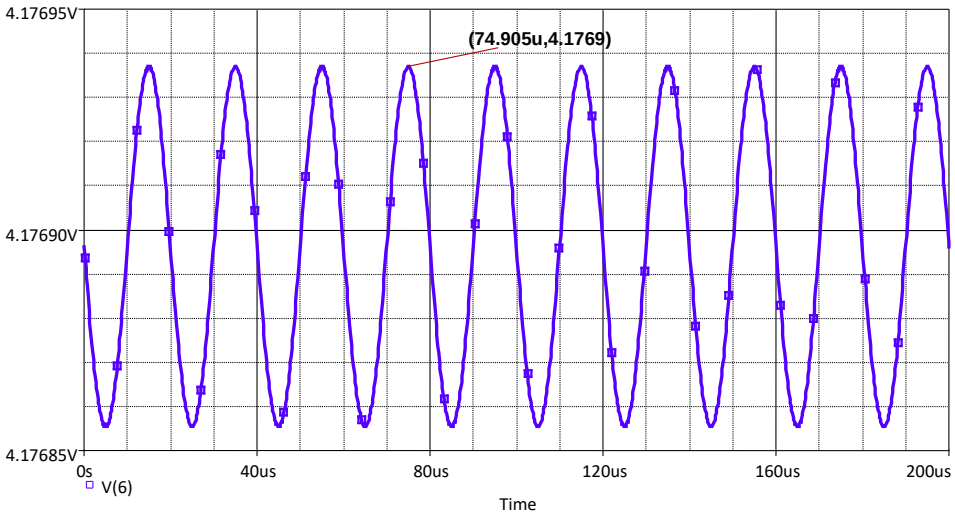


Fig. 5.13. The transient response of the amplifier in example 3, designed for polarization.

Simulating the circuit in figure 5.12,(c) with spice program we obtain the values for unknown resistances. The results obtained are: R_1 = 4.332/1.005e-03 = 4.232 kΩ, and R_7 = 4.077/1.0e-05 = 407.7 kΩ.

Our next step is to test the circuit thus designed. To do this, we remove the fixators, which means short circuit for F_x(0, 10 μA) and open circuit for F_x(4V, 0), and replace the norators (in Fig. 5.12, (c)) with R_1 and R_7 that have been found. Then we run the circuit for transient analysis, when $v_{in} = 0.6\,sin(2\pi 5.10^4 t)$. Simulation result is shown in Figure 5.13, which is almost without distortion.

5.5 DESIGNING INPUT AND OUTPUT GAINS AND IMPEDANCES

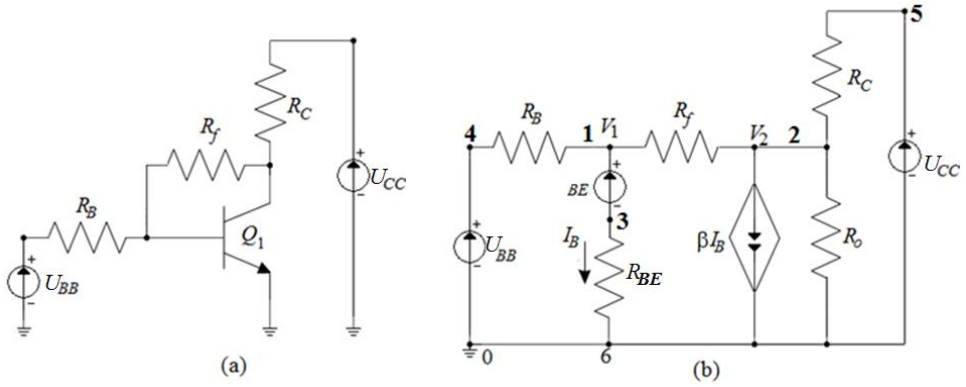
5.5.1. Fixator-norator pairs in a circuit

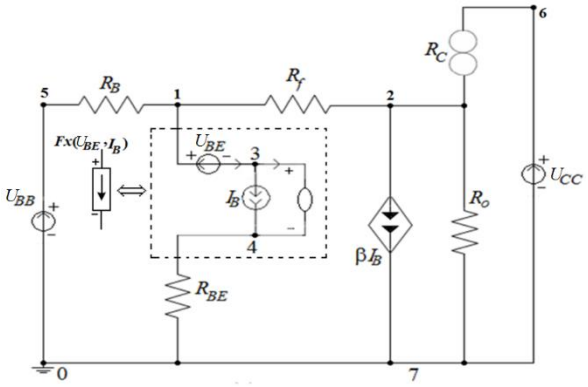
As mentioned earlier, one of the conditions for associating a fixator with a norator is that there is a reaction from the norator to the fixator. The purpose of this reaction is to harness the increase in voltage or current in the mating norator. In fact, because we simulate a fixator-norator pair with a voltage-controlled source with very high gain, the lack of reaction between them can cause serious instability and cause values to explode; that is, it can generate a voltage or current of very high value (negative or positive) at the norator location or elsewhere in the circuit. The only way to control this increase is to establish a reaction between the two in the pair. The following two examples show these reaction effects in the treatment of fixator-norator pairs.

Example 5.4: To see the reaction (feedback) effect between a norator and its pairing fixatorr, let's consider the polarization circuit of a BJT amplifier with a simple common reaction transmitter (feedback), shown in Figure 5.14, (a). In this example we assume that the transistor works linearly in its active region so that we can line the polarization circuit accordingly, as shown in Figure 5.14, (b). The common transmitter amplifier circuit with the fixator-norator pair is shown in Figure 5.14,(c), where the fixator-norator has been replaced by its equivalent circuit in Figure 5.3. Table 1 provides the component values for the linearized amplifier.

Table 1. Component values for linearized amplifier

U_{CC} V	U_{BB} V	U_{BE} V	R_B kΩ	R_{BE} kΩ	Ro kΩ	β
5	0.83	0.64	16.7	2	50	120





(c)

Fig. 5.14. a) The polarization circuit of a BJT amplifier with common jet transmitter; b) Linearized polarization circuit for amplifier; c) The joint transmitter amplifier circuit with the fixator-norator pair, [3, 5, 12].

Now in our first step we assume $R_C = 2$ kΩ and we do two experiments with this amplifier. In the first experiment we remove the feedback resistance R_f from the circuit (without reaction), and in the second experiment we assign $R_f = 200$ kΩ.

Table 2 provides the simulation results for the two experiments.

Table 2. Simulation results for the linearized amplifier

R_f kΩ	V_1 V	V_2 V	I_B μA
Open	0.6603	-13.8464	10.16
200	0.6455	-1.01526	2.745

In the next step we take the case with reaction ($R_f = 200$ kΩ) and try to find the power conductive resistance R_C for a fixed $I_B = 2{,}745$ μA. Figure 5.11 shows the circuit built for this situation. As shown, the F_x fixator (U_{BE}, I_B) is associated with the R_C norator. In Figure 5.11, the Fx fixator (U_{BE}, I_B) is replaced by its equivalent circuit in Figure 5.3, (a). The simulation results for this case provide $U_{RC} = 3.47412$ V and $I_{RC} = 1.71486$ mA, where the U_{RC} and I_{RC} are the voltage and current of the R_C norator. This brings us to $R_C = U_{RC} / I_{RC} = 2{,}026$ kΩ, as we expected.

Now we eliminate the reaction (feedback) and repeat the circuit simulation with a fixed $I_B = 10.36$ μA, which is slightly different from the previous value. This time, the simulation results become surprisingly different. We get $U_{RC} = 37.32$ V and $I_{RC} = 5{,}968$ mA, which are obviously not correct and are also unstable. Again, the reason for this instability and defective result is due to the lack of reaction (feedback) between the R_C norator and the F_x fixator(U_{BE}, I_B). That is, the current changes through the R_C and the voltage at its terminals are not "noticed" by the Fx control fixator (U_{BE}, I_B).

5.6 CONCLUSIONS

This chapter describes a new modeling of active devices based on nullors at the abstraction circuit level. Simulating the nullors with ideal voltage-controlled voltage sources, $e_c = A_{c\_C}\, u_C$, with the control gate an independent ideal current source, $j_C = 0.0$ A and with the transfer factor (amplification) in voltage A_{c_C} very high (ideally infinite), analog circuits with nullors can be analyzed with any of the existing simulation software. In this way, all types of equations that describe the operation of circuits can be easily formulated, regardless of whether the circuit contains nullors or not. For the polarization of analog circuits, a new strategy has

been introduced. This paper presents a new circuit element, *the Norator Fixator Pair (PFN*) (PFN), which is the main component in the polarization design strategy. Fixators and norators are paired as effective tools to perform a targeted influence on the analyzed circuit. It is shown that these pairs are very useful in matching the critical polarization specifications with the power resources in DC. In general, there are two types of fixators modeling for nonlinear devices. In the first type, called *complete modeling*, the component is removed entirely from the circuit and replaced by one or more fixators that represent the component with their corresponding (intentional) polarization. In the second method, called *partial modeling, the* component remains in the circuit, but one or more fixators maintain their fixed polarization to the specified values. In both cases, the PFNs are simulated with equivalent circuits containing (fig. 5.3) devices recognized by most analog circuit simulation software. The given examples certify the usefulness of fixator-norator pairs in polarizing analog circuits and in their optimal design.

The design tools and procedures introduced in this work are new and extensible. The proposed tools can be interpreted as the beginning of a new methodology in the design of analog circuits.

Local polarization minimizes DC consumption in the circuit. In general, the methodology can be used to monitor DC consumption in a circuit and direct it so that the power can be effectively reduced.

By using fixator-norator pairs, a circuit designer can specify and fix the design criteria (relevant to polarization) throughout the project. The pair also serves to locate and find values for voltage/current sources or components that conduct dc current.

All the proposed procedures can be easily implemented in dedicated programs for simulations of complex analog circuits with nulls. Many significant examples have been given that certify the validity of the proposed models.

6. FINAL CONCLUSIONS, CONTRIBUTIONS, FUTURE RESEARCH DIRECTIONS

The final chapter synthesizes the scientific activity carried out during the elaboration of this doctoral thesis, presenting punctually the conclusions and the results obtained. The chapter ends with a series of suggestions and recommendations on further research.

6.1. FINAL CONCLUSIONS

As a result of the accelerated development of computing techniques and of the increasingly advanced hardware and software equipment, the problems related to the design and analysis of electrical systems have largely moved from the test laboratory to the personal computer. The optimal sizing, stress tests, the degree of stress of some components, all these are currently carried out with the help of specialized programs that offer results and solutions in a short time and with material saving.

In this context, there is a need on the one hand to develop performing computing programs, often adapted to a certain category of problems, and on the other hand to develop models with a certain degree of generality, which would be easy to implement and that would offer results as close as possible to the real values, which would be obtained experimentally.

In the present PHD thesis there were presented advanced procedures for simulation and analysis of complex electronic circuits with nullities. New algorithms and computer programs dedicated to the analysis of analog circuits with nulls have been developed.

In Chapter 2, a new modeling of active devices based on nulls was presented after a brief description of the concepts of nullator, norator and nullor and their properties is passed to

the modeling of active devices not only to the voltage mode, but also to the current mode and to the mixed mode of operation from the point of view of the circuit with two ports and four terminals are described in some details.

For the simulation of the four biport-controlled sources with nullors and, in general, for the modeling of multiport circuit elements with equivalent circuit circuits formed by bipolar circuit elements and taking into account the behavior of nullors in terms of current and voltage, two graphs are associated, for the systematic formulation of Kirchhoff theorems, one *of* G^i current and another of G^u voltage . The two graphs have the same topology (the same number of: sides, knots and independent loops) and the sides are characterized by identical parameters, they differ in the positions of bipolar circuit elements (sides) simulating the four sources ordered by the carrier. Kirchhoff's first theorem and the equations of the bubble currents are formulated on the G^i current graph, Kirchhoff's second theorem, and the nodal (modified) equations are formulated on the voltage graph G^u, and in the characteristic equations (constituents) the currents (voltages) on the sides of the current (voltage) graph are used.

By simulating the nullators by ideal sources independent of current with the current intensity $j = 0$ A and of the norators with ideal voltage sources controlled in voltage $e_c(u_C)$ with the transfer factor (amplification) in voltage A with very high values (theoretically infinite), all types of equations, in any operating regime, can be formulated directly on the circuit with the nullors without the need for the graphs of current and voltage. The control voltages of the voltage sources controlled in the voltage are those from the terminals of the nullors – the nullors are biport circuit elements with the input side formed by a nullator, and the output side consists of a norator.

The examples presented in detail validate the models presented for analog circuits with nullors.

Chapter 3 presents the necessary and sufficient conditions to be satisfied by the linear one-port circuits to be substituted for the equivalent Thévenin, Norton and Hybrid circuits. These circuits are widely used in the analysis of analog circuits. It is simply demonstrated, based on the superposition theorems, the Thévenin and Norton theorems.

A new modeling technique, *called H~,* is introduced for single-port networks. A guided design procedure for polarization was introduced in the work. The developed strategy separates the linear and nonlinear portions of an analog circuit and takes more control over the nonlinear portions. This separation of portions (components) within the circuit is achieved by introducing a new port modeling that nulliffies the ports of nonlinear devices. This, in turn, leads to a new polarization technique for nonlinear components.

The use of Thévenin and Norton equivalent circuits in the simulation of nonlinear circuits with a small number of nonlinear circuit elements leads to a reduction in the calculation time and an increase in the accuracy of the results obtained.

In chapter 4 is presented a very simple and very precise method of analyzing dynamic circuits with inconsistent initial conditions. This approach is based on the modified nodal method, modeling the ideal circuit breakers by time-varying resistors having zero R_{ON} and R_{OFF} very high (much higher than the lowest resistance in the circuit.

The regressive Euler formula is used to integrate switching circuit equations. The switching time is assumed to be t_0 . In this way, the initial consistent conditions at are automatically set in accordance with the initial inconsistent conditions at t_{0_+}. For the calculation of the Dirac impulse areas for the condensator currents and/or the coil voltages, we must multiply these variables by the size of the integration step h at the time when the circuit breakers change their state, and after the switching the initial inconsistent conditions appear.

The analyzed circuit can be linear or nonlinear. In the case of a circuit with nonlinear elements there is a restriction: the circuit equations with nonlinear elements must be algebraic and the variables of these equations must not depend on impulses.

The easiest method of analyzing linear circuits with excess elements and CII is based on the Laplace transform. This procedure has the advantage that it converts integro-differential equations into algebraic equations (in which the coefficients of algebraic equations contain the symbolic variable *s* (complex frequency)) and includes the initial conditions in the equations to be solved, implicitly treating them as independent sources. Therefore, in the operational method, the circuit is considered not only in its transition over the time interval $(0, \infty)$, but also in its transition in $(0_-, 0_+)$, in the vicinity of the origin. Implicitly take into account the singularities that appear at $t = 0$.

As shown in work [1], if for the voltages of linear capacitors and for the currents of linear coils, the initial conditions at the time of the CII are considered to be automatically regularized. Therefore, the correct use of the initial conditions in the Laplace equivalent schemes of linear electrical circuits leads to minor risks in the analysis of these transient circuits. Because inconsistent initial conditions automatically adjust with this method, the risk of errors is generated by the wrong initial conditions. The operational representation of electrical circuits allows transient analysis, without any difficulty in both the (semi-)symbolic and numerical approaches. $t_{0\_}$

The validity and effectiveness of methods of analysis of CII pathological circuits and switching circuits are proven by the variety of circuits given as examples.

Chapter 5 describes a new modeling of active devices based on nulls at the abstraction circuit level. Simulating nullities with ideal voltage sources controlled by voltage, $e_c = A_{c\_C}\, u_C$, with the control gate an independent ideal power source, $j_C = 0{,}0$ A and with the voltage transfer factor (amplification) A_{c_C} very large (ideally infinite), analog circuits with nulls can be analyzed with any of the existing simulation software. In this way, all types of equations that describe the operation of circuits can be easily formulated, regardless of whether the circuit contains nullities or not. For the polarization of analog circuits, a new strategy has been introduced. This paper presents a new circuit element, *The Norator Fixator Pair – PFN* (*FNP*), which is the main component in the polarization design strategy. Fixators and norators are paired as effective tools to perform a targeted influence on the analyzed circuit. It is shown that these pairs are very useful in matching the critical polarization specifications with the power resources in cc. In general, there are two types of fixator modeling for nonlinear devices. In the first type, called *complete modeling*, the component is removed entirely from the circuit and replaced by one or more fasteners that represent the component with their corresponding (intentional) polarization. In the second method, called *partial modeling, the* component remains in the circuit, but one or more fixators maintain their fixed polarization to the specified values. In both cases, the NFPs are simulated with equivalent circuits containing (fig. 4.3) devices recognized by most analog circuit simulation software. The given examples certify the usefulness of fixator-norator pairs in polarizing analog circuits and in their optimal design.

Local polarization minimizes DC consumption in the circuit. In general, the methodology can be used to monitor dc consumption in a circuit and direct it so that the power can be effectively reduced.

By using fixator-norator pairs, a circuit designer can specify and fix the design criteria (relevant to polarization) throughout the project. The pair also serves to locate and find values for voltage/current sources or components that conduct dc current.

All the proposed procedures can be easily implemented in dedicated programs for simulations of complex analog circuits with nullors. Many significant examples have been given that certify the validity of the proposed models.

6.2 MAIN ORIGINAL CONTRIBUTIONS

In a society where computer technology and programs specialized in solving everyday problems are intensively used, the concerns related to the development of new models, performant methods of analysis and new procedures to model different linear and/or nonlinear analog circuits constitute a permanent activity. Electrical engineering could not be an exception. From the need to develop new equipment, to optimize the existing ones or to integrate them into complex systems, there was also the need to develop specialized programs that would solve these problems or at least ensure an optimal framework for carrying out high-performance specialized studies. One of the recent challenges is to develop simple models of electrical system components, so that they can be used easily and at any time to build more complex structures that want to be analyzed and improved. In this context, the topic addressed in this doctoral thesis represents a topic of interest for the engineering field.
The main original contributions made by the author in this doctoral thesis are:

1. The work begins with a carefully selected and up-to-date documentation regarding the analysis, modeling, simulation and design of linear and/or nonlinear analog circuits. It presents the main problems that occur in the simulation of complex analog circuits that in their composition a great diversity of electronic components. The methods of analysis, modelling, simulation and design of existing linear and/or nonlinear analog circuits and the most widely used computing programs shall be identified. The results are synthesized in a useful manner and thus constitute a useful tool for the development of further research in the field;

- The original implementation of some advanced methods of simulation and modeling of complex electronic circuits by using new simple circuit elements such as: nullators, noratos, nullors and pairs of fixators-norators;
- New and efficient procedures for adapting the existing simulation and analysis programs (SPICE, MAPLE, MATLAB, SYSEG, SYTFG, ECSAP, etc.), complex electronic circuits with nullors are developed;

1. Use of the equivalence of the four types of suse ordered with equivalent circuits consisting only of bipolar circuit elements and nullors in the symbolic or partial-symbolic calculation of the circuit functions for complex analog circuits;

- The successful use of all methods for the analysis of normal electronic circuits (the method based on Kirchhoff's theorems, the loop currents method, the classical node method, the modified nodal method, the state equation method and the method of semi-state equations) for the analysis of linear and/or nonlinear analog circuits linearized on portions with nullors was used. The variety as a structure of analog circuits with the analyzed nullities confirms the use of the use of nullors models of complex electronic devices;
- By modeling nullor amplifiers and then simulating norator by ideal current-independent sources with current intensity $j = 0$ A and norator with ideal voltage-controlled sources $e_c(u_C)$ with the transfer factor (amplification) in voltage A with very high values (theoretically infinite), allows systematic and particularly efficient analysis of practical complex circuits containing operational amplifiers;
- The necessary and sufficient conditions to be satisfied by the one-port linear circuits to be substituted for the equivalent Thévenin, Norton and Hybrid circuits are exposed. These circuits are widely used in the analysis of analog circuits. It is simply demonstrated, based on the superposition theorem, the Thévenin and Norton theorems;
- It introduces a new modeling technique *called H~*, for single-port networks. It is shown that H~ models are more dynamic compared to Thevenin or Norton equivalent circuits and have the ability to describe port behavior more accurately. A special type of H~ model, called the nullified H~ model, is also introduced, or simple model H; and many

properties of H-modeling, including power management in the circuit, are being investigated. A major property of H-modeling is the local polarization of transistors. Separates nonlinear components from the linear portion of the circuit for faster and more efficient polarization of the circuit. Here a designer can take advantage of H-modeling and the polarization of individual transistors (or in combinations) without having to perform normal circuit polarization;

- Develop a guided design procedure for polarization. The developed strategy separates the linear and nonlinear portions of an analog circuit and takes more control over the nonlinear portions. This separation of portions (components) within the circuit is achieved by introducing a new port modeling that nullifies the ports of nonlinear devices. This, in turn, leads to a new polarization technique for nonlinear components;
- It is shown how the equivalent circuits Thévenin, Norton and Hybrid can be used, with great success, in the simulation of nonlinear circuits with a small number of nonlinear circuit elements, This procedure leads to a reduction of the calculation time and an increase in the accuracy of the results obtained;
- In chapter 4 is presented a very simple and very precise method of analyzing dynamic circuits with inconsistent initial conditions. This approach is based on the modified nodal method, modeling the ideal circuit breakers through time-varying resistors having R_{ON} zero and R_{OFF} very high (much higher than the lowest resistance in the circuit);
- The implicit Euler algorithm is used to integrate the equations of the switching circuit. The switching time is assumed to be t_0 . In this way, the initial consistent conditions at t_{0_+} are automatically set in accordance with the initial inconsistent conditions at t_{0_-} . In order to calculate the dirac pulse areas for the condenser currents and/or the coil voltages, we must multiply these variables by the size of the integration step *h* at the time when the circuit breakers change their state, and after switching, the initial inconsistent conditions appear;
- The analyzed circuit can be linear or nonlinear. In the case of a circuit with nonlinear elements there is a restriction: the equations of the circuit with nonlinear elements must be algebraic and the variables of these equations must not depend on impulses;
- It has been assumed that time-varying resistors have a linear variation during switching, and the duration of switching $(t^{'} - t_0)$ is less than or equal to the size of the integration step. The Euler Regressive Formula (ERF) is used to integrate equations of switching circuits. In order to calculate the dirac pulse areas for the condenser currents and/or coil voltages, we must multiply these variables by the size of the integration step *h* at the time when the circuit breakers change their state, and after the switching the initial inconsistent conditions appear;
- It has been shown that the easiest method of analyzing linear circuits with excess elements and CII is based on the Laplace transform. This procedure has the advantage that it converts integro-differential equations into algebraic equations (in which the coefficients of algebraic equations contain the symbolic variable *s* (complex frequency)) and includes the initial conditions in the equations to be solved, implicitly treating them as independent sources. Therefore, in the operational method, the circuit is considered not only in its transition over the time interval (0, ∞), but also in its transition in (0_-, 0_+), in the vicinity of origin. Implicitly take into account the singularities that appear at $t = 0$;
- The correct use of initial conditions in the Laplace equivalent schemes of linear electrical circuits leads to minor risks in the analysis of these transient circuits. Because inconsistent initial conditions automatically adjust with this method, the risk of errors is generated by the wrong initial conditions. The operational representation of electrical

circuits allows transient analysis, without any difficulty in both the (semi-)symbolic and numerical approaches.

- For the analysis of static power converters, the technique of mediation of the state space was briefly presented.
- In order to highlight the validity and efficiency of the methods of analysis of the pathological circuits with CII and of the switching circuits, a large and diverse number, as a structure, of IIC electrical circuits were analyzed;
- Development of new methods of modeling active devices based on nullors at the level of the abstraction circuit. Simulating nullors with ideal voltage-controlled voltage sources, $e_c = A_{c\_C}\, u_C$, with the control gate an independent ideal power source, $j_C = 0{,}0$ A and with the voltage transfer factor (amplification) A_{c_C} very large (ideally infinite), analog circuits with nullors can be analyzed with any of the existing simulation software. In this way, all types of equations describing the operation of circuits can be easily formulated, regardless of whether the circuit contains nullors or not;
- For the polarization of analog circuits, a new strategy has been introduced. A new circuit element, the *Norator Fixator Pair –(NFP*), is presented, which is the main component in polarization design strategies. Fixators and norators are paired as effective tools to perform a targeted influence on the analyzed circuit. It is shown that these pairs are very useful in matching the critical polarization specifications with the power resources in DC. In general, there are two types of fastener modeling for nonlinear devices. In the first type, called *complete modeling*, the component is removed entirely from the circuit and replaced by one or more fixators that represent the component with their corresponding (intentional) polarization. In the second method, called *partial modeling*, the component remains in the circuit, but one or more fixators maintain their fixed polarization to the specified values. In both cases, the NFPs are simulated with equivalent circuits containing devices recognised by most analog circuit simulation software;
- The examples given certify the usefulness of the fixator-norator pairs in the polarization of analog circuits and in their optimal design;
- Local polarization minimizes DC consumption in the circuit. In general, the methodology can be used to monitor dc consumption in a circuit and direct it so that the power can be effectively reduced;
- By using fixator-norator pairs, a circuit designer can specify and fix the design criteria (relevant to polarization) throughout the project. The pair also serves to locate and find values for voltage/current sources or components that conduct dc current;
- All the proposed procedures can be easily implemented in dedicated programs for simulations of complex analog circuits with nullors. Many significant examples have been given that certify the validity of the proposed models.

6.3 FUTURE RESEARCH AND DEVELOPMENT PERSPECTIVES

Starting from the results obtained in this thesis, the following main directions of continuing future research can be identified:

- Adaptation of the software presented in the thesis to the current and future needs of engineering science related to the analysis of analog and digital circuits;
- Successful use of nullors and pairs of fixators-norators in the simulation of complex electronic devices in various operating modes;
- Introduction of new tools (computing tools) by circuit designers that allow them to understand and exploit the nonlinearity of circuits for the most useful processing;

- Extending the use of Thévenin, Norton and Hybrid equivalent circuits to multiport electrical circuit analysis;
- Elaboration of new methods of polarization of nonlinear circuits;
- Streamlining the methods of circuit analysis with inconsistent initial conditions;
- Studying the nonlinear behavior of the circuit in a graphical way, facilitating the development of a qualitative appreciation for nonlinear analog circuits.

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