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Doctoral School of Electronics, Telecommunications and Information Tehnology

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SUMMARY

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GALVANICALLY ISOLATED GATE DRIVER FOR POWER DEVICES

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Content

Chapter 1
Introduction

In recent decades, a global collaboration between governments and researchers is aimed towards reducing the dependence on fossil fuels and replacing them with alternative energy solutions. Energy conversion is possible using power semiconductor devices with advanced control mechanisms, which monitor the output and input parameters, and control the power switches accordingly.

Currently, the *Insulated Gate Bipolar Transistor* (IGBT) is the most widespread power device made of silicon. Its control is carried out by means of a gate driver that amplifies the control signal generated by a microcontroller to the levels of currents and voltages necessary for charging and discharging the input capacity of the switch. Another essential function of the gate driver is to separate the low-voltage range of the microcontroller from the high-voltage domain in which the switch operates.

Various errors can occur during normal operation of the system consisting of the microcontroller, the gate driver, and the IGBT, which can lead to exceeding the parametric limits of the components in the energy conversion chain.

The purpose of this work is to develop and implement a galvanically isolated gate driver for power devices, with robust data communication through the isolation barrier. The robust transmission of information from the input block to the output block, and vice versa, is ensured by designing and implementing an extensive set of protection circuits which prevent improper operation of the gate driver and of the power switch. The robust transfer of information is also ensured through three proposed new architectures that optimize the transmission paths by encoding and decoding error signals, and by improving *Common-Mode Transient Immunity* (CMTI) performances of the gate driver.

Chapter 2
Power Devices

An IGBT is used as a switch in power applications [1]-[3]. Thus, it operates in two regions, namely, cut-off or saturation. As a result, the term conduction for IGBT refers to the saturation region. When the IGBT switches on, a current overshoot occurs, $I_{C,MAX}$, expressed in (2.1), which is dependent on the current through the load, I_L, the charge stored in the freewheeling diode, Q_{RR}, and the dI_C/dt slope of the collector current [3][4]. Similarly, at turn-off, a voltage overshoot is induced, $V_{CE,MAX}$, described in (2.2), which is determined by the supply voltage of the load, V_{VCC}, the value of the inductive load, L_S, and the dI_C/dt slope [3][4].

$$I_{C,MAX} = I_L + I_{RR} = I_L + \sqrt{Q_{RR}\frac{dI_C}{dt}} \tag{2.1}$$

$$V_{CE,MAX} = V_{VCC} - L_S\frac{dI_C}{dt} \tag{2.2}$$

The dI_C/dt slope of the collector current depends on the I_G current provided by the gate driver for charging and discharging the input capacity of the IGBT. I_G is controlled by means of the internal resistance of the gate driver, R_G.

The IGBT is maintained in the *Safe Operating Area* (SOA) by reducing the dI_C/dt slope during switching processes. This effect is achieved through an external resistor, R_{EXT}, connected in series with the parasitic resistor of the gate driver, R_G. The disadvantage of the external resistance lies in the increase of the switching times, and implicitly, the increase of power losses.

An IGBT exhibits significant power losses during the switching process [1]-[3]. In order to minimize the power losses during this process, the parasitic resistance R_G of the gate driver must be as low as possible, resulting in fast dI_C/dt. However, modifying the dI_C/dt slope also influences $I_{C,MAX}$ and $V_{CE,MAX}$. For fast dI_C/dt, the resulting current and voltage overshoots can lead to the IGBT operating outside SOA. Therefore, the power switch can be thermally destroyed.

Thus, the control of an IGBT implies a compromise between the current and voltage overshoots, and the power losses that occur during the switching processes.

In typical IGBT applications, certain operating conditions impact the overshoots on the I_C current and on the V_{CE} voltage [3]. The extent to which these parameters are influenced may lead to the power switch working outside the safe operating area. As a result, current gate drivers for IGBTs contain protection circuits that detect and prevent improper operation of the power device.

Chapter 3
Gate Drivers

In an electronic system, a gate driver is connected between the microcontroller and the power device and amplifies the control signal to the voltage and currents levels required to control the switch. Thus, a gate driver communicates with the microcontroller's low-voltage domain, as well as the high-voltage region in which the switch operates. Therefore, another essential function of these circuits is the electrical separation of the two operating regions [3][5]-[8].

The basic structure of a gate driver is illustrated in Figure 3.1. The input block of the gate driver, or primary block, processes the control signal *IN* by means of a Trigger Schmitt circuit [9][10]. The secondary circuit, or output block, of the gate driver is referenced to the emitter terminal of the power switch. Within this block, the input signal is amplified to the level required for IGBT control [9][10]. The interface circuit provides electrical separation of the two voltage regions with which the gate driver communicates. This allows individual blocks to be referenced to a different potential compared to the global ground. The interface circuit also ensures the transfer of signals between the two component blocks [5][11][12].

Most of the current gate drivers available on the market also include a reverse communication path through which different states of the power device are transmitted [5]-[8]. The reverse communication path consists of a protection block integrated within the output circuit, which monitors the IGBT operating conditions. The protection blocks prevents the power device from operating outside SOA and generates an error signal when a faulty condition is detected. The interface circuit transfers the error signal to the primary block where it is processed within a control circuit and communicated to the microcontroller via the terminal *FLT*.

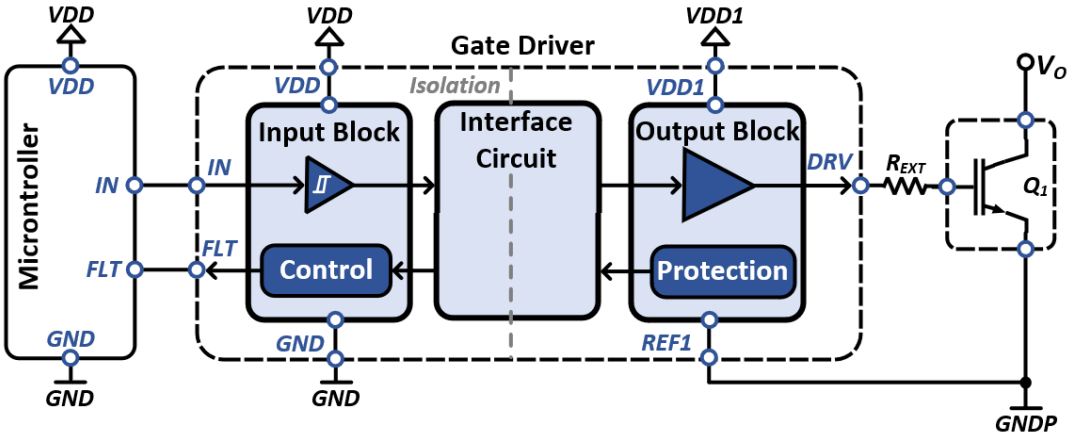


Figure 3.1 *Structure of a gate driver with protective block*

Chapter 4
Technique for Robust Data Communication

4.1 Block diagram of the proposed circuit

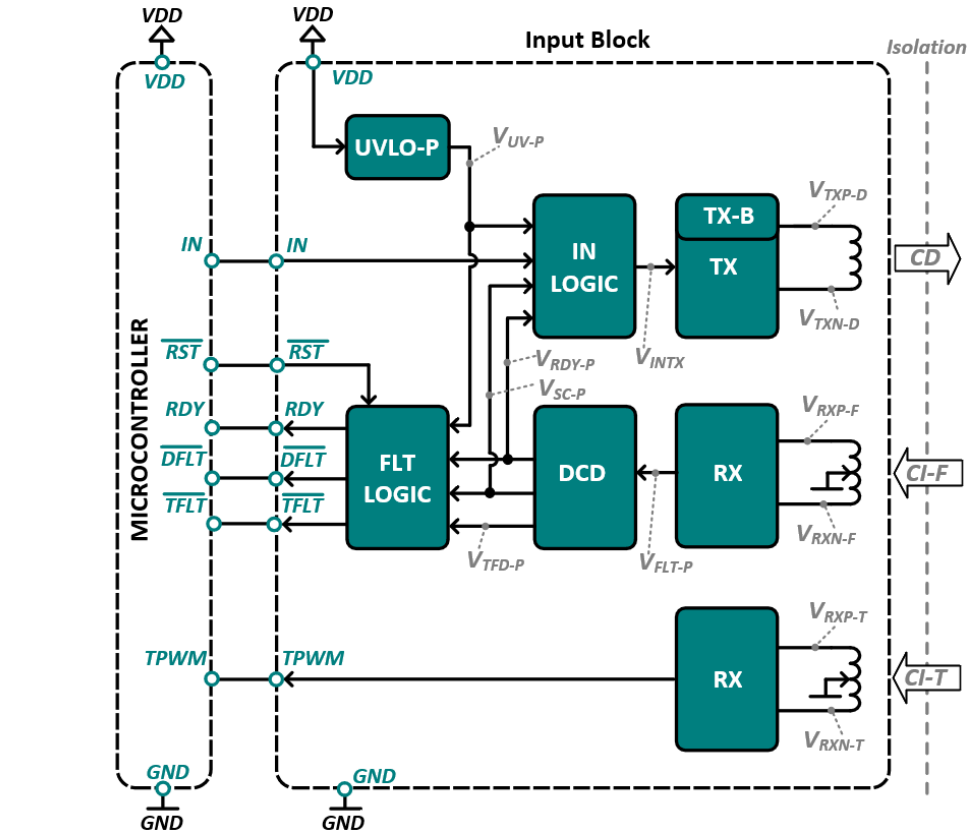
This chapter proposes a galvanically isolated gate driver for power devices, with robust data communication through the isolation barrier. The architecture of the circuit is presented in Figure 4.1, where the electrical separation of the internal blocks is ensured by means of three integrated transformers. The proposed gate driver includes three transmission paths consisting of the three transformers, together with a transmission circuit, TX, and a reception circuit, RX: a direct path (CD in Figure 4.1) which transfers the control signal from the microcontroller, and two reverse paths through which error signals are communicated (CI-F), respectively, the IGBT temperature (CI-T).

The output circuit is supplied by a positive voltage, *VDD1*, and a negative voltage, *VEE1*, both referenced to the *REF1* potential. The drive terminal, *DRV*, varies between these levels and three other pins, *DST*, *CL*, and *TS*, monitor the operating conditions of the IGBT.

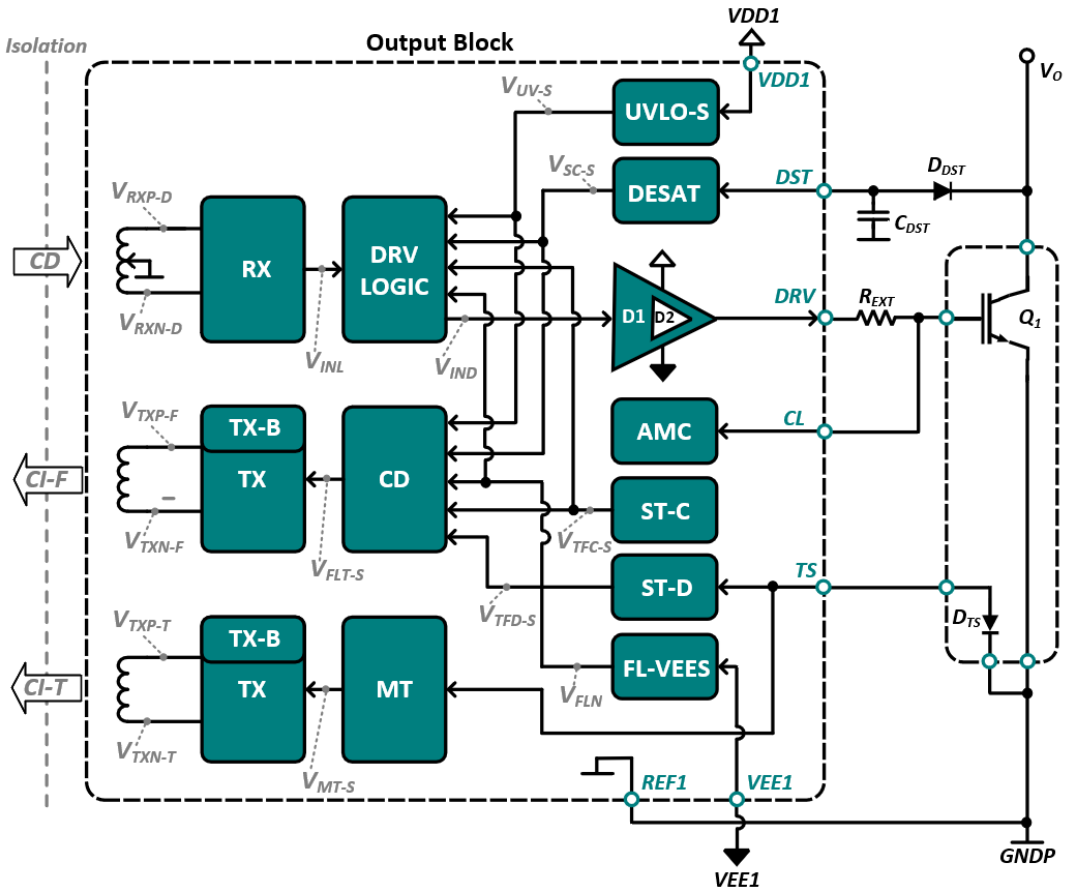
The input block contains, in addition to the power pin, *VDD*, and the control pin, *IN*, a terminal for resetting the entire circuit, $\overline{RST}$, and four reporting pins to the microcontroller. Three of these, *RDY*, $\overline{DFLT}$, and $\overline{TFLT}$, communicate error signals, while *TPWM* continuously reports the IGBT temperature.

The robust transmission of information is ensured primarily by implementing an extensive set of protection circuits for the IGBT and for the internal blocks. The IGBT is protected against over-current (DESAT), parasitic turn-on (AMC), and over-temperature (MT and ST-D). For the output block, over-temperature (ST-C), *VDD1* under-voltage lockout (UVLO-S), and *VEE1* terminal disconnection (FL-VEE) are monitored, while the input block is protected against *VDD* under-voltage lockout (UVLO-P). A series of logic circuits, DRV LOGIC, FLT LOGIC, and IN LOGIC, are configured to process the error signals.

The second stage in the development of the gate driver consists of optimizing the transmission paths in terms of area by encoding (CD) the error signals on the output block, and decoding them (DCD) within the input block. Thus, only one reverse transmission path is used (CI-F in Figure 4.1a. and Figure 4.1b) to communicate fault signals for the IGBT and for the output block. Additionally, the common-mode transient immunity is improved with the help of a proposed new architecture, implemented in the TX-B block.



a)



b)

Figure 4.1 *Internal blocks of the proposed gate driver a) primary b) secondary*

4.2 Implementation of protection circuits

4.2.1 Protection circuit for under-voltage lockout

The decrease of the positive supply voltage V_{VDD1} in the secondary block is detected through the architecture in Figure 4.2. A power switch operating with insufficient gate voltage leads to V_{CE} voltage increasing. This results in increased conduction losses [3][7]. V_{VDD1} cannot be monitored directly due to the high levels required. Therefore, the supply voltage is reduced by means of the resistive divider consisting of R_{SNS1} and R_{SNS2}. C_1 compares the divided supply voltage, V_{SNS}, against a reference voltage, V_{UVS-R}, dependent on the state of the comparator. As an additional protective measure against potential noise, the output signal of the comparator is passed through a noise filter (Figure 4.2).

The output signal of the gate driver, *DRV*, follows the *VDD1* variation until it drops below the $V_{UVLOS-OFF}$ threshold. Within the output block, the *UV-S* signal is first transmitted to the DRV LOGIC block where it resets a latch if V_{SNS} decreases below V_{UVS-R} for longer than t_F. As a result, V_{DRV} switches off using the low-impedance driver block, D1. Moreover, the information about *VDD1* under-voltage lockout is communicated to the input block via the CI-F path, and *RDY* is asserted low. The gate driver returns to normal operation when the supply voltage *VDD1* rises above the $V_{UVLOS-ON}$ threshold.

The gate drivers available on the market usually include a monitoring block for the supply voltage of the primary circuit, *VDD* [9][10]. This protection is necessary to ensure robust transmission of the control signal through the galvanic isolation barrier and correct communication of error signals to the microcontroller. *VDD* under-voltage lockout detection circuit from Figure 4.3 uses a comparator with internal hysteresis. In this case, the supply voltage ranges between 3.3 V and 5 V. When *VDD* decreases below the designed threshold, the gate driver's response is identical to the one described for *VDD1* under-voltage lockout condition.

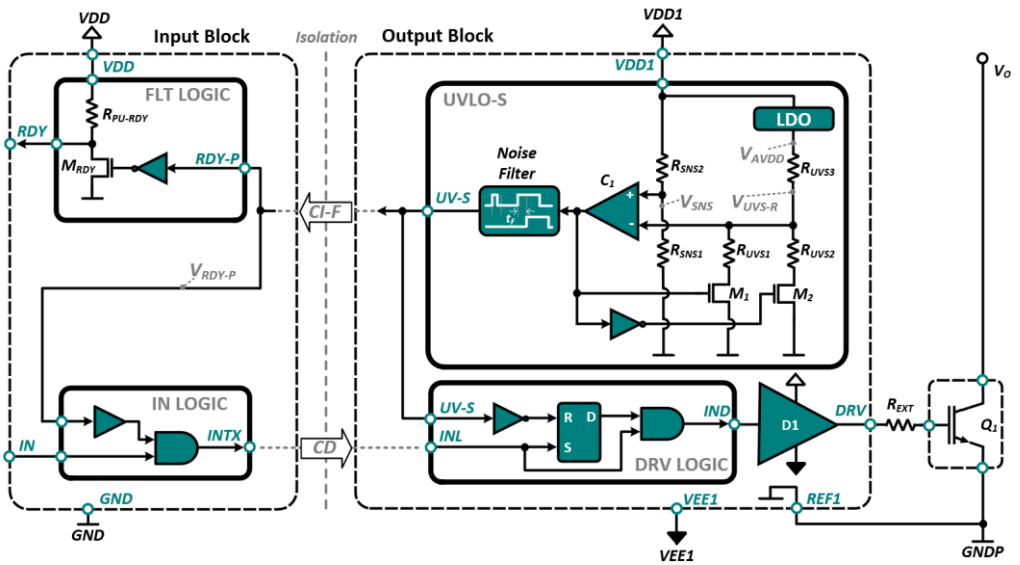


Figure 4.2 *VDD1 Under-Voltage Lockout Detection and Communication Circuit*

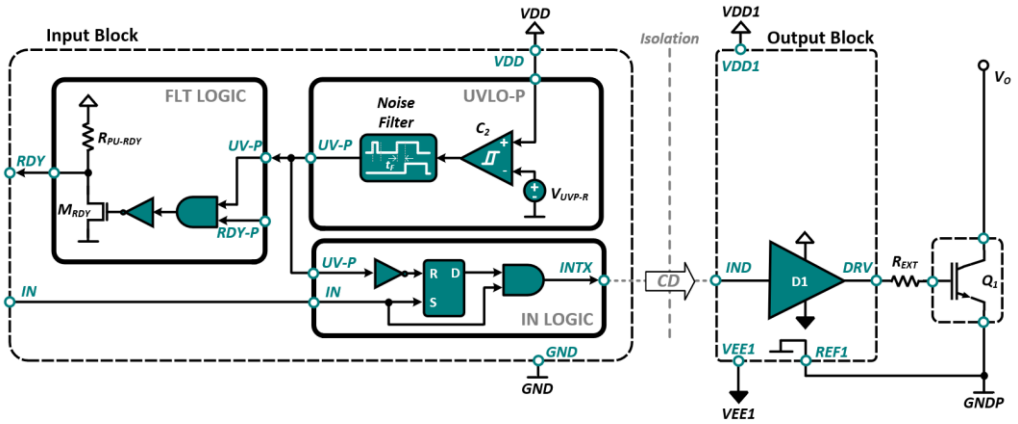


Figure 4.3 *VDD Under-Voltage Lockout Detection and Communication Circuit*

4.2.2 Protection circuit for IGBT over-current

An increase of the collector current, I_C, during constant gate-emitter voltage causes the voltage V_{CE} to increase. Thus, the IGBT exits the saturation region and operates in the active region. As a result, the IGBT over-current condition is also known as power device desaturation. An IGBT can operate under these conditions without being thermally destructed for a short interval, between 6 μs and 10 μs [3][13].

The IGBT over-current protection circuit is presented in Figure 4.4 and is based on monitoring the voltage drop across the power device [3][5][6]. Switch M_{IDST} is added to disable the current source I_{DST} when the control signal *IN* is not active. In addition, the V_{DST} voltage is reduced through the resistive divider consisting of R_{DST1} and R_{DST2}. This is necessary to protect the input of the comparator *C3* from the high values that may appear. Voltage drop monitoring on the IGBT starts when D_{DST} is forward biased:

$$V_{DST} = V_F + V_{CE,SAT} \tag{4.1}$$

During a short-circuit condition, the V_O voltage increases significantly and leads to D_{DST} being reverse biased, I_{DST} charges the external capacitor C_{DST}, and C_3 output switches high [3] after $t_{DST,}$ a delay necessary for V_{DST-D} to reach V_{SC}:

$$t_{DST} = \frac{C_{DST}}{I_{DST}} \left(\frac{R_{DST1} + R_{DST2}}{R_{DST1}} V_{SC} - V_F - V_{CE,SAT}\right) \tag{4.2}$$

After C_3 switches high, a timer (Figure 4.4) is enabled to activate *SC-S* for a fixed time interval called "communication time". During this time interval, the DRV LOGIC block switches off the power device. The IGBT is turned off through a high impedance path, D2 in Figure 4.4, that minimizes the V_{CE} overshoot. The over-current error signal is also transmitted to the primary block during the communication interval via the CI-F path, and pin $\overline{DFLT}$ is forced low. A latch within the FLT LOGIC blocks is set and the $\overline{DFLT}$ pin remains 0 until a rising edge is sent on $\overline{RST}$. In addition, the IGBT is turned on only after a rising edge is recorded on V_{INL}.

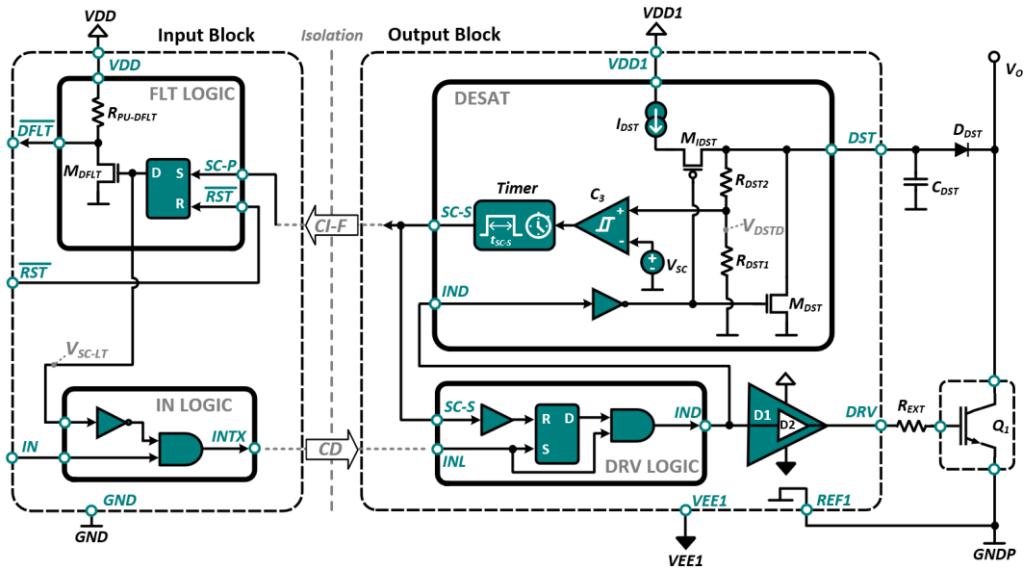


Figure 4.4 *IGBT Over-current detection and communication circuit*

4.2.3 Protection circuit for IGBT parasitic turn-on

Such a circuit is shown in Figure 4.5 and it is also referenced in the literature as *Active Miller Clamp* – AMC. The gate voltage of the power device is monitored via pin *CL*. An input adapter, IAU in Figure 4.5, limits the V_{CL} voltage to 5 V in reference to *VEE1*, in order to protect the internal devices [14]. Comparator C_4 switches high when the IGBT is turned off and V_{DRV} drops below the $V_{CL\text{-}THR}$ threshold. When these conditions are met, the output signal of C_4 is recorded in a latch circuit which activates the M_{CL} switch. M_{CL} provides a low-impedance discharge path for the I_{CG} current injected by the Miller capacitance, C_{CG}, during V_{CE} variation .

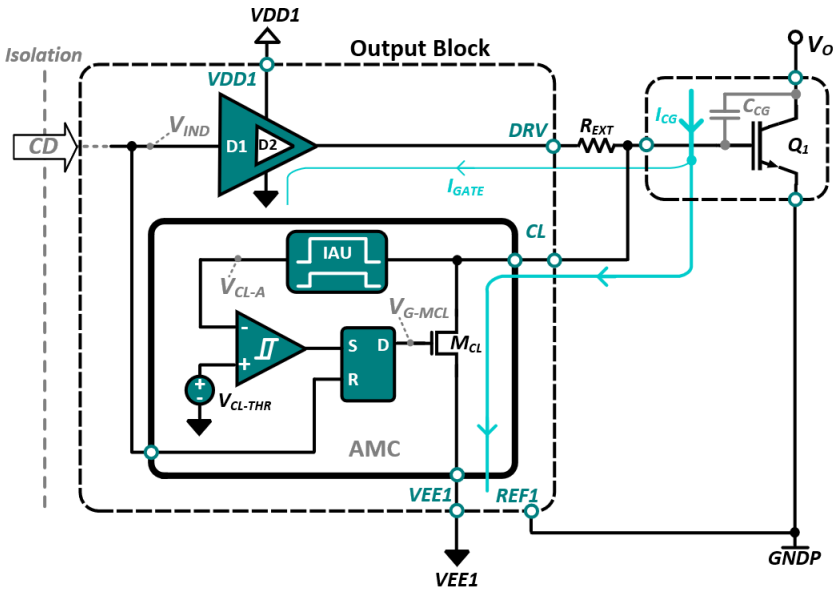


Figure 4.5 *Circuit for protection against IGBT parasitic turn-on*

4.2.4 Protection circuit for *VEE1* terminal floating

A new protection function is proposed within this work [15]. Figure 4.6 features a circuit that monitors the negative supply voltage. The proposed architecture follows the V_{VEE1} voltage and transmits an error signal to the microcontroller if the *VEE1* pin is floating. The novelty of this protection function lies in the possibility of connecting the *VEE1* pin to a negative supply source, or to the reference potential of the secondary block, V_{REF1}. In these conditions, $I_{B\text{-}F2}$ biases diode D_{F2} which provides the reference voltage of the comparator, $V_{F\text{-}INP}$:

$$V_{F-INP} = V_{DF2} \tag{4.3}$$

The negative input of the comparator, $V_{F\text{-}INN}$, monitors the *VEE1* terminal through the voltage drop on the R_{F1} resistor. $V_{F\text{-}INN}$ is pulled below the V_{REF1} reference level when the gate driver is supplied with a negative voltage. Thus, the D_{F1} diode is forward biased and limits $V_{F\text{-}INN}$ voltage to aproximately -0.7 V. At the same time, D_{F1} injects a current, I_{DF1}, through the R_{F1} resistor to set the operating point. The value of the $V_{F\text{-}INN}$ voltage is obtained as follows:

$$V_{F-INN} = V_{RN} = (I_{DF1} + I_{B-F1})R_{F1} + V_{VEE1} \tag{4.4}$$

Under these conditions, *FLN* is active to signal the proper connection of the *VEE1* terminal, and *RDY* is activated.

If the *VEE1* pin is not connected properly (board fault, circuit fault, broken connection wire, etc.), the negative supply voltage increases and is limited by D_{ESD}, at $V_{F\text{-}DESD}$ above the reference level. $V_{F\text{-}INP}$ is given by the voltage drop on the D_{F2} diode to compensate for the temperature variation of the V_{VEE1} voltage when the pin is floating. At the same time, the negative input of the comparator follows the V_{VEE1} voltage. Under these conditions, the output signal of the comparator switches low. As a consequence, the control signal is no longer transmitted to *DRV* and the *RDY* signal is pulled low to communicate the condition externally. The circuit returns from this condition when the *VEE1* terminal is connected to the *REF1* reference level or to a negative voltage source.

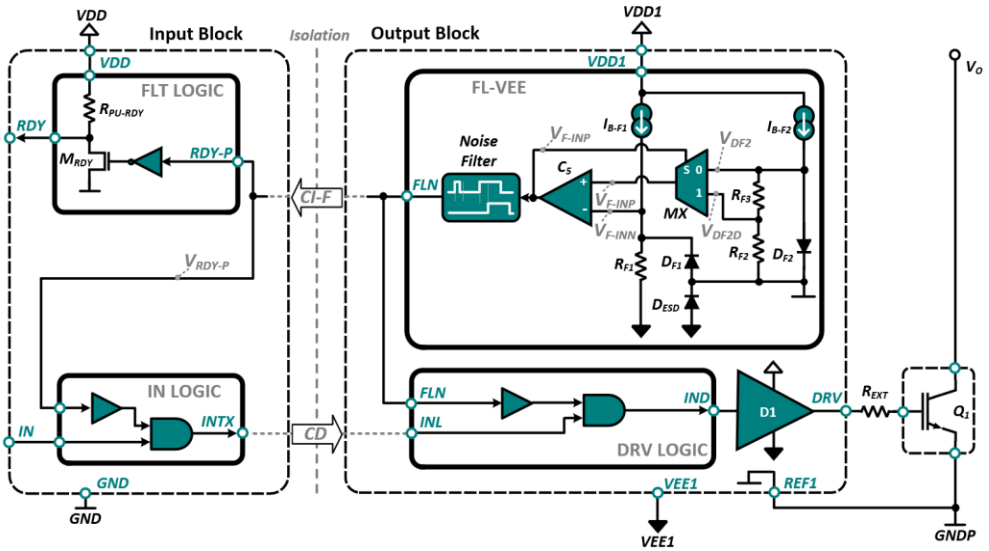


Figure 4.6 *Circuit for protection against VEE1 terminal floating*

4.2.5 Over-temperature protection circuit

The detection circuit for the over-temperature condition of the output block is shown in Figure 4.7. A comparator with internal hysteresis, C_6, monitors an internal voltage, $V_{F\text{-}DCTS}$, and changes its state when the voltage drops below a predetermined threshold, $V_{C\text{-}TSR}$. The architecture in Figure 4.7 includes a temperature sensor [16] implemented with diode $D_{C\text{-}TS}$. The over-temperature condition of the output block is reported on *RDY*, and the control signal *DRV* is disabled.

The proposed gate driver includes the architecture from Figure 4.8 to measure the temperature of the power switch [17]. The configuration is compatible with smart power devices that integrate a temperature sensor into their capsule. The structure is represented in Figure 4.8 with the help of diode D_{TS}. Current source I_{TS} biases the external sensor connected to the pin *TS*, and the voltage drop on D_{TS} is monitored by two comparators. C_7 compares V_{TS} with a periodic sawtooth signal, V_{OSC}, to generate $V_{MT\text{-}S}$. As the temperature of the power device increases, the voltage drop on D_{TS}, $V_{D\text{-}TS}$, decreases, and the duty cycle of *MT-S* increases. *MT-S* is transmitted on a dedicated reverse path, CI-T in Figure 4.8, to the primary block to continuously communicate the temperature of the power device.

The IGBT over-temperature condition is also detected by the C_8 comparator from Figure 4.8. Its output is asserted high when V_{TS} drops below the reference threshold $V_{D\text{-}TSR}$, corresponding to a specific temperature. Thus, the signal $V_{ST\text{-}D}$ is encoded and transferred over the CI-D path to the primary block to communicate the error via the $\overline{TFLT}$ pin. This redundancy of the IGBT temperature information increases the safety of the system and ensures that the faulty condition is communicated, even if one of the transfer paths is damaged [17].

The proposed gate driver includes a new architecture that disables the IGBT's over-temperature detection function when terminal *TS* is floating [17]. When pin *TS* is connected to an external temperature sensor, $M_{TS\text{-}F}$ is in linear region. The current through the branch is compared against a constant current, $I_{R\text{-}TS}$. If *TS* pin is floating, V_{TS} is pulled to V_{AVDD} through resistance $R_{PU\text{-}TS}$. Thus, the source-gate voltage of the transistor $M_{TS\text{-}F}$ decreases, and $I_{F\text{-}TS}$ becomes null. As a consequence, $V_{TS\text{-}EN}$ switches high and disables the current source I_{TS}.

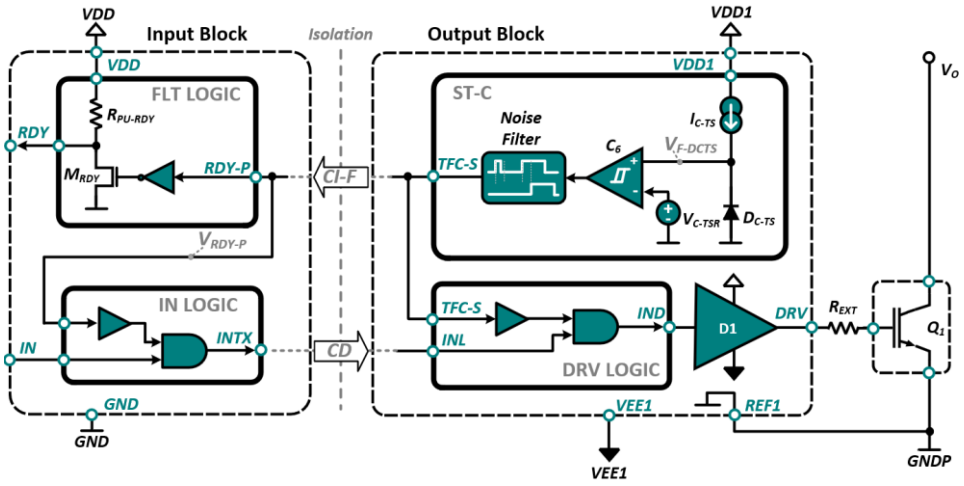


Figure 4.7 *Circuit for protection against secondary block over-temperature*

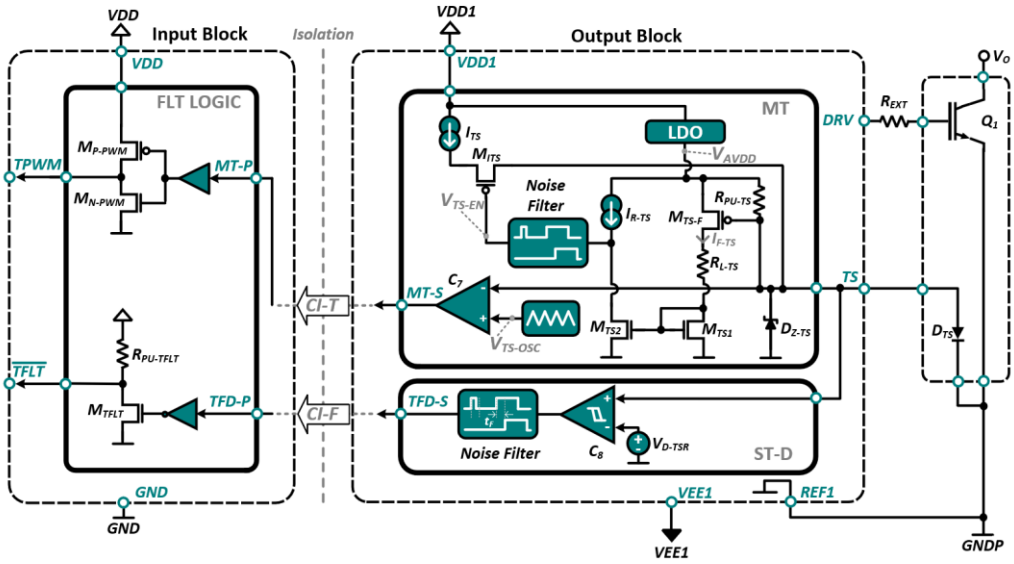


Figure 4.8 *Circuit for protection against IGBT over-temperature*

4.3 Transmission Paths

4.3.1 Encoding and decoding error signals

In order to optimize the circuit area, the error signals detected on the secondary block are transmitted to the primary circuit using a single reverse communication path, CI-F. In order to differentiate the error signals, they are first encoded using a proposed new block, CD from Figure 4.9, and then communicated through the galvanic isolation barrier. Within the primary block, a decoding process takes place by means of the DCD circuit from Figure 4.9 [17].

The coding block combines the error signals of the output block. Thus, the *UV-S* signal is processed together with *FLN* and *TFC-S*. The CD-R block generates a periodic signal, characterized by period t_{PR} and width t_{PWR}, when the output block is operating optimally. This signal is transmitted through the isolation barrier to the primary circuit. When decoding the periodic signal, the DCD-R block activates *RDY-P*. A faulty operating condition of the output block interrupts the generation of the periodic signal. In the absence of three consecutive pulses, the DCD-R block sets *RDY-P* to 0.

The IGBT over-temperature condition is signaled by *TFD-S* switching low. As a result, CD-T generates a periodic signal with a frequency 10 times higher compared to the frequency of the pulses transmitted during normal operation. The two periodic signals are superimposed and transmitted through the CI-F isolation path. In the input block, the DCD-T circuit detects the high-frequency signal and sets *TFD-P* to 0.

The detection of the IGBT over-current condition results in the generation of a single pulse at the output of the CD-D block. The width of this pulse is 7 times larger than t_{PWR}. The transmission of the over-current pulse is prioritized through the isolation pathway. The DCD-D decoding circuit measures the width of the transmitted signal and forces *SC-P* to 0 to signal the encountered error.

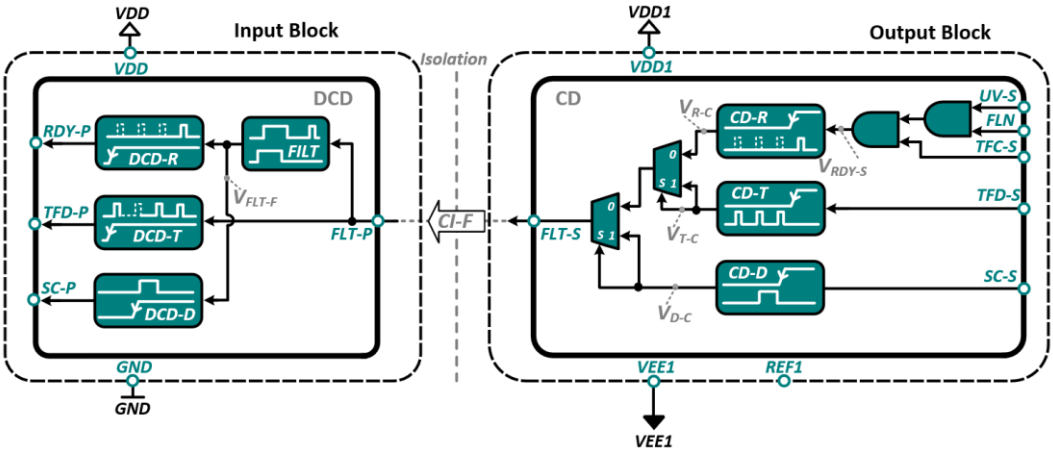


Figure 4.9 *Circuits for coding and decoding error signals*

4.3.2 Signal transmission

The proposed gate driver uses an oscillator which employs the On-Off Keying transmission technique to transfer signals through the galvanic isolation barrier. The transmission circuit is shown in Figure 4.10 and consists of a negative-g_m LC oscillator [18]. The signal from the oscillator's input is modulated in amplitude, and its spectrum is translated to a higher frequency. The configuration uses the primary winding, L_P, of the integrated transformer to create an LC oscillator together with capacitor C_{TX}. When the control signal activates, switch M_{N3} is activated and enables the I_{TX} current source. Thus, nodes V_{TXP-D} and V_{TXP-N} start oscillating. An imbalance is created between the two branches, which is necessary to maintain the oscillations.

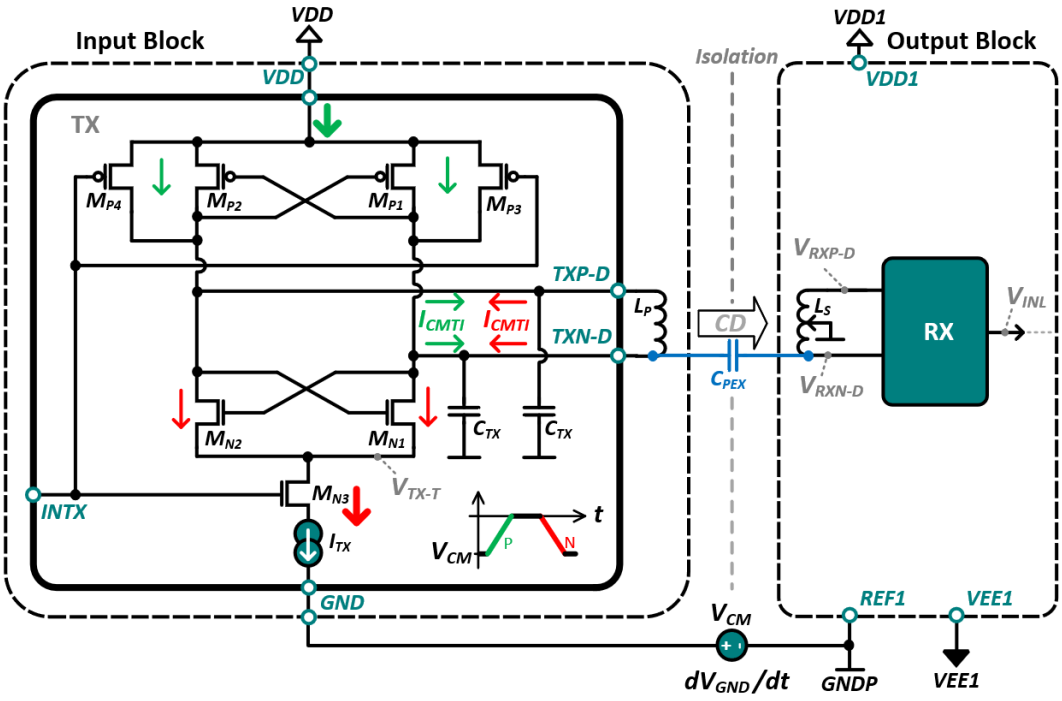


Figure 4.10 *Architecture of the transmission circuit*

4.3.3 Common-Mode Transient Immunity Improvement

A critical feature of galvanically isolated gate drivers is the Common Mode Transient Immunity, or the noise immunity. This defines the maximum dV_{REFx}/dt slope up to which the output signal *DRV* is not affected [19][20]. The test method described in the literature involves varying *GND* between *GNDP* and -*VCC*, which has a similar effect to fluctuating V_{REFx} from *GNDP* to *VCC* [20]. In this case, *VCC* represents the amplitude of the common-mode signal [21].

Figure 4.10 presents the CMTI testing method and details the effect of *GND* variation on the proposed transmission circuit. Two types of CMT events are defined: a positive event (green slope in Figure 4.10) where *GND* increases from $-V_{VCC}$ to the *REF1* potential, with a certain dV_{GND}/dt slope. Similarly, a negative CMT condition (red slope in Figure 4.10) is characterized by *GND* decreasing relative to *REF1* to $-V_{VCC}$. A current, I_{CMTI}, occurs at the output nodes of the oscillator during these events:

$$I_{CMTI} = C_{PEX} \frac{dV_{GND}}{dt} \tag{4.5}$$

where C_{PEX} represents the parasitic capacitance between the transformer windings.

When the oscillator input is active and a negative CMT event is applied, $V_{TXP\text{-}D}$ and $V_{TXP\text{-}N}$ increase based on the value of the injected current. For high I_{CMTI} values, the output nodes of the oscillator increase to the point where oscillations disappear. As a result, V_{INL} switches low and the control signal *DRV* registers a false turn-off for the duration of the CMT negative condition.

The CMTI performances of the proposed gate driver are improved with the help of the new configuration in Figure 4.11 [22][23]. This circuit contains three internal blocks. CMT-MON monitors the output signals of the oscillator, $V_{TXP\text{-}D}$ and $V_{TXP\text{-}N}$, and activates M_{N6} when they exceed the level of the supply voltage, V_{VDD}. The CMT-DL block memorizes the active state for a fixed interval, and CMT-CD enables an additional current path, $I_{TX\text{-}B}$, to discharge I_{CMTI} during a negative CMT condition and *IN* active. Thus, *TXP-D* and *TXP-N* continue to oscillate, and the control signal V_{INL} no longer registers a false turn-off. Additionally, the FP block at RX output filters out any glitches shorter than $t_{IN\text{-}F}$.

Figure 4.12 shows a Shmoo diagram that highlights the noise immunity of the proposed circuit as a function of common-mode signal amplitude, V_{CM}, and slope dV_{GND}/dt. Values for the FP filtering time and the additional current $I_{TX\text{-}B}$ were chosen to minimize their impact on propagation delay time and total current consumption. For zone A, the transmission block is capable of discharging an additional current of 5 mA without stopping the oscillations. In zone B of Figure 4.12, FP filters out any false deactivation of *DRV* for CMT negative events with a duration shorter than 20 ns.

The circuit proposed in Figure 4.11 prevents false turn-off for dV_{GND}/dt slopes in area C. $I_{TX\text{-}B}$ is set to 18 mA (corresponding to dV_{GND}/dt = 70 kV/μs) to cover all dV_{GND}/dt included in zone C. Additionally, $C_{TX\text{-}B}$ and $R_{TX\text{-}B}$ are sized so that $I_{TX\text{-}B}$ is activated for 200 ns. This interval ensures that the oscillations at the output of the transmission circuit are maintained for all dV_{GND}/dt slopes, while also taking into account the temperature and process variations.

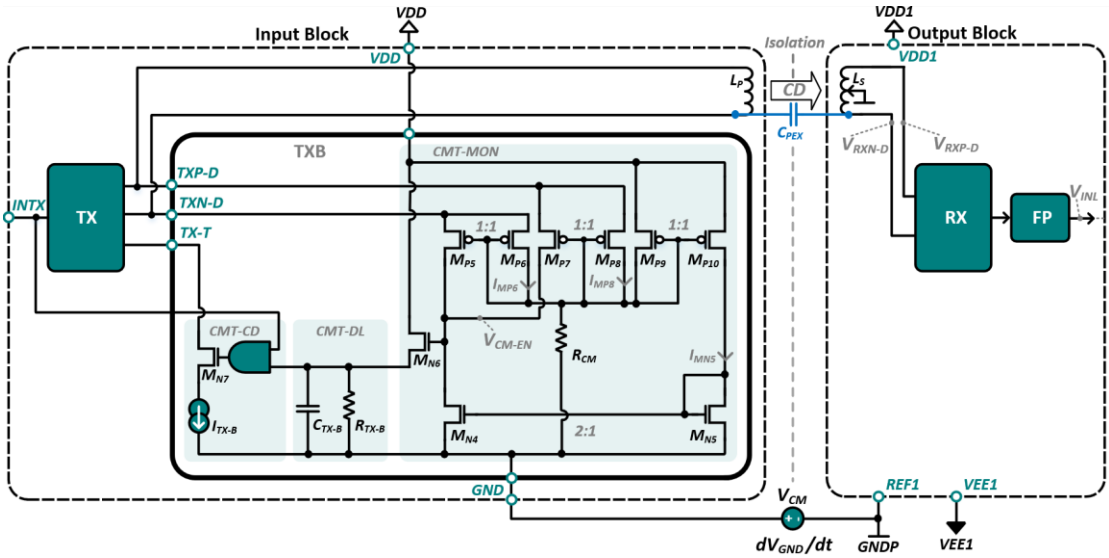


Figure 4.11 *Proposed circuit to improve CMTI performances*

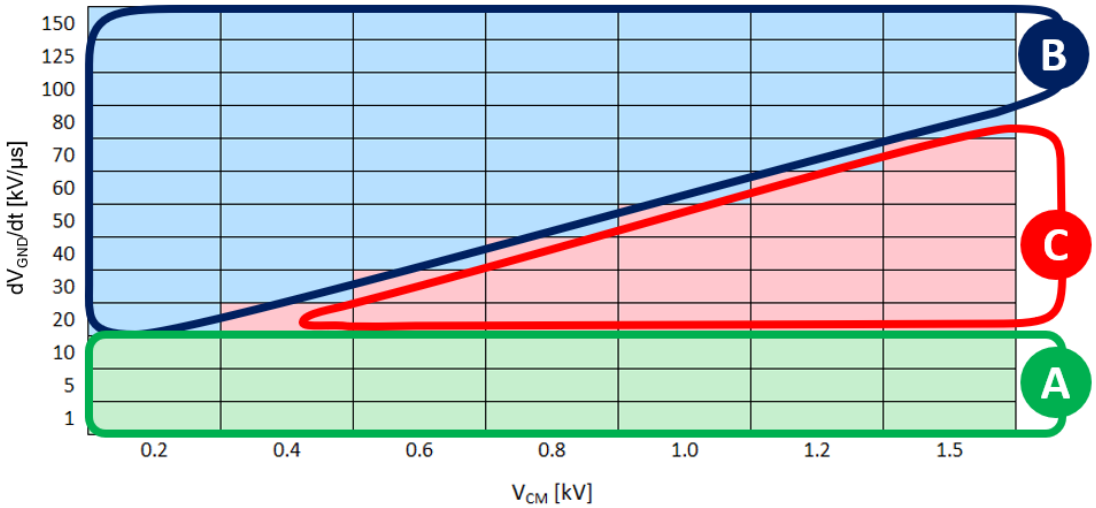


Figure 4.12 *Shmoo diagram highlighting the improved CMTI performances of the proposed gate driver*

Chapter 5
Experimental Results

5.1 Verification Environment

The gate driver in Figure 4.1 was implemented and simulated in the Cadence Virtuoso environment, using BSIM3v3 models for transistors belonging to a 0.25 μm and 5 V technology. Figure 5.1 shows a screenshot from the Cadence Virtuoso environment. Each terminal in Figure 5.1 is internally connected to the corresponding block by means of two resistors and an inductance. They are used to model parasitic elements of the package. Thus, the two resistors have a combined value of 67.2 mΩ, and the parasitic inductance is 2 nH.

Once the proper operation of the gate driver is confirmed through simulations, the development is continued with silicon implementation and experimental results. In this scope, the circuits were packaged in SOIC16 plastic capsules.

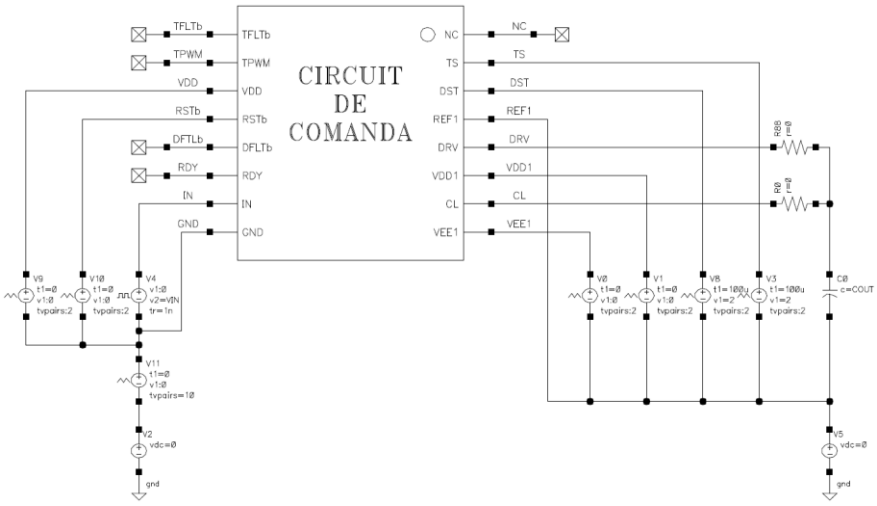


Figure 5.1 *Simulation testbench of the proposed gate driver*

5.2 Verification of Protection Circuits

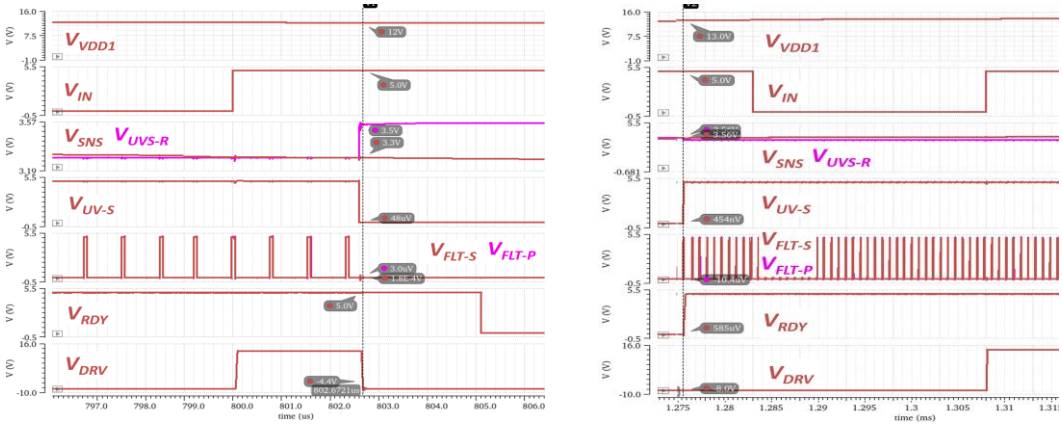
5.2.1 Supply under-voltage lockout

For this verification, the following conditions were used: $V_{VDD} = V_{\overline{RST}}$ = 5 V, V_{DST} = 0 V, V_{VEE1} = -8 V, while the *TS* pin is floating and *DRV* terminal is connected to a capacitive load of 100 nF. A rectangular signal with a frequency of 20 kHz and a 50% duty cycle is applied to the input, and *VDD1* is varied between 15 V and 10 V.

Figure 5.2 presents the simulation results when *VDD1* falls below the set threshold of 12 V. As long as the $V_{VDD1} > V_{UVLOS\text{-}OFF}$ condition applies, *UV-S* is asserted high. As a result, a periodic signal is transmitted to the primary block to communicate the normal operation of the gate driver and set *RDY* to 1.

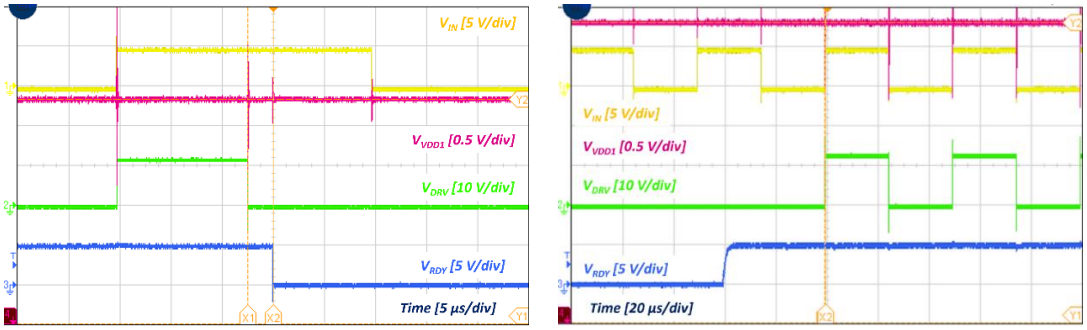
For V_{VDD1} < 12 V, signal *UV-S* switches low, while V_{DRV} is pulled low and does not follow the input signal. Additionally, the generation of the periodic signal is stopped and *RDY* is set to 0 in the absence of three consecutive pulses. In Figure 5.2b, a reverse sequence checks the behavior of the gate driver when the V_{VDD1} voltage increases above 13 V. The results of the simulations are also validated through experimental results after silicon implementation. Oscilloscope captures in Figure 5.3a and Figure 5.3b confirm the simulated behavior for both decreasing, and increasing, the supply voltage V_{VDD1}. The sillicon validation is completed with statistical data on the parameters of interest, resulted from testing 70 circuits at three different temperatures. The values are included in Table 5.1 and confirm that the thresholds and hysteresis are within the design limits.

The response of the gate driver to the variation of the supply voltage of the primary block, V_{VDD}, is validated experimentally, and the oscilloscope capture is presented in Figure 5.4. The circuit is in normal operation when *VDD* exceeds the threshold of 2.8 V. V_{RDY} follows the V_{VDD} variation down to the 2.65 V threshold. Below this value, the control signal is no longer transmitted to the output, while *RDY* is set to 0. Statistical data for the parameters were obtained using the conditions described above to test 70 circuits, and the values are within specifications, as shown by Table 5.1.



a) b)

Figure 5.2 *Simulation results for a) decreasing b) increasing* V_{VDD1}



a) b)

Figure 5.3 *Oscilloscope capture with the response of the gate driver to a) decreasing b) increasing* V_{VDD1}

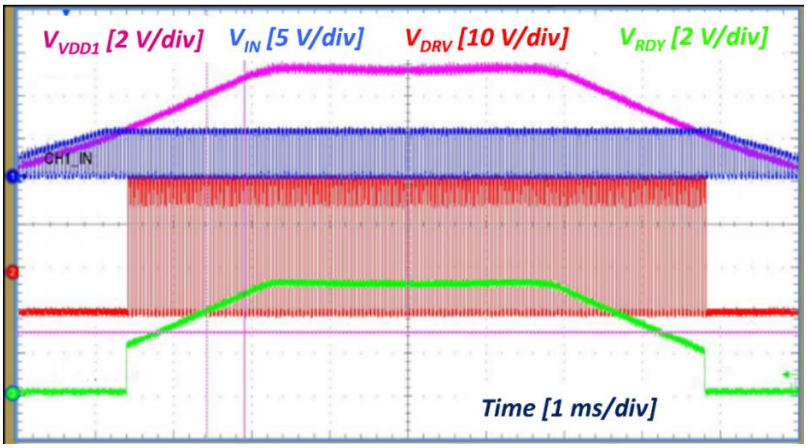


Figure 5.4 *Oscilloscope capture – gate driver behavior for V_{VDD} variation*

5.2.2 IGBT Over-current

The verification of the proposed gate driver continues with the simulation of the IGBT over-current protection function. In Figure 5.5, V_{DST} ranges from 0 V to 10 V when *DRV* is 1. For V_{DST} = 9 V, $V_{DST\text{-}D}$ reaches the reference value V_{SC} = 3 V. Thus, *SC-S* is activated for a duration of 5 µs. As a result, the output voltage V_{DRV} switches low via the D2 driver, which is evidenced by the slow switching slope. At the same time, a wide pulse is generated and transmitted on the reverse path CI-F. Once this pulse is detected, $\overline{DFLT}$ is asserted low to signal the condition encountered. The experimental results from Figure 5.6 show an identical behavior.

Figure 5.6 also pictures resuming the normal operation after the detection of an IGBT over-current condition. For this, a negative pulse must be transmitted on the $\overline{RST}$ pin. The $\overline{DFLT}$ pin is activated once a positive edge is detected on the $\overline{RST}$ signal, while the output signal starts following the input after a positive edge is transmitted on IN. The experimental results from Table 5.1 include the process and temperature variation for V_{DST} and I_{DST} after testing 70 circuits at 3 different temperatures. Thus, the values obtained are within the design limits.

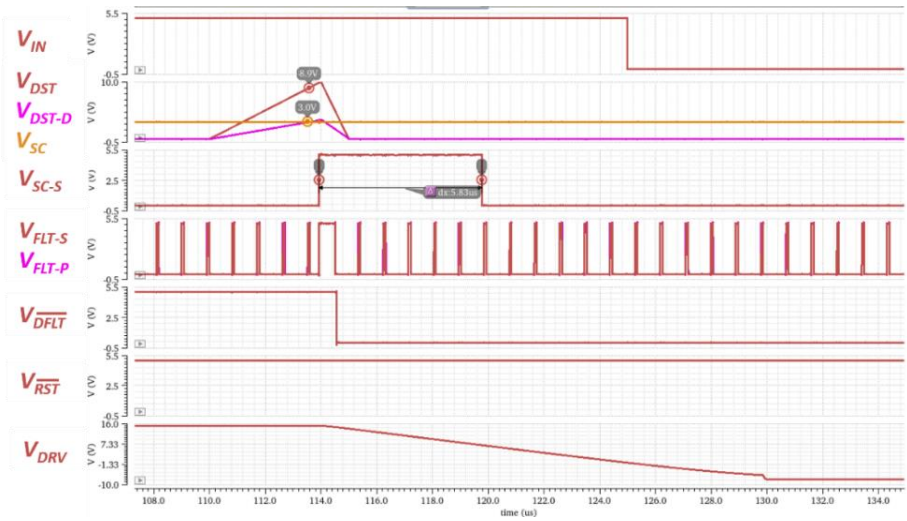


Figure 5.5 *Simulation results for IGBT over-current fault transmission*

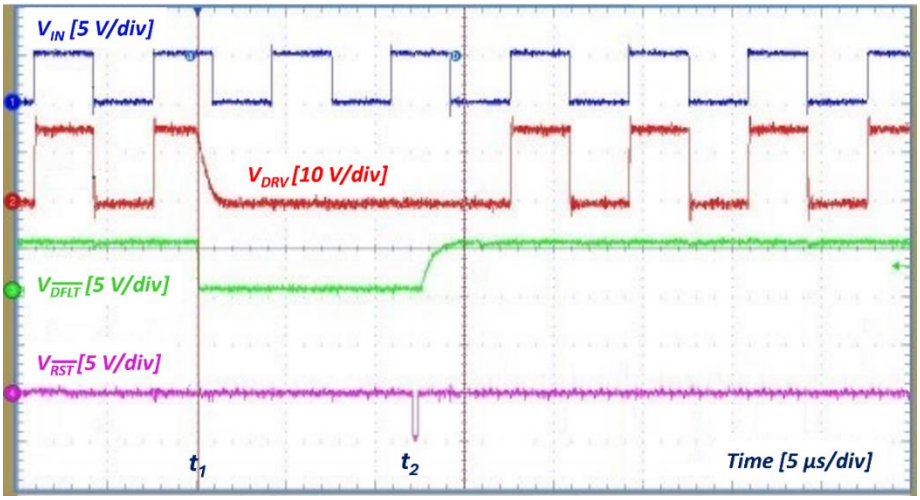
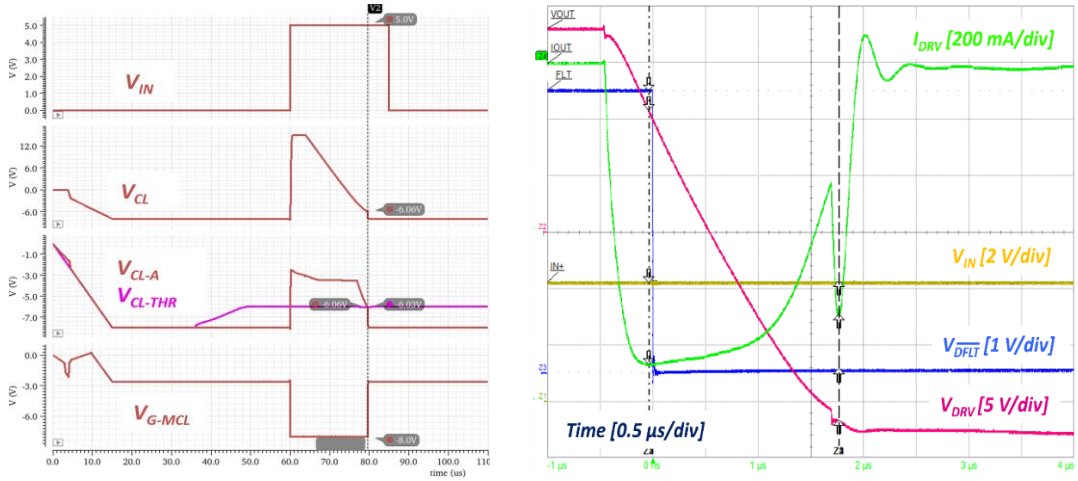


Figure 5.6 *Gate driver response to IGBT over-current condition*

5.2.3 IGBT Parasitic Turn-on

The protection circuit against IGBT parasitic turn-on is simulated by connecting terminals *CL* and *DRV* to a capacitive load of 1 µF. The waveforms resulting from the simulations are shown in Figure 5.7a, and the experimental results are included in Figure 5.7b. V_{VEE1} is -8 V, while V_{VDD1} is 15 V, and the primary block is supplied to V_{VDD} = 5 V. At the same time, $V_{\overline{RST}}$ = 5 V and *TS* terminal is floating.

Under these conditions, the NMOS transistor in the AMC circuit is activated and its gate-source voltage, $V_{G\text{-}MCL}$ in Figure 5.7, has a value of 5 V relative to the negative supply voltage, V_{VEE1}. When V_{DST} increases above the threshold value, V_{CL} switches low slowly, and $V_{CL\text{-}A}$ follows its variation once V_{CL} drops below 4.6 V relative to V_{VEE1}. When the $V_{CL} - V_{VEE1} < V_{CL\text{-}THR}$ condition is met, transistor M_{CL} is activated and discharges the remaining charge. Statistical data from Table 5.1 obtained by measuring 70 circuits at 3 temperatures shows the $V_{CL\text{-}THR}$ threshold is within specifications.



a) b)

Figure 5.7 *a) Simulation b) experimental results for IGBT parasitic turn-on protection circuit*

5.2.4 VEE1 Terminal Floating

The protection circuit for *VEE1* terminal disconnection was simulated using the following conditions: $V_{VDD} = V_{\overline{RST}} = 5$ V, $V_{VDD1} = 15$ V, $V_{DST} = 0$ V, pin *TS* floating, and V_{IN} is a rectangular signal with frequency 20 kHz, amplitude 5 V and duty cycle 50%. The waveforms obtained are included in Figure 5.8. At 210 µs, pin *VEE1* is left floating. V_{VEE1} begins to increase and it is limited by diode D_{ESD} to 575 mV. In these conditions, $V_{F\text{-}INN}$ increases above the reference voltage, $V_{F\text{-}INP}$. Consequently, signal *FLN* switches low, *RDY* is set to 0 and the control signal is no longer transmitted to V_{DRV}. The faulty condition reporting is also validated experimentally in Figure 5.9a, where V_{VEE1} is slowly varied between -1.5 V and 1 V.

In Figure 5.8, when terminal *VEE1* is reconnected to the -8 V voltage source, $V_{F\text{-}INN}$ immediately drops to -713 mV. As a result, *FLN* switches high to allow the communication of periodic pulses to the input block, and *RDY* is set to 1. The response of the gate driver is validated experimentally in Figure 5.9b.

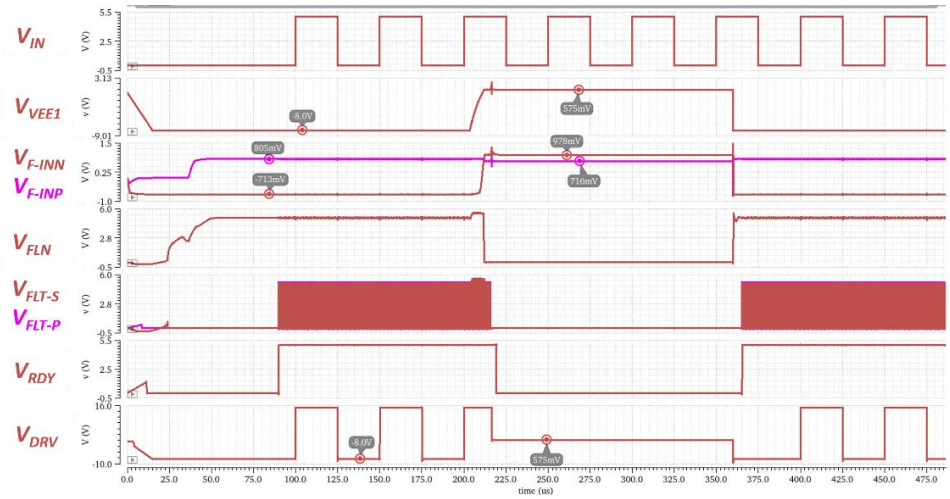
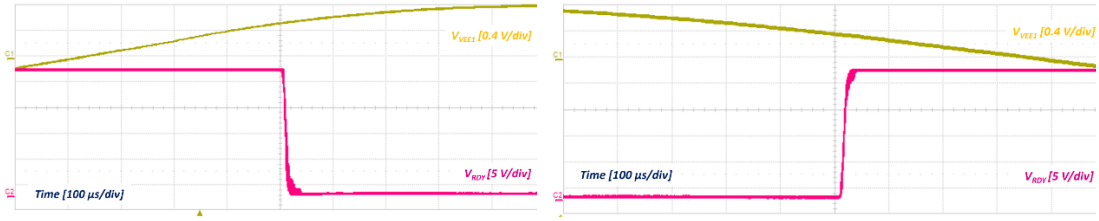


Figure 5.8 *Simulation results for VEE1 pin floating*



a) b)

Figure 5.9 *Oscilloscope capture with the response of the gate driver to a) increasing b) decreasing V_{VEE1}*

5.2.5 Over-temperature

The circuit in Figure 4.7 for detecting the output block over-temperature was validated through experimental results on 5 units using a Temptronic ATS-545 temperature source. The gate driver reports an error via the *RDY* pin when the mean temperature exceeds 181 °C. In reverse variation, the gate driver resumes normal operation at 155 °C.

The IGBT over-temperature protection circuit was validated through simulations and measurements. The conditions used are: V_{VEE1} = -8 V, V_{VDD1} = 15 V, V_{VDD} = $V_{\overline{RST}}$ = 5 V and V_{DST} = 0 V. V_{IN} connects to a function generator providing a rectangular periodic signal, with frequency 20 kHz, amplitude 5 V and duty cycle 50%. In Figure 5.10 and Figure 5.11, when V_{TS} drops below 1.68V, the secondary block transmits a narrow periodic high-frequency signal to the input circuit to report the IGBT over-temperature condition. These narrow pulses are superimposed over the wider pulses associated with normal operation of the output block. Once the high-frequency pulses are detected, $\overline{TFLT}$ switches low to report the error externally, without affecting the transmission of the control signal to the output.

The experimental results from Figure 5.11 show *TPWM* behavior when V_{TS} decreases. The duty cycle increases as the voltage decreases, equivalent to IGBT temperature increasing. In addition, the duty cycle value is validated in Figure 5.12 where DC_{TPWM} is 50% for V_{TS} = 2.875 V. Statistical data from Table 5.1 obtained by testing 70 circuits at 25° C show the values are within specifications.

The new architecture that disables the IGBT over-temperature detection when *TS* pin is floating, was verified through experimental results in Figure 5.13. In these circumstances, V_{TS} is limited to 5 V and *TPWM* is set to 0. In addition, the $\overline{TFLT}$ state is not affected, and the output signal follows the signal applied to the input.

Figure 5.10 *Simulation results for $\overline{TFLT}$ error signal transmission*

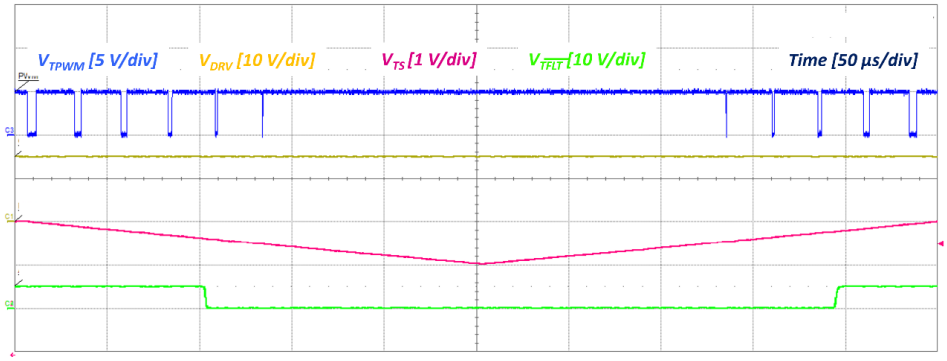


Figure 5.11 *Oscilloscope Capture for V_{TS} variation*

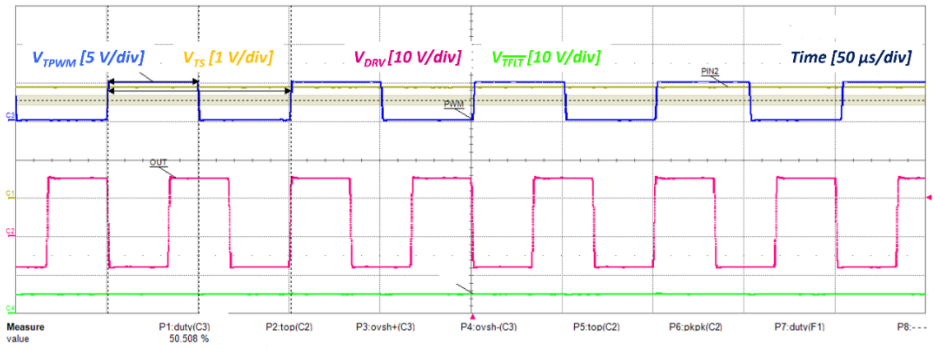


Figure 5.12 *Oscilloscope capture for V_{TS} = 2.875 V*

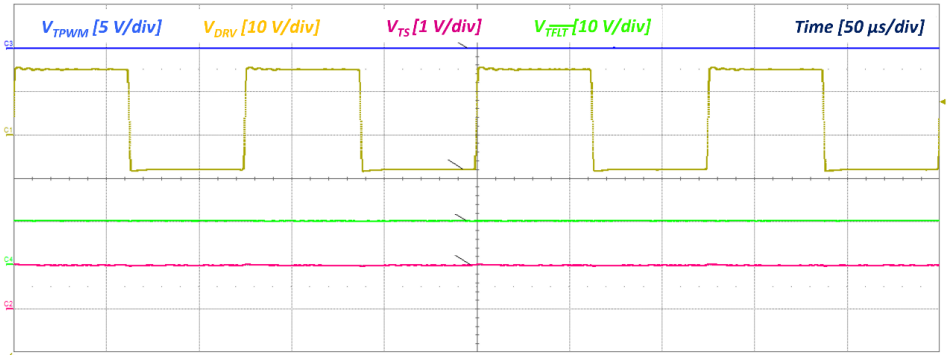


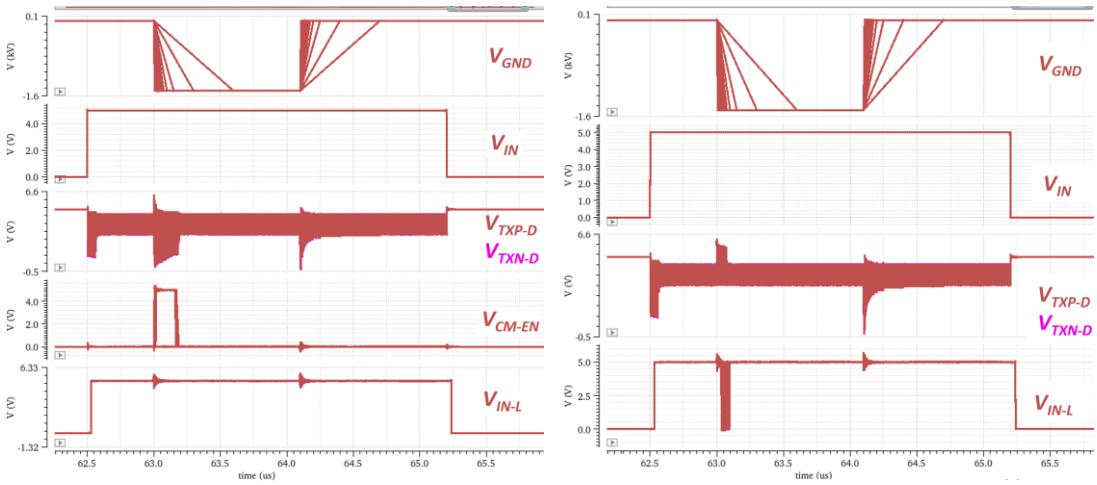
Figure 5.13 *Oscilloscope Capture for TS pin floating*

5.3 Common-Mode Transient Immunity

Figure 5.14a shows the response of the gate driver to *GND* variation when the CMTI enhancements circuits, TX-B and FP, are enabled. In this scope, *GND* voltage fluctuates from 0 V to –1500 V relative to *REF1* when V_{IN} is activated. dV_{GND}/dt slopes range from 1 kV/µs to 150 kV/µs for three different technological processes and three temperature points from -40 °C to 125 °C.

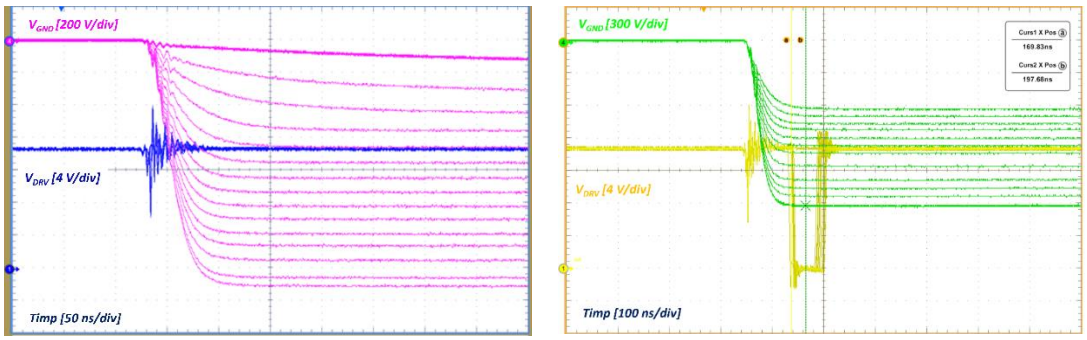
In the event of a negative CMT event occurring when V_{IN} is activated, *CM-EN* is set to 1 for 200 ns and enables the additional current source I_{TX-B} from Figure 4.11. V_{IN-L} remains high for all simulated conditions. Figure 5.14b shows the simulation results obtained when deactivating the TX-B and FP blocks. In this case, the negative CMT event appearing during V_{IN} = 5 V leads to oscillations stopping at the output of the transmission circuit due to I_{CMTI}. As a result, the control signal registers a false negative turn-off.

The experimental measurements were conducted on 5 circuits, at room temperature. Terminal *GND* was varied relative to *REF1*, using amplitudes from -200 V to -1500 V, in a time interval between 10 ns and 60 ns, resulting in slopes dV_{GND}/dt from 3 kV/µs to 150 kV/µs. For measurements obtained in Figure 5.15a, the TX-B and FB blocks are activated, and *DRV* remains high for all conditions tested. Comparative measurements were ran for a gate driver with the TX-B and FP blocks deactivated. Oscilloscope capture from Figure 5.15b shows that the output signal has a false turn off for different dV_{GND}/dt slopes.



a) b)

Figure 5.14 *CMTI simulation results with TX-B and FP a) enabled b) disabled*



a) b)

Figure 5.15 *V_{DRV} response to CMTI using amplitudes from -200 V to -1500 V and a 30 ns time interval with TXB and FP a) enabled b) disabled*

5.4 Comparison with commercialized circuits

The performance of the proposed gate driver from Figure 4.1 are compared with four current gate driver families [9][10][24]-[26], and the results are summarized in Table 5.1. The values measured for the parameters of the protection functions are similar, even higher, compared to the circuits studied. In addition, the proposed circuit is the only one that includes an extensive range of protection functions for the IGBT and for the internal blocks. Moreover, the protection function against negative supply terminal floating is not found in any of the gate drivers available on the semiconductor market. Common-mode transient immunity shows similar or superior results compared to most of the circuits studied.

Table 5.1 *Comparative table with current gate drivers.*

Parameter/ Function	Symbol	This work			UCC21750			1ED3322MC12N			STGAP4S			BM60052AFV-C		
		LSL	Mean	USL	LSL	Mean	USL	LSL	Mean	USL	LSL	Mean	USL	LSL	Mean	USL
$V_{UVLOS-OFF}$	V	11.7	12	12.3	9.9	11.8	12.3	11.9	12.6	-	11.3	12	12.6	10.9	11.5	12.1
$V_{UVLOS-ON}$	V	12.7	13	13.3	12	12.8	13.3	-	13.6	14.2	11.3	12	12.6	10.9	11.5	12.1
$V_{UVLOS-HYST}$	V	0.8	1	1.2	-	0.8	-	0.6	0.9	-	0.7	1	1.3	0.8	1.2	1.6
$V_{UVLOP-OFF}$	V	2.4	2.65	2.9	2.35	2.5	2.65	2.5	-	-	2.67	2.85	2.98	3.2	3.4	3.6
$V_{UVLOP-ON}$	V	2.6	2.8	3.0	2.55	2.7	2.85	-	-	3.1	2.7	2.9	3.04	-	-	-
$V_{UVLOP-HYST}$	mV	100	150	200	-	200	-	100	200	-	45	55	65	70	100	130
V_{DST}	V	8.7*	9	9.3*	8.5	9.15	9.8	8.5	9	9.5	8.3	9	9.4	6	6.4	6.8
I_{DST}	µA	440*	500	560*	430	500	570	438	510	582	460	500	540	300	335	370
Slow turn-off	-	√			√			√			√			√		
V_{CL-THR}	V	1.84*	2	2.16*	1.5	2	2.5	1.6	2.1	2.4	1.7	2	2.3	1.8	2	2.2
VEE1 floating	-	√			X			X			X			X		
V_{TS} - DC_{TPWM} = 10%	V		4			4.5			X			X			1.35**	
V_{TS} - DC_{TPWM} = 50%	V		2.88			2.5			X			X			2.59**	
V_{TS} - DC_{TPWM} = 90%	V		1.75			0.5			X			X			3.84**	
DC_{TPWM}	%	48.2*	50	51.2*	48.5	50	51.5		X			X		47**	50**	53**
f_{TPWM}	kHz	7	10	13	380	400	420		X			X		8**	10**	14**
IGBT OT	-	√			X			X			X			X		
Secondary block OT	-	√			X			X			√			X		
dV_{GND}/dt	kV/µs	150			150			300			100			100		

* Values calculated based on experimental results

** Values extracted from BM60059FV-C

Chapter 6
Conclusions

6.1 Results achieved

This thesis was dedicated to the analysis and design of a galvanically isolated gate driver for IGBTs. The aim was to develop and implement a robust mechanism for data communication through the isolation barrier. The proposed gate driver includes three integrated transformers that electrically separate the voltage domains and ensure signal transfer between the input and output blocks. The robust transmission of information is ensured primarily by the design and implementation of an extensive set of protection circuits which prevent improper operation of the gate driver and of the power switch. In addition, two new architectures were developed to monitor the negative supply terminal and to offer compatibility for applications with IGBTs that are not equipped with a temperature sensor. Two other proposed circuits optimize the transmission path in terms of area by encoding and decoding the error signals communicated to the microcontroller. Finally, a new configuration was developed to improve the common-mode transient immunity in order to maintain data communication integrity in noisy environments. The developed gate driver was implemented in a 0.25 μm and 5 V BCD technology, and its validation was completed through simulations and through experimental results.

Chapter 2 is dedicated to the performance analysis of power devices based on trends of the current electronics industry. The study focused on the insulated gate bipolar transistor, which is the most widespread power switch developed on silicon. The chapter highlights the cross-section of an IGBT and provides a detailed description of the static characteristics and switching processes, accompanied by the related mathematical relationships. Moreover, it was shown that during the switching processes, current and voltage overshoots can lead to the IGBT functioning outside the safe operating area. As a result, protection circuits are needed to compensate the undesirable effects.

Chapter 3 begins by presenting the basic structure of a gate driver, highlighting the role of the component blocks, input and output, and the functions performed by the interface circuit between them. In addition, this chapter analyzes a series of architectures described in the literature and used for the protection of the gate driver and of the power switch. The configurations studied include protection against supply under-voltage lockout, and protection against IGBT over-current, over-temperature, and parasitic turn-on.

The second part of Chapter 3 is focused on the data transmission within the gate driver. In this scope, different methods of electrical separation existing in the literature were compared, and the information was synthesized within a radar diagram. Thus, the

comparison highlights the undeniable advantages offered by galvanic isolation over conventional solutions. Moreover, the electrical separation based on inductive coupling offers superior CMTI performances, which is a critical parameter of gate drivers for power devices.

As a result, the analysis in Chapter 3 is subsequently focused on the transmission techniques used in galvanically isolated gate drivers with inductive coupling. The comparison of communication methods follows key parameters of the control system and it is represented graphically by means of a radar diagram. The amplitude modulation transmission technique, or On-Off Keying, satisfies the essential parameter for gate drivers, namely the common-mode transient immunity.

Chapter 4 presents the block diagram of the proposed gate driver and describes its operation. The architecture includes three transmission paths ensured by the integrated transformers: a direct path that transfers the control signal from the microcontroller, and two reverse paths through which the error signals are communicated, respectively, the IGBT temperature. The correct operation of the gate driver was guaranteed by improving the supply under-voltage lockout protection circuit, where new components were added to allow the supply voltage to be monitored using a 5 V technology, and to eliminate partial pulses when returning to normal operation. Similar elements were also used for the circuits that prevent the erroneous operation of the power device, namely, the over-current protection circuit and the parasitic turn-on protection circuit.

In the same chapter, two new architectures are introduced for verifying the operating conditions of the power switch. This category includes the protection circuit against the negative supply terminal floating. The block monitors the negative supply pin and transmits an external error signal when the terminal is floating. This protection function is specific to the proposed gate driver and does not appear in the structure of any of the gate drivers currently available on the market. Moreover, the IGBT over-temperature protection block includes an original structure, used to offer compatibility for applications with IGBTs without a temperature sensor.

In addition to the protection circuits, chapter 4 details new blocks developed for the optimization of the transmission paths. Two original architectures optimize the circuit area by encoding and decoding the error signals transferred through the galvanic isolation barrier. Thus, a single communication path is used to transmit five error signals reporting improper operation of the gate driver or of the IGBT.

Chapter 4 ends with information about the design of the transmission circuit. A negative-g_m LC oscillator uses the primary winding of the corresponding integrated transformer to transmit the information through the galvanic isolation barrier. The chapter presents a series of CMTI testing methods described in the literature, and details the effects of *GND* variation on the LC tank oscillator. Thus, the transmission circuit is sensitive to negative CMT event and active input signal. As a result, an innovative architecture was proposed to prevent false turn-off of the control signal during the aforementioned conditions.

The performance of the proposed gate driver was evaluated in **Chapter 5** by means of simulations and experimental results. The chapter begins by presenting the complete schematic of the gate driver developed in the Cadence Virtuoso environment using

BSIM3v3 models. Once validated, the circuits were manufactured in a 5 V and 0.25 μm BCD technology, and packaged in SOIC16 plastic capsules.

The proposed protection circuits were initially verified through simulations, with the scope of conducting a functional comparison with the ideal waveforms. Thus, the simulations results for the improved protection blocks and for the proposed new architectures are in agreement with the ideal behavior. The second part of the verifications is based on experimental results, which analyze the responses of the output signal, *DRV*, and of the error signals. The measurements results reveal the proper functionality of the proposed gate driver, confirming the simulation results.

Chapter 5 also presents statistical data based on experimental validation of the design parameters for the protection circuits against supply under-voltage lockout ($V_{UVLOS\text{-}ON}$, $V_{UVLOS\text{-}OFF}$, $V_{UVLOS\text{-}HYST}$, $V_{UVLOP\text{-}ON}$, $V_{UVLOP\text{-}OFF}$, $V_{UVLOP\text{-}HYST}$), IGBT over-current (V_{DST}, I_{DST}) and IGBT parasitic turn-on ($V_{CL\text{-}THR}$). The results were obtained after testing 70 circuits in the temperature range between -40 °C and 125 °C. The process capability, CPK, is greater than 2 for all the parameters. This ensures that the process and temperature variation is within the ±6σ limits. A similar analysis is performed for the parameters associated with the IGBT over-temperature protection circuit, DC_{TPWM} for V_{TS} = 2.875 V, and f_{TPWM}. In this case, 70 circuits were tested at 25 °C and the CPK was 3.61. In addition, the temperature variation of the parameters was analyzed by testing 3 circuits at temperatures between -40 °C and 125 °C.

The last part of Chapter 5 assesses the common-mode transient immunity of the proposed gate driver. The new architectures introduced to improve CMTI performances were tested on 5 circuits measured at 25 °C, using amplitudes between -200 V and -1500 V, with a time duration ranging from 10 ns to 60 ns. The output signal was not affected in any of these conditions and remained active. Thus, the gate driver is immune to common mode transients with slopes up to 150 kV/μs. Moreover, the efficiency of the developed architectures was confirmed by performing a similar set of tests on a gate driver in which the aforementioned circuits were disabled. In this case, the control signal exhibited false turn-off for CMT slopes between 20 kV/μs and 70 kV/μs.

Finally, also in chapter 5 a comparison is performed between the proposed gate driver and four families of gate drivers available on the semiconductor market. The proposed circuit shows a smaller variation for the parameters associated with the protection function against supply under-voltage lockout, $V_{UVLOS\text{-}ON}$ and $V_{UVLOS\text{-}OFF}$. Comparable results were obtained for the parameters of the IGBT over-current protection circuit, V_{DST} and I_{DST}, and of the IGBT parasitic turn-on protection block, $V_{CL\text{-}THR}$. CMTI performances are similar, even superior, compared to three of the four circuits analyzed. The proposed gate driver is differentiated by integrating an extensive set of protection blocks. The circuit includes a new protection function, which monitors the disconnection of the negative supply terminal. Moreover, the implemented circuit is the only one that transmits the temperature information of the IGBT using two different isolation paths, thus ensuring the communication of the erroneous condition even in case one of the transfer paths is damaged.

6.2 Original contributions

This thesis includes a series of original elements, presented during the research period in various publications. These include specialized conferences, scientific journals and profile events. The following original aspects are highlighted:

- ✓ Summaries from the literature on:
  - ➢ Evolution of power devices and analysis of their performance in the current context of the electronics industry.
  - ➢ The peculiarities of the insulated gate bipolar transistor, including the cross-section, static characteristics, switching processes, and safe operating area, accompanied by related mathematical equations.
  - ➢ Actual protection techniques used in gate drivers for IGBTs, including supply under-voltage lockout protection, IGBT over-current, over-temperature, and parasitic turn-on protections.
  - ➢ Comparative study of electrical separation methods used in gate drivers for power devices.
  - ➢ Comparative study of transmission techniques within galvanically isolated gate drivers with inductive coupling.
- ✓ Design of improved architectures for protection circuits integrated into the structure of the proposed gate driver. The improvements consist of adapting the structures to 5 V technology, eliminating partial pulses when returning to normal operation, and reducing the current consumption:
  - ➢ Design and simulation of circuits for the supply under-voltage lockout protection of the component blocks [1],[2].
  - ➢ Implementation and verification of a method for IGBT over-current protection [1],[2].
  - ➢ Design and validation of an architecture for the prevention of IGBT parasitic turn-on due to the current injected by the Miller capacitance [1].
  - ➢ Implementation and simulation of protection techniques against over-temperature of the gate driver and over-temperature of the IGBT [3].
- ✓ Development and design of new architectures to ensure robust data communication through the galvanic isolation barrier:
  - ➢ Transmission of IGBT temperature information using two communication paths to ensure redundancy in its measurement [3].
  - ➢ Design and verification of an architecture that disables the IGBT over-temperature detection function when the terminal is floating. This feature provides compatibility with applications that use a power switch without a temperature sensor [3].

- Implementation and simulation of a configuration for protection against the disconnection of the negative supply terminal of the gate driver [4].
- Implementation and verification of coding and decoding architectures for the error signals transmitted through the galvanic isolation barrier to optimize the circuit area [1][2][3].
- Design and simulation of methods to improve common-mode transient immunity that keep the control signal active in the event of a negative CMT event. The proposed architecture was the subject of a paper presented at the IEEE 49th European Solid State Circuits Conference (ESSCIRC) [5].

✓ Implementation of the gate driver containing the proposed architectures in a BCD technology of 0.25 μm and 5 V [1], [2], [4], [5].

✓ Validation through simulations and measurements of the correct operation of the proposed gate driver:

- Functional validation of improved protection methods and comparison of the experimental results with simulations [1], [2].
- Testing of 70 circuits in the temperature range from -40 °C to 125 °C and processing of statistical data for parameters associated with protection functions against supply under-voltage lockout, IGBT over-current and IGBT parasitic turn-on.
- Validation of the IGBT over-temperature protection circuit by measuring 70 circuits at 25 °C, as well as testing 3 circuits in the temperature range from -40 °C to 125 °C.
- Testing the new architecture used to disable the IGBT over-temperature monitoring function when the terminal is floating.
- Validation of the new architecture for protection against the disconnection of the negative supply terminal of the gate driver [4].
- Validation of new configurations used to improve CMT performances. Measurements were conducted for CMT slopes from 3 kV/μs to 150 kV/μs. The efficiency of the developed architectures was confirmed by performing a similar set of tests on a gate driver in which the circuits for improving noise immunity are disabled [5].

✓ Comparison of the proposed gate driver with 4 families of gate drivers for IGBTs available on the semiconductor market.

6.3 List of original works

[1] **I. Hurez**, T. Chen, F. Vladoianu, V. Anghel, G. Brezeanu, "*Galvanically Isolated IGBT Gate Driver with Advanced Protections and A Fault Detection Reporting Method*," in **Romanian Journal of Information Science and Technology (ROMJIST)**, Vol.22, no. 1, 2019, pp. 69-84, Q1 (2024), IF = 3.7, ISI, **WOS: 000469865900006**.

[2] **I. Hurez**, T. Chen, F. Vladoianu, V. Anghel, G. Brezeanu, "*Message Recovered: A Robust Fault Detections and Reporting Method for Galvanically Isolated IGBT Gate Drivers*", in **Proceedings of the International Semiconductor Conference (CAS)**, 10-12 Oct. 2018, Sinaia, Romania, pp. 205 – 208, ISI, **WOS: 000514386700040, DOI 10.1109/SMICND.2018.8539764**.

[3] K. Song, **I. Hurez**, V. Anghel "*Gate Driver with Temperature Monitoring Features*", Patent, **US11881857-B2**, Granted 23. Ian. 2024.

[4] **I. Hurez**, K. Song, A. Enache, V. Anghel, G. Brezeanu "*To Float or Not To Float – Negative Supply Diagnostic for Gate Drivers*", in **Proceedings of the International Semiconductor Conference (CAS),** 12-14 Oct. 2022, Poiana Brasov, Romania, pp. 149 – 152, IEEE, DOI 10.1109/CAS56377.2022.9934311.

[5] **I. Hurez**, V. Anghel, G. Brezeanu "*A Negative-Gm Oscillator with Common Mode Transient Immunity Enhancements for Galvanically Isolated Gate Drivers*" in **Proceedings of the IEEE 49th European Solid State Circuits Conference (ESSCIRC)**, 11-14 Sep. 2023, Lisbon, Portugal, pp. 245 – 248, IEEE, DOI 10.1109/ESSCIRC59616.2023.10268713.

[6] F. Vladoianu, M. Strelec, **I. Hurez**, V. Anghel, G. Brezeanu "*Changing the Paradigm in Common Mode Transient Immunity (CMTI) Testing of Dual Channel Galvanically Isolated Gate Drivers*", in **Proceedings of the International Semiconductor Conference (CAS)**, 6-8 Oct. 2021, Romania, pp. 125-128, ISI, **WOS: 000853482700024**, DOI 10.1109/CAS52836.2021.9604169.

[7] **I. Hurez**, V. Anghel, F. Vladoianu, G. Brezeanu "*A Disruptive Technology – Improving Half-Bridge Gate Driver Performances Using Galvanic Isolation*", in **Proceedings of the International Semiconductor Conference (CAS)**, 9-11 Oct. 2019, Sinaia, Romania, pp. 137-140, ISI, **WOS: 000514295300028**, DOI 10.1109/SMICND.2019.8923899.

[8] F. Vladoianu, K. Song, **I. Hurez**, V. Anghel, G. Brezeanu "*A Tale of Two Circuits – Comparing Performances of Input Adapters As Interface Elements for High Voltage Applications*", in **Proceedings of the International Semiconductor Conference (CAS)**, 7-9 Oct. 2020, Sinaia, Romania, pp. 119-122, ISI, **WOS: 000637264600027, DOI 10.1109/CAS50358.2020.9267973**.

[9] A Dragan (Vasile), A. Negut, A. Enache, **I. Hurez**, V. Anghel, G. Brezeanu, "*In Focus: Data Hold Time for Temperature Sensors with High Speed I2C Interface*", in **Proceedings of the International Semiconductor Conference (CAS)**, 11-13 Oct. 2023, Sinaia, Romania, pp. 111-114, IEEE, DOI: 10.1109/CAS59036.2023.10303655.

[10] A. G. Banu, S. Stamate, V. Anghel, **I. Hurez**, S. Mihalache "*The Jack-of-all-Trades: a Multi-Function Pin for Dead-Time Control*", accepted for presentation at the **International Semiconductor Conference (CAS) 2024**.

[11] S. Stamate, A.G. Banu, V. Anghel, **I. Hurez**, V. Bricicaru, F. Draghici "*Advanced Protection Functions for Smart IGBT Gate Drivers are Paving the Road to Damage-Free Systems*", acceptată pentru prezentare la **International Semiconductor Conference (CAS) 2024**.

6.4 Prospects for further development

Future research will consider the design and implementation of specialized protection functions for gate drivers for MOS transistors developed in silicon carbide technology. This category includes a function known in the literature as *Active Short Circuit*, in which the power device is activated to create a system-wide short-circuit that discharges the accumulated charge.

Moreover, SiC MOSFETs require minimizing reaction time for over-current protection. For this purpose, the protection circuit uses an external resistor connected to an auxiliary terminal of the power device. Such an architecture allows a reaction time of less than 1 μs to be obtained, and the initial results obtained were included in a paper accepted for rpesentation at the International Semiconductor Conference (CAS) 2024.

- S. Stamate, A.G. Banu, V. Anghel, **I. Hurez**, V. Bricicaru, F. Draghici "*Advanced Protection Functions for Smart IGBT Gate Drivers are Paving the Road to Damage-Free Systems*", accepted for presentation at **International Semiconductor Conference (CAS) 2024**.

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[14] F. Vladoianu, K. Song, **I. Hurez**, V. Anghel, G. Brezeanu "*A Tale of Two Circuits –*

Comparing Performances of Input Adapters As Interface Elements for High Voltage Applications,", in Proceedings of the International Semiconductor Conference (CAS), 7-9 Oct. 2020, Sinaia, Romania, pp. 119-122, ISI, WOS: 000637264600027, DOI 10.1109/CAS50358.2020.9267973.

[15] **I. Hurez**, K. Song, A. Enache, V. Anghel, G. Brezeanu "*To Float or Not To Float – Negative Supply Diagnostic for Gate Drivers,*", in Proceedings of the International Semiconductor Conference (CAS), 12-14 Oct. 2022, Poiana Brasov, Romania, pp. 149 – 152, IEEE, DOI 10.1109/CAS56377.2022.9934311.

[16] A Dragan (Vasile), A. Negut, A. Enache, **I. Hurez**, V. Anghel, G. Brezeanu, "*In Focus: Data Hold Time for Temperature Sensors with High Speed I2C Interface,*", in Proceedings of the International Semiconductor Conference (CAS), 11-13 Oct. 2023, Sinaia, Romania, pp. 111-114, IEEE, DOI: 10.1109/CAS59036.2023.10303655.

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