NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY POLITEHNICA BUCHAREST

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Ph.D. THESIS SUMMARY

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SENSOR SIGNAL CONDITIONING CIRCUITS

THESIS COMMITTEE

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Content

Chapter 1

Introduction

1.1 Presentation of the field of the doctoral thesis

Hydrogen (H_2) has long been identified as a potential substitute for fossil fuels. It is climate neutral if obtained through water electrolysis using regenerable energy. Given the accelerating rate of global climate change, determined by CO_2 emissions generated through hydrocarbon consumption, developing alternate energy sources is becoming even more critical.

The main limiting factor for hydrogen adoption as an energy source is safety, since it is a highly explosive gas, in a wide range of concentration (from 4% up to 75%). Thus, it becomes necessary to have accurate and reliable sensors, accompanied by equally performant signal conditioning (processing) circuits.

In the case of sensing structures for H_2, those developed on semiconductor substrates have been proven to have very good sensitivity, long lifespan, small size and reduced cost. Oftentimes, these structures have a Metal-Oxide-Semiconductor (MOS) structure, leading to a nonlinear capacitance behavior. When these sensors are heated up to high temperatures, gas sensitivity and response times significantly improve, allowing for rapid detection of concentrations as low as tens of ppm. In this manner, leaks can be identified early, before concentrations in the explosive range are reached.

Nevertheless, any sensor requires an analog signal conditioning circuit. In the case of MOS structures for H_2 detection, the main research effort has been previously directed mostly towards sensors development. Their characteristics are extracted under laboratory conditions, using characterization systems. Conversely, fewer solutions have been reported for the analog conditioning circuits. A possible cause is the nonlinear capacitance of the MOS structure, which requires dedicated topologies to address.

Consequently, the doctoral thesis proposes an innovative approach for MOS sensor signal processing, based on using the well-known Phase-Locked Loop (PLL) architecture as an interface for such nonlinear structures. A typical PLL circuit includes a Voltage-Controlled Oscillator (VCO – having a variable frequency). The PLL adjusts its control voltage in order to obtain a constant phase difference between its output signal and a reference signal. The simplest method of creating such an oscillator is to include in its resonant circuit a nonlinear capacitance, with the bias determined by the control voltage (for instance, the capacitance of a H_2 MOS sensor).

1.2 Scope of the doctoral thesis

The scope of the doctoral thesis includes establishing the architecture, as well as the design, simulation, implementation using discrete components (Printed Circuit Board – PCB) and experimental validation of an analog PLL signal conditioning circuit for MOS capacitor H_2 sensors (nonlinear capacitance). The circuit should reproduce the conditions under which the sensors are characterized, albeit in a portable form.

1.3 Content of the doctoral thesis

Chapter 2 begins with a description of the role that signal conditioning circuits have in measurement systems for non-electrical quantities, as well as the performances they should achieve. Common gas sensor types are presented, followed by the analysis of two circuit architectures used for capacitive sensors and their limitations.

Chapter 3 targets the MOS capacitor H_2 sensor used in this application, which is built on a silicon carbide substrate (SiC). Small-signal capacitance and resistance versus bias voltage characteristics are extracted. The capacitance-voltage (C-V) curve evinces a left shift when the sensor is exposed to H_2, an effect utilized in the signal conditioning circuit. Moreover, a low parallel resistance is observed, which needs to be accounted for during the circuit design. SPICE models are developed for the sensor and a method for replacing it with varicap diodes is identified. Finally, arguments are given for a constant capacitance measurement principle, which leads to a PLL architecture.

Chapter 4 opens with a description of the requirements for the PLL circuit. A Charge-Pump PLL (CP-PLL) architecture is selected, which contains a Voltage Controlled Oscillator (VCO), a Phase Frequency Detector (PFD), a Charge Pump (CP) and a Low-Pass Filter (LPF). Moreover, a Reference Oscillator (REFO) similar to the VCO within the loop is used for generating the PLL input signal. A dedicated Supply Circuit provides two DC voltages required by the PLL blocks, while ensuring noise resistance. For all the listed blocks, dedicated schematics are developed, starting from well-known basic topologies.

Chapter 5 describes the component selection process, as well as the verification of the CP-PLL through simulation. Moreover, a continuous linear time invariant system of the PLL is developed, in order to evaluate its dynamic behavior and stability. With the fully designed blocks, simulations are carried out on the complete circuit and an error source for the CP-PLL is identified. A way of reducing this error is also proposed, which utilizes a first technique, named Calibration Method 1 (CM1).

Chapter 6 is focused on the physical implementation and validation through measurements of the CP-PLL conditioning circuit. Three variants are presented, used to identify some of the issues solved in the design. Moreover, a Calibration Method 2 (CM2) is proposed, with which the circuit precision can be experimentally evaluated. Finally, the accuracy of the proposed CP-PLL topology is demonstrated through the evaluation of its electrical performances, as well as through H_2 detection measurements.

Chapter 2

Sensors and Conditioning Circuits

2.1 Data acquisition methods

Modern systems for measuring non-electrical quantities include, along sensors, their associated analog interfacing circuits, as well as a significant digital processing part [1],[2],[3], as illustrated in Fig. 2.1.

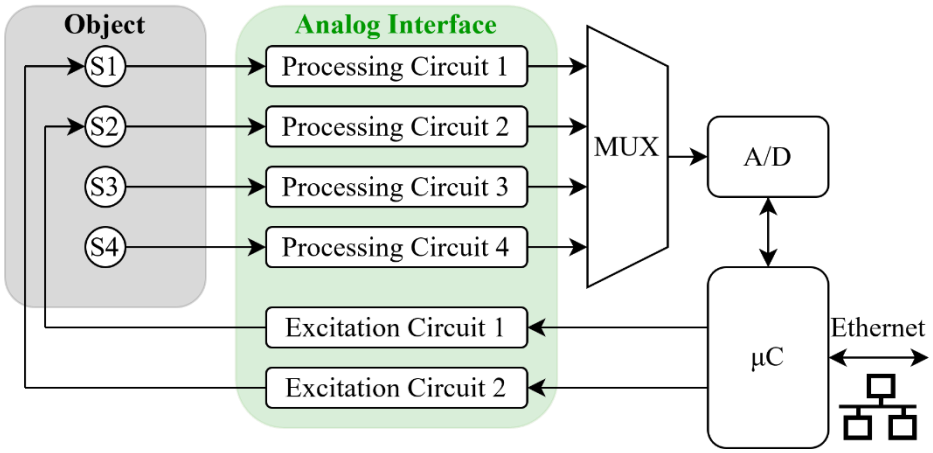


Figure 2.1 *Block schematic of a data acquisition system*

Two types of sensors were illustrated in Fig. 2.1: active (S1, S2 – require external electrical energy) and passive (S3, S4 – convert the non-electrical stimulus energy into electrical energy). Thus, the analog interfacing circuit can have both a signal processing function, as well as a sensor excitation role [1],[2],[3],[4],[5]. For instance, for the utilized MOS H_2 sensor, excitation includes a DC bias voltage and a small-signal oscillation – the quantity of interest is the high frequency small-signal capacitance [6],[7],[8],[9]. Nevertheless, for simplicity, the analog sensor interface will be hereafter referred to as a "conditioning circuit" or a "processing circuit".

For these interfacing circuits, the key performances are [1],[2],[3],[4],[5]: input impedance (adapted to the output impedance of the sensor), offset, gain (the ratio between the output quantity and the input one), linearity (for simple non-electrical quantity estimation), bandwidth (set considering a compromise between noise and response time), stability (in the case of circuits with feedback).

2.2 Gas sensors

The most common gas sensor types are [1],[2],[3],[4],[10]:

- Electrochemical sensors – used for electrochemically active gas species;
- Catalytic sensors – based on the temperature variation of a resistive element;
- NDIR sensors ("Non-Dispersive Infrared") – spectroscopic devices;
- PID sensors ("Photo-Ionization Detector") – photon bombardment of gas;
- Semiconductor sensors – formed through the deposition of a metal or a metal oxide on a semiconductor substrate [7],[10]. The MOS capacitor used in this thesis represents such a capacitive device.

2.3 Conditioning circuits for capacitive sensors

A first analyzed circuit is based on the differential measurement principle (comparison with a reference structure) and utilizes a quad-diode bridge [11]. The topology was conceived for linear capacitive MEMS sensors [11] and is thus difficult to adapt for the nonlinear MOS structure used in this application [12].

A second analyzed architecture (likewise differential – Fig. 2.2), is based on the change in the resonant frequency of bandpass RLC structures and was conceived specifically for MOS capacitor H_2 sensors [12]. For this topology, there is a significant disadvantage given by the nonlinear dependency of V_{OUT} on the sensor capacitance [12]. Moreover, before the signal $v_s(t)$ (containing the H_2 concentration information) is amplified by the $+G$ block (Fig. 2.2), it has a low amplitude and is susceptible to noise.

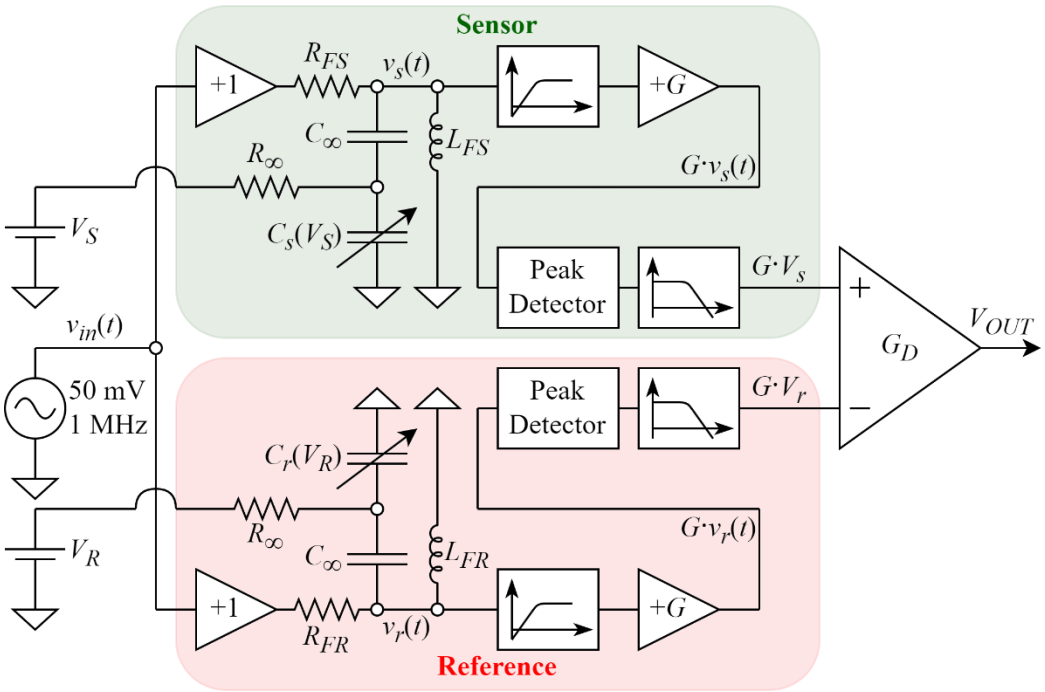


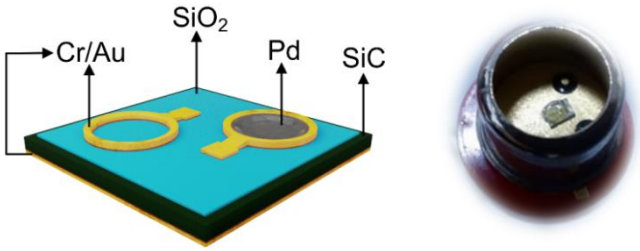
Figure 2.2 *Circuit with RLC bandpass filters for MOS capacitor sensors [12]*

Chapter 3

SiC-MOS Gas Sensor

3.1 Sensor structure and characteristics

The utilized H_2 sensor is a MOS capacitor, built on an n-type silicon carbide (SiC) substrate, [6],[7],[8],[9],[12]. Its role is to convert the H_2 concentration into a nonlinear capacitance. The sensor has a dual structure (Fig. 3.1.a) and is encapsulated in a TO39 package (Fig. 3.1.b) [7]. The sensor itself uses palladium (Pd) as the gate metal, well known for its catalytic role in H_2 adsorption [7]. A second structure (reference), without the Pd layer, is used for parasitic capacitance evaluation [8]. The ohmic substrate contact on the bottom of the die (*B*), as well as the gate contact for the active sensor structure (*G*) are developed using Chromium (Cr) and Gold (Au).



(a) (b)

Figure 3.1 *SiC-MOS sensor: (a) physical structure [7] (b) encapsulated structure [7]*

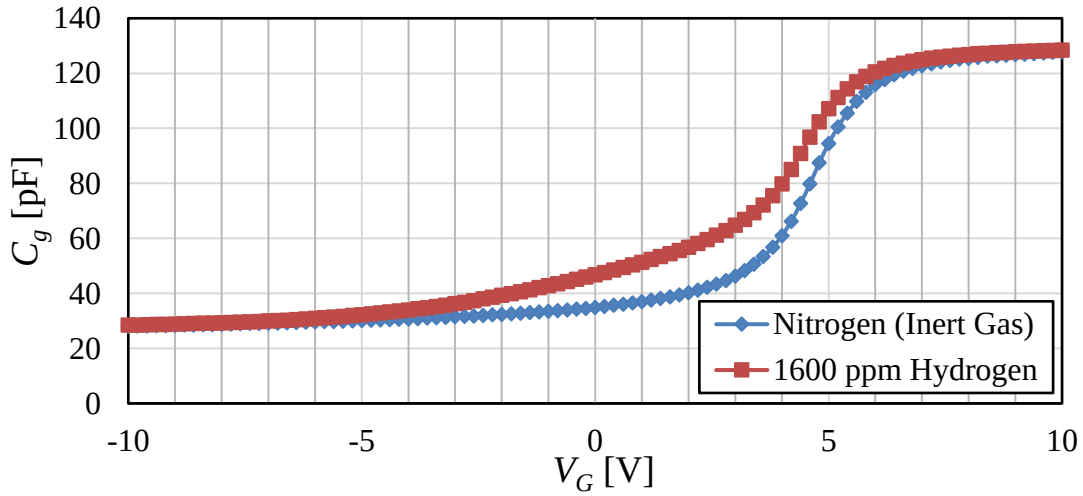


Figure 3.2 *$C_g(V_G)$ characteristics of SiC-MOS sensor at θ = 100 °C in an atmosphere of N_2 (blue) and in the presence of a 1600 ppm H_2 concentration (red)*

The main sensor characteristic is the high frequency small-signal capacitance variation with the gate bias ($C_g(V_G)$ – Fig. 3.2) [6]. It was extracted experimentally with a Keithley 4200-SCS characterization system A MOS sensor with the structure from Fig. 3.1 was considered, heated up to 100 °C, both in an inert atmosphere (100% N_2) and with 1600 ppm H_2. The substrate *B* is tied to ground and the DC bias voltage of the gate *G* is swept between -10 V and 10 V. In order to measure the capacitance, a small sine signal (100 mV_{pp} peak-to-peak amplitude) with a frequency of 1 MHz is applied.

On the graph obtained in N_2 (Fig. 3.2) the three operating regions of a MOS capacitor are observed [6],[14],[15]: inversion (V_G < 3 V), depletion (V_G between 3 and 6 V) and accumulation (V_G > 6 V). The effect of H_2 is most significant in the depletion region, where the capacitance varies strongly with the bias – the left-shift of the C-V characteristic. Thus, in the developed circuit, the sensor must be biased in this region.

Together with the $C_g(V_G)$ plots, the variation of the parallel parasitic resistance $R_g(V_G)$ is extracted under the same conditions. The characteristics in Fig. 3.3 are thus obtained. The minimum resistance value is around 20 kΩ (in the depletion region). It should be noted that both $C_g(V_G)$ and $R_g(V_G)$ are influenced by the ambient conditions during and before the measurement (for instance, temperature and humidity) [7].

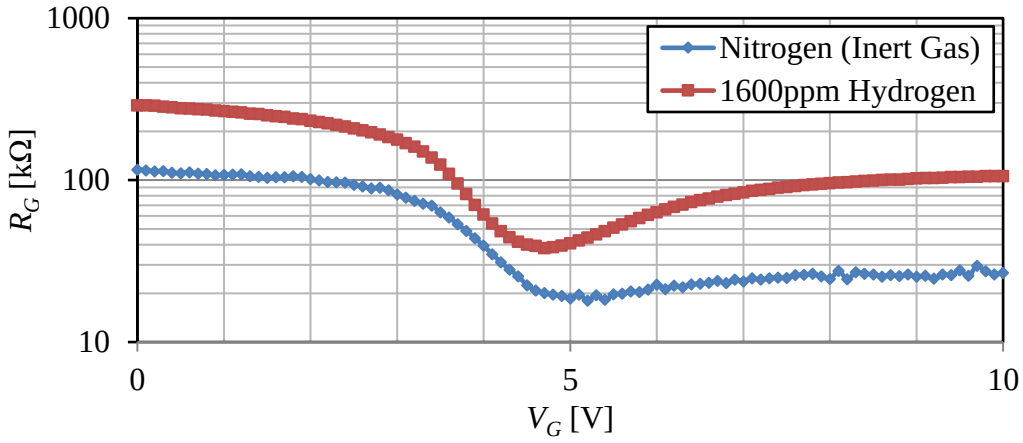


Figure 3.3 *Resistance-voltage characteristics of SiC-MOS sensor at θ = 100 °C in an atmosphere of N_2 (blue) and in the presence of a 1600 ppm H_2 concentration (red)*

3.2 SPICE modeling of the SiC-MOS sensor

In the case of the SiC-MOS sensor, the development of a SPICE model, for use in simulations with the conditioning circuit, is desired. Thus, an accurate emulation of characteristics such as those from Fig. 3.2 and Fig. 3.3 is critical. Consequently, the following approaches for modeling the sensor were investigated:

1) Using a known model and extracting its parameters – e.g., BSIM model [16];
2) Developing a new model based on the device physics and the associated equations – such as the *p-diode* model for Schottky diodes [12],[17],[18],[19];
3) Developing a behavioral model – for instance, in the Verilog-A language [20];
4) Modeling using an alternate device with similar characteristics – allows for system calibration without the influence of ambient conditions [21].

For the MOS sensor, approaches 3 and 4 are used. In the case of method 3, the device is modeled as a nonlinear capacitance in parallel with a nonlinear conductance:

$$i_{GB}(t)=C_g\left(v_{GB}(t)\right)\cdot\frac{\mathrm{d}v_{GB}(t)}{\mathrm{d}t}+G_g\left(v_{GB}(t)\right)\cdot v_{GB}(t) \qquad (3.1)$$

For the two nonlinear quantities, the experimental data in Fig. 3.2 and Fig. 3.3 is used. In the case of the resistance/conductance, which is noisier (Fig. 3.3), numerical filtration is carried out using Matlab. [22]. The resulting data sets are included in two Verilog-A models implementing equation (3.1), using the *$table_model* function [20]:

```
`include "constants.vams"
`include "disciplines.vams"

module MOS_Sensor(G, B);

inout G, B;
electrical G, B;
real c,g;

analog begin
 c=$table_model((V(G,B)),"cap.txt","3CC");
 g=$table_model((V(G,B)),"cond.txt","3CC");
 I(G,B) <+ c * ddt(V(G,B)) + g * V(G,B);
end

endmodule
```

```
`include "constants.vams"
`include "disciplines.vams"

module MOS_Sensor(G, B);

inout G, B;
electrical G, B;
real c,g;
real y [0:1];

analog begin
 c=$table_model((V(G,B)),"cap.txt","3CC");
 g=$table_model((V(G,B)),"cond.txt","3CC");
 y[0] = g;
 y[1] = c;
 I(G,B) <+ laplace_nd(V(G,B)), y, {1});
end

endmodule
```

The first model (left side) represents a time-domain implementation, while the second (right side) is in the frequency-domain. Thus, as could be expected, simulations carried out to validate the two models indicated that the first one is more appropriate for *transient* analysis (time) and the second one for *AC* analysis (frequency).

For method 4, it was determined that a similar C-V characteristic can be obtained with two SMV1237 varicap diodes [23] connected in parallel (Fig. 3.4). Using the diode parameters [24] and V_+ = 7 V, the plots from Fig. 3.5 are obtained.

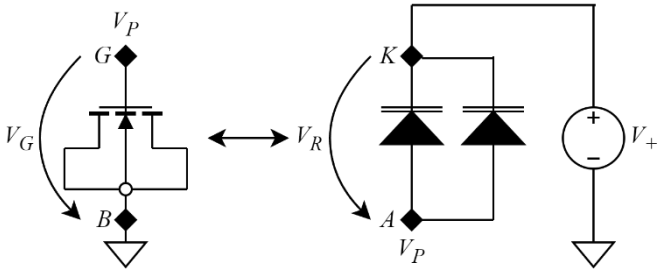


Figure 3.4 *Equivalence between MOS sensor and two varicap diodes*

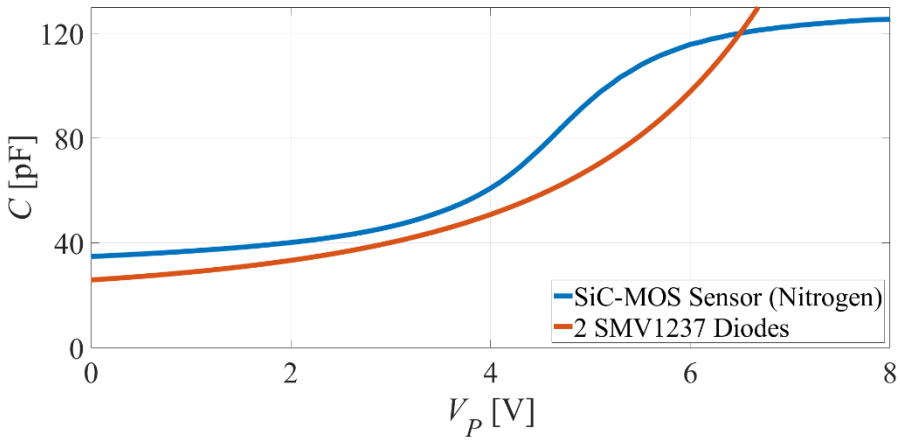


Figure 3.5 *C-V plots: MOS sensor (in nitrogen) vs. two SMV1237 diodes in parallel*

3.3 Measurement principles for the SiC-MOS sensor

The conditioning circuit transforms the left-shift of the $C_g(V_G)$ sensor curve as a result of H_2 influence into the variation of a single electrical quantity. For this purpose, two principles may be used, shown in Fig. 3.6 (includes plots from Fig. 3.2) [6],[7],[25]:

a. **Principle V_G = const** (denoted by *a* – Fig. 3.6) – the V_G voltage is kept constant and the capacitance C_g is the measured variable. This approach is also used in the circuit from Fig. 2.2 [12], while another implementation method involves using a Voltage-Controlled Oscillator (VCO) [6],[25];

b. **Principle C_g = const** (denoted by *b* – Fig. 3.6) – the sensor capacitance is maintained constant, by adjusting V_G as the H_2 concentration changes. This technique leads to a Phase-Locked Loop (PLL) circuit architecture [26]. The PLL comprises a Controlled Oscillator, which in turn includes the SiC-MOS sensor. Thus, by adjusting V_G in order to maintain a constant frequency for the oscillator, C_g also becomes invariant.

Between the two approaches, the **C_g = const** principle is preferred due to three major advantages versus the VCO implementation of the **V_G = const** technique [6],[7]:

- Linearity – a PLL circuit generates the same shift in the bias voltage seen in the C-V plots (at a certain set constant capacitance);
- The output quantity is a voltage – easier to process in a portable solution compared to frequency;
- The working frequency is constant and can be made equal to the characterization value (1 MHz) – preferrable due to the dependency of the MOS capacitance dependence on frequency [14]. Therefore, large variations compared to the characterization frequency can lead to changes in the MOS sensor $C_g(V_G)$ curve, negatively impacting measurement accuracy.

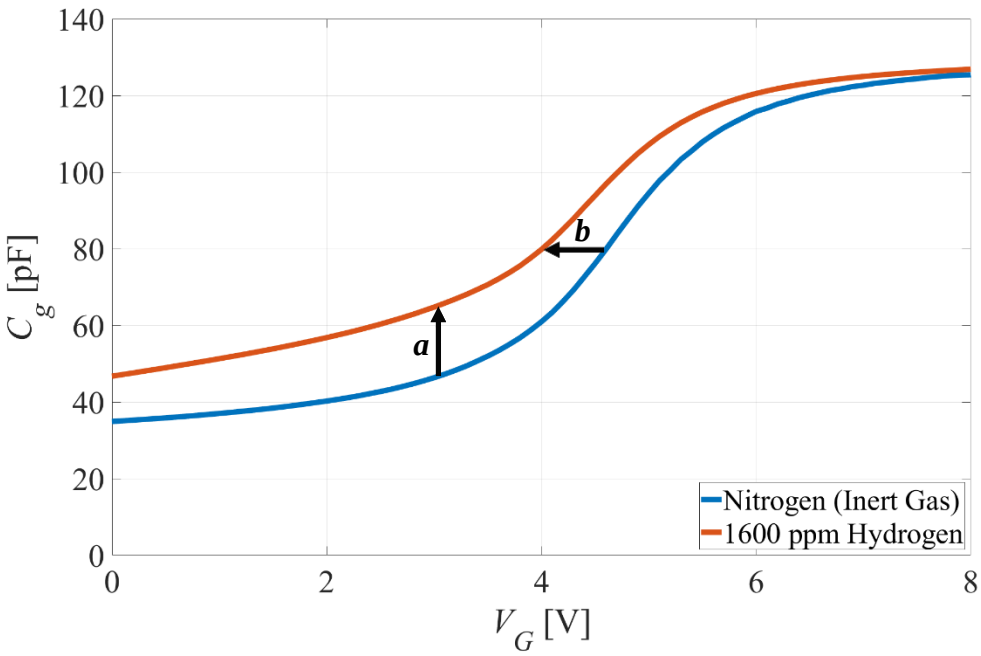


Figure 3.6 *Measurement principles using the MOS sensor*

Chapter 4

Architecture of Sensor Signal Conditioning Circuit

4.1 PLL conditioning circuit

Based on the sensor characterization, the following design requirements are imposed for the PLL conditioning circuit:

1) Sensor substrate tied to ground – same connection as in characterization;
2) Sensor bias voltages in the 1...6 V range – depletion region;
3) 1 MHz operating frequency – the value used in characterization;
4) Small-signal operation of the sensor (≤100 mV_{pp}) – linear AC behavior;
5) Correct operation with a low sensor parasitic resistance ($R_g \geq 20$ kΩ);
6) Circuit errors ≤100 mV – for H_2 detection, errors equal to roughly 10-15% of the $C_g(V_G)$ shift between 0 and 1600 ppm (Fig. 3.2) are accepted [21];
7) Possibility to calibrate – for error compensation.

A Charge-Pump PLL (CP-PLL) architecture was selected for the proposed conditioning circuit, with the block schematic shown in Fig. 4.1 [21],[27].

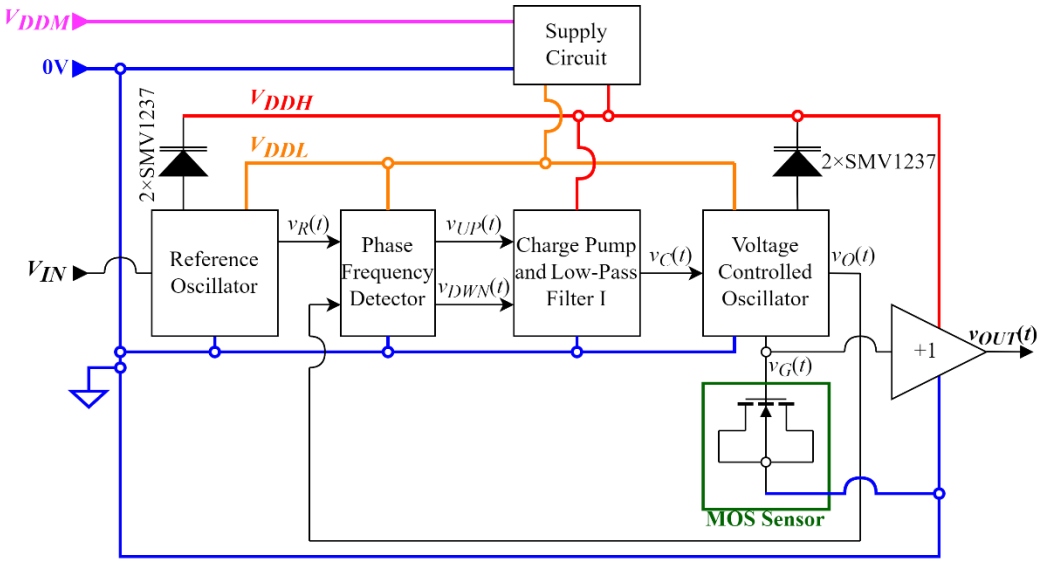


Figure 4.1 *CP-PLL circuit block schematic*

The CP-PLL circuit in Fig. 4.1 comprises the following blocks:

- Voltage-Controlled Oscillator (VCO) – generates $v_O(t)$, with the frequency f_{osc} determined by the control voltage $v_C(t)$, through the variation of C_g with V_G (the latter imposed by $v_C(t)$) and applies a small sensor signal (≤100 mV_{pp});
- Reference Oscillator (REFO) – nearly identical to the VCO, generates the reference signal $v_R(t)$, with the frequency f_{ref} set by the input voltage V_{IN}. The sole difference is that the REFO only contains varicap diodes (no sensor);
- Phase Frequency Detector (PFD) – generates signals $v_{UP}(t)$, $v_{DWN}(t)$, whose duty cycles η_{UP}, η_{DWN} vary with the phase shift between $v_R(t)$, $v_O(t)$;
- Charge Pump (CP) and Low-Pass Filter I (LPF I) – together they generate the control voltage $v_C(t)$ for the VCO, based on the duty cycles of $v_{UP}(t)$, $v_{DWN}(t)$;
- Voltage Follower +1 – allows for $v_G(t)$ readout (the output quantity influenced by concentration) without perturbing VCO operation;
- Supply Circuit – starting from a main voltage V_{DDM}, the block generates two voltage levels for supplying the PLL (V_{DDL} – for the oscillators and detector; V_{DDH} – for biasing the sensor in the depletion region through the CP-LPF I);

The CP-PLL operates using negative feedback. When H_2 concentration rises, the C-V sensor characteristic shifts to the left (Fig. 3.2), so C_g tends to increase initially. Consequently, f_{osc} decreases, leading to $f_{osc} < f_{ref}$. Thus, the edges of $v_O(t)$ appear less often than those of $v_R(t)$, which translates, on average, to $\varphi_{osc} < \varphi_{ref}$. Based on the PFD's mode of operation, the result is $\eta_{DWN} < \eta_{UP}$. Then, CP-LPF I is designed in such a manner that $\eta_{DWN} < \eta_{UP}$ leads to a decrease in $v_C(t)$ and therefore in the sensor bias V_G. A V_G reduction translates into falling C_g and thus into an f_{osc} increase – variation in the direction opposite the initial one implies negative feedback. The process continues until the PLL returns to the lock condition: $f_{osc} = f_{ref} \Leftrightarrow \Delta\varphi = \text{const} \Leftrightarrow v_C(t) = \text{const}$ [7],[26].

4.2 Voltage controlled oscillator

The proposed Voltage-Controlled Oscillator schematic is depicted in Fig. 4.2.

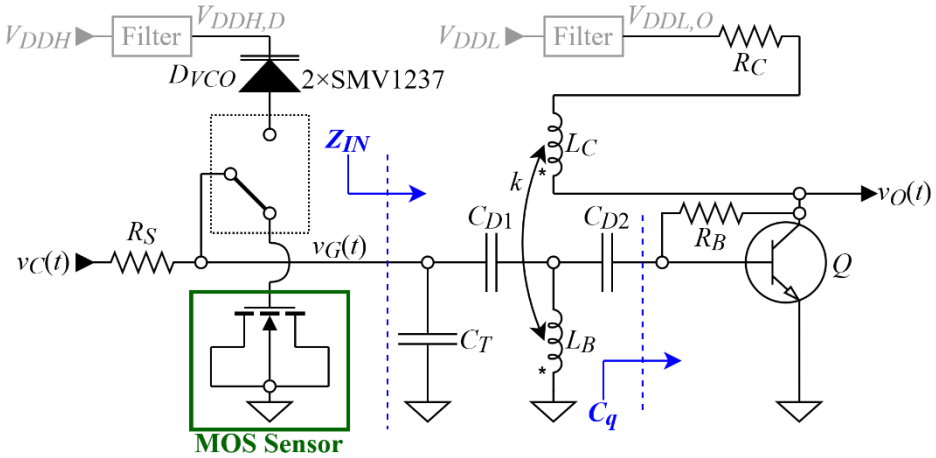


Figure 4.2 *Proposed voltage-controlled oscillator schematic*

The topology in Fig. 4.2 is an Armstrong architecture [28], which allows for the MOS sensor to have its substrate tied to ground, as well as operate under small-signal conditions (placed at the input of Q). The schematic in Fig. 4.2 comprises [6],[7],[25]:

- *Filters* – to reduce the noise on the two supply voltages;
- Q – bipolar transistor, the amplifying element of the oscillator;
- R_C, R_B – resistors for setting the quiescent point of Q;
- L_C, L_B – coupled coils, representing the oscillator's positive feedback loop;
- C_{D1}, C_{D2} – coupling capacitors (for separating the DC bias points of the MOS sensor, the base of Q and the inductance L_B);
- C_T – capacitor for adjusting the oscillation frequency (trim);
- R_S – separation resistor, necessary because the sensor bias must be set by the control voltage $v_C(t)$, while the AC signal is injected through C_{D1};
- *2×SMV1237* – varicap diodes, used in calibration as stable C-V references.

The f_{osc} frequency is determined mainly by the resonant circuit in the base of Q:

$$f_{osc}(V_G) = \frac{1}{2\pi\sqrt{L_B\left[C_g(V_G) + C_T + C_q\right]}} \tag{4.1}$$

where C_q is the transistor's input capacitance, including the Miller effect [25].

An important characteristic of the VCO is the gain, defined as:

$$K_{VCO,C}(v_C) = \frac{\mathrm{d}f_{osc}(v_C)}{\mathrm{d}v_C} \tag{4.2}$$

Since f_{osc} actually depends on the MOS sensor bias voltages, it is more relevant to express the gain as a function of V_G:

$$K_{VCO,G}(V_G) = \frac{\mathrm{d}f_{osc}(V_G)}{\mathrm{d}V_G} = -\frac{1}{4\pi\sqrt{L_B \cdot \left[C_g(V_G) + C_T + C_q\right]^3}} \cdot \frac{\mathrm{d}C_g(V_G)}{\mathrm{d}V_G} \tag{4.3}$$

Equation (4.3) shows that the variation of f_{osc} with respect to V_G is opposite that of the sensor capacitance. Consequently, given that $C_g(V_G)$ is strictly increasing with V_G (Fig. 3.2), $K_{VCO,G}$ is always negative. A higher $\mathrm{d}C_g/\mathrm{d}V_G$ variation leads to an increased $K_{VCO,G}$ gain (considering the absolute value). The gain should be as high as possible, for better CP-PLL accuracy (i.e. through sensitivity to small changes in V_G).

Given the presence of R_S at the VCO input, a Low-Pass Filter II (LPF II) is formed, as illustrated in Fig. 4.3 (assuming a purely capacitive input impedance Z_{IN}). This structure affects the response time and stability of the CP-PLL conditioning circuit.

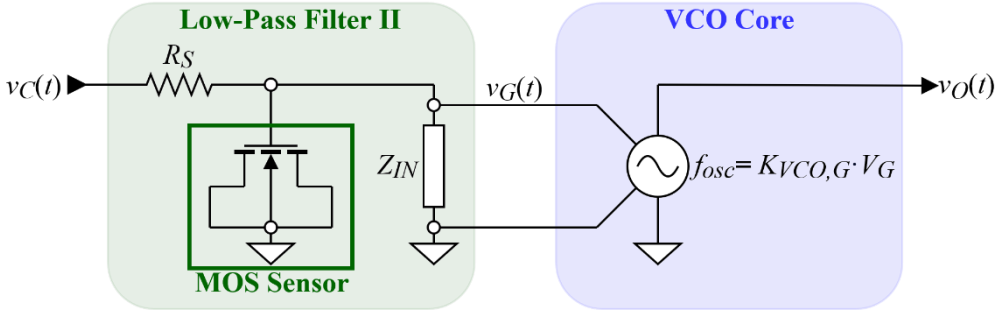


Figure 4.3 *Equivalent functional schematic of the voltage-controlled oscillator*

The Reference Oscillator (REFO) has a structure similar to the VCO (including component values), with the sole difference that, in its case, the nonlinear capacitance is given only by the two SMV1237 diodes. Therefore, a technique for evaluating and adjusting PLL accuracy can be developed (hereafter referred to as CM1 – Calibration Method 1). This procedure relies on the fact that, when the varicap diodes are connected in the VCO (Fig. 4.2), the two oscillators become identical, and their frequency-voltage curves are the same [21]. Since the PLL equalizes the frequencies, it is expected that:

$$f_{osc}(v_C)\big|_{2\times\text{SMV1237}} = f_{ref}(V_{IN}) \Rightarrow v_C = V_{IN} \tag{4.4}$$

However, if the two characteristics are identical, but the relation $v_C = V_{IN}$ is not true, this implies that the CP-PLL is operating in an erroneous manner [21]. In this case, the error sources must be identified and eliminated, to ensure correct measurement.

4.3 Phase frequency detector

The Phase Frequency Detector (PFD) has the topology seen in Fig. 4.4 [7],[21], developed starting from the well-known schematic used for this block in Charge-Pump PLL circuits [26],[27]. The components of this block are:

- *Filters* – in order to reduce the switching noise injected into the V_{DDL} supply (including between the digital sub-blocks of the detector);
- *Buffer circuits* – digital conversion of oscillator signals $v_R(t)$, $v_O(t)$ [6];
- *D-type flip-flops* – part of the basic PFD schematic [26],[27];
- *NAND gate* – part of the basic PFD schematic [26],[27];
- $R_{L,R}$, $R_{L,O}$, $R_{L,UP}$, $R_{L,DWN}$, $R_{L,N}$ – series resistors for limiting the output currents and thus the duration of d*i*/d*t* events, to reduce switching noise [29],[30],[31]. This solution was identified as the most appropriate for this purpose, given the implementation of the CP-PLL circuit using discrete components [7].

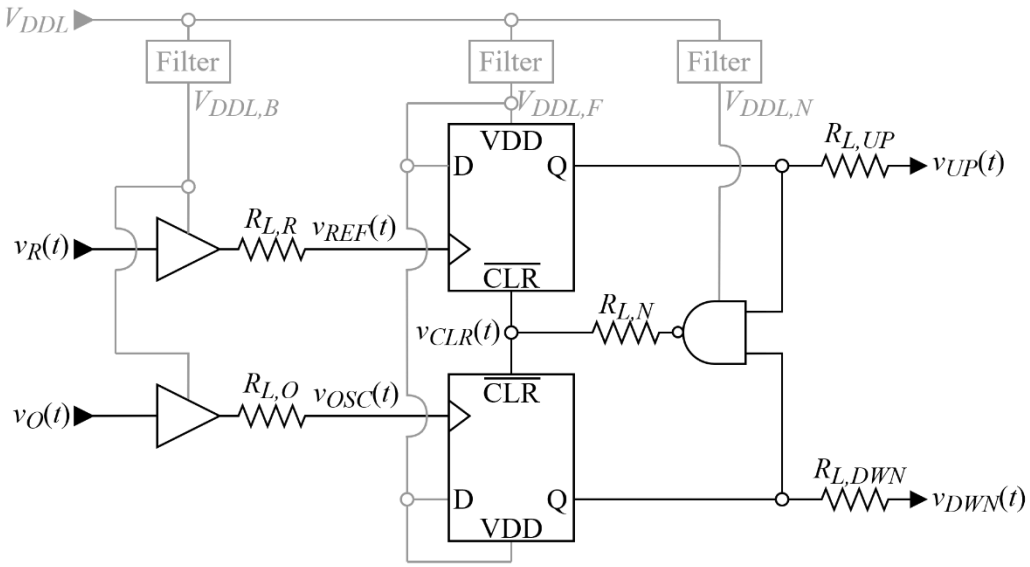


Figure 4.4 *Proposed topology of phase frequency detector*

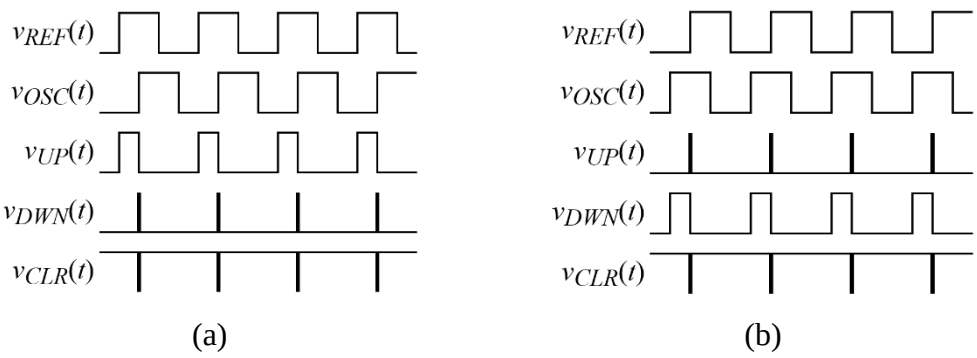


Figure 4.5 *Phase frequency detector operation in two scenarios: (a) $v_{REF}(t)$ leads $v_{OSC}(t)$ (b) $v_{OSC}(t)$ leads $v_{REF}(t)$*

Fig. 4.5 illustrates the ideal waveforms of the PFD from Fig. 4.4. The behavior mentioned in section 4.1: when $\varphi_{osc} < \varphi_{ref}$, (i.e. $v_{REF}(t)$ leads $v_{OSC}(t)$), the relation between duty cycles is $\eta_{DWN} < \eta_{UP}$ (and vice-versa, when $v_{OSC}(t)$ leads $v_{REF}(t)$). When the PLL locks ($v_C(t)$ = const), with adequate Charge Pump sizing, the oscillators' signals are in phase and short pulses are generated on $v_{UP}(t)$ and $v_{DWN}(t)$. In other words, in lock condition, the Charge Pump is driven in order to maintain a constant $v_C(t)$ [6],[7].

4.4 Charge pump and low-pass filter

The structure formed with the Charge Pump (CP) and Low-Pass Filter I (LPF I) has the topology shown in Fig. 4.6 [6],[7], which can be implemented using discrete components. An active filter structure is used, since it allows for simple generation of the constant pump currents, using resistors. This can be achieved due to the fact that the voltage at the inverting *OA* input is fixed at a constant voltage (set by V_{CM}). Moreover, LPF I has a key role in the dynamic and stability of the PLL [6],[7],[26],[27].

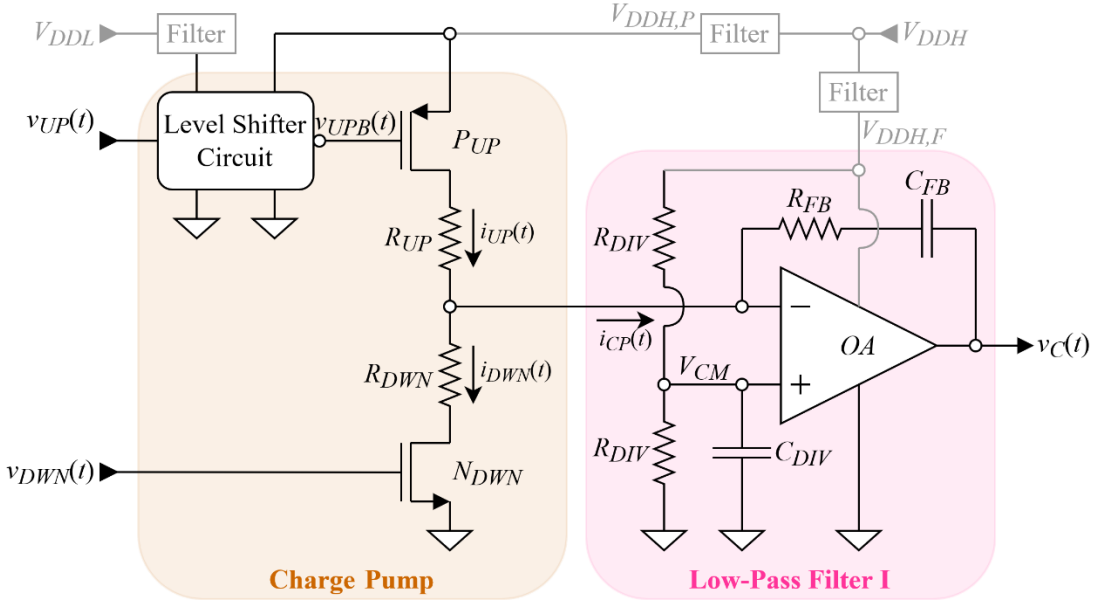


Figure 4.6 *Proposed topology of pump-filter structure*

The topology in Fig. 4.6 comprises [6],[7]:

- *Filters* – reduce the switching noise injected into the supply lines;
- *OA* – operational amplifier;
- R_{DIV}, C_{DIV} – generate the V_{CM} voltage, set to half of V_{DDH};
- C_{FB} – the capacitance being charged and discharged by the pump currents;
- R_{FB} – part of the integrating low-pass filter, with a role in PLL stability;
- P_{UP}, N_{DWN} –PMOS and NMOS switches for activating the pump currents;
- R_{UP}, R_{DWN} – set the values for the pump's discharging and charging currents;
- *Level shifter and driver circuit* – converts the $v_{UP}(t)$ signal from the [0, V_{DDL}] range to the [0, V_{DDH}] range and inverts it in order to drive the PMOS switch.

The constant currents of the charge pump from Fig. 4.6 are given by [6],[7]:

$$I_{UP} = \frac{V_{DDH}}{2R_{UP}} \qquad I_{DWN} = \frac{V_{DDH}}{2R_{DWN}} \tag{4.5}$$

Ideally, the variation of the v_C voltage after an oscillation cycle is [6],[7]:

$$\Delta v_C = \frac{I_{DWN}}{C_{FB}} \cdot t_{DWN} - \frac{I_{UP}}{C_{FB}} \cdot t_{UP} = \frac{V_{DDH}}{2C_{FB}} \left(\frac{t_{DWN}}{R_{DWN}} - \frac{t_{UP}}{R_{UP}} \right) \tag{4.6}$$

where t_{DWN}, t_{UP} are the logic "1" pulses durations for $v_{DWN}(t)$ and $v_{UP}(t)$, respectively. When the PLL locks onto the frequency f_{ref}, the control voltage remains constant:

$$\Delta v_C = 0 \Leftrightarrow \frac{t_{DWN}}{R_{DWN}} = \frac{t_{UP}}{R_{UP}} \Leftrightarrow \frac{t_{DWN}}{t_{UP}} = \frac{R_{DWN}}{R_{UP}} \tag{4.7}$$

In order to achieve lock condition with $\Delta\varphi = 0$, the PFD needs to generate equal duration logic "1" pulses [6],[7]. Therefore, resistances R_{UP} and R_{DWN} must be equal. On the other hand, an error term (t_{CP}) is also present, representing the speed mismatch of the UP and DWN signal paths. In these conditions, equation (4.7) becomes:

$$\frac{t_{DWN}}{t_{UP} + t_{CP}} = \frac{R_{DWN}}{R_{UP}} \tag{4.8}$$

A significant contribution to t_{CP} is owed to the level shifter circuit used for driving the PMOS switch (Fig. 4.6). Thus, an investigation into potential topologies for this block is carried out, focusing on two output stage structures:

- push-pull [32],[33],[34] – both the pull-up and pull-down functionalities for the output are done using actively driven devices;
- open-drain [29],[30],[31] – only one of the pull-up or pull-down structures is driven, the other one is always enabled (e.g., resistor or current source).

Improved schematics are proposed for each of these two approaches, presented in Fig. 4.7 (push-pull) [32] and in Fig. 4.8 (open-drain) [29],[30],[31]. In the case of the push-pull version (Fig. 4.7), mixed voltage transistors are used (low voltage gate, high voltage drain) together with innovative "pull-up" structures ($NNLH_x$, PL_x) to improve the speed of both switching events ("0" → "1" and "1" → "0") [32]. For the open-drain topology from Fig. 4.8, a feedback configuration is used to reduce the propagation delay at the "1" → "0" output transition, while maintaining a controlled output switching rate (due to noise considerations) [29],[30],[31]. Nevertheless, given the implementation using discrete components of the CP-PLL circuit, it is preferrable to use a simple level shifter (formed only with N_{UPB}, R_{UPB} and $v_{DRV}(t) = v_{UP}(t)$ – Fig. 4.8). In this case, other solutions are identified for compensating the error term t_{CP} (equation (4.8)).

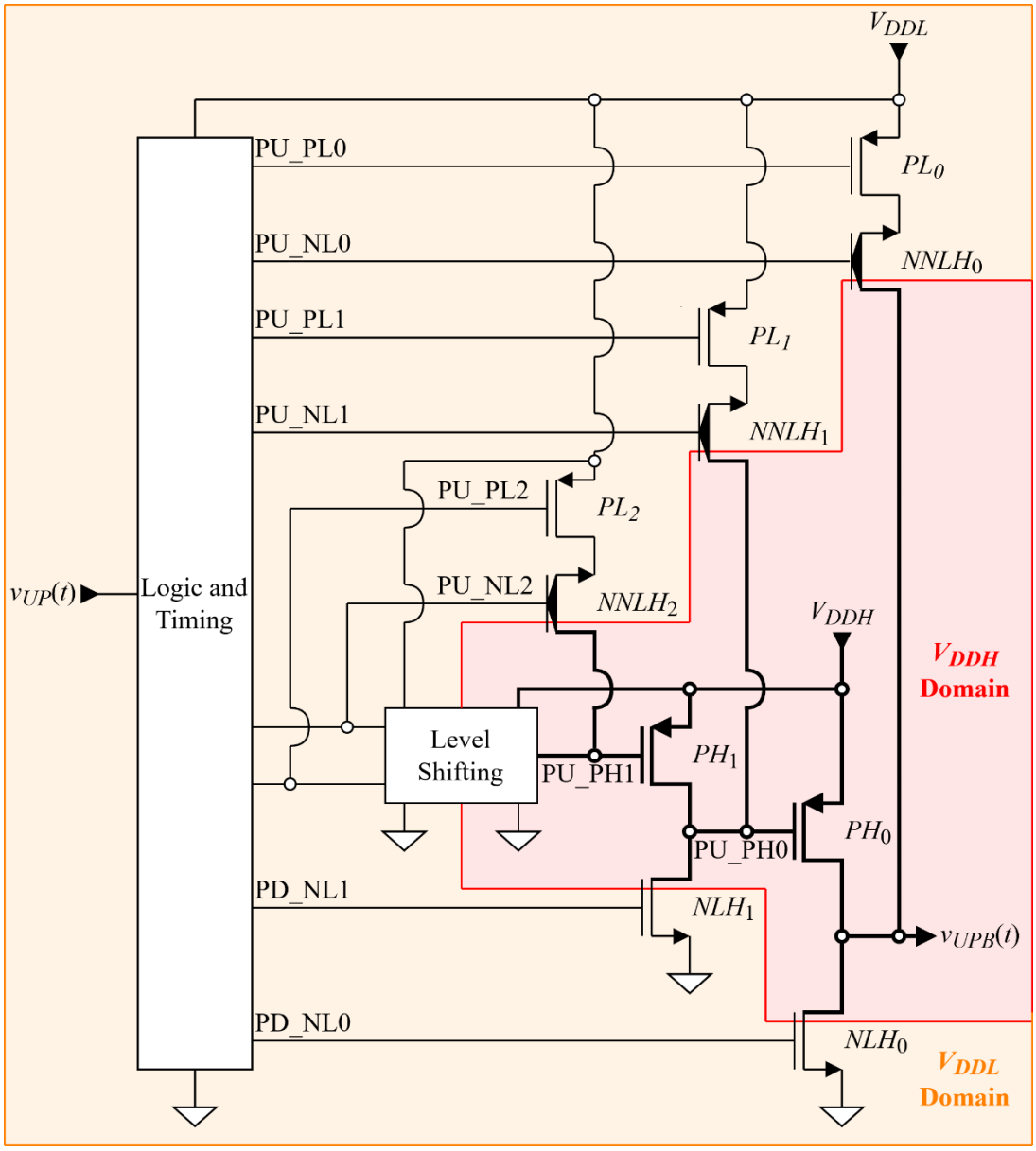


Figure 4.7 *Improved push-pull level-shifter and driver circuit [32]*

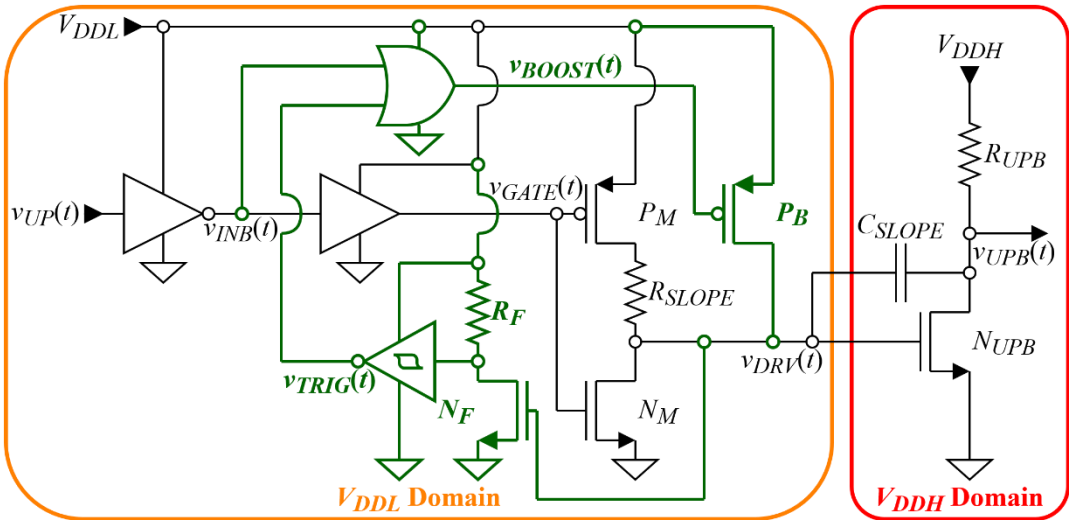


Figure 4.8 *Improved open-drain level-shifter and driver circuit [29],[30],[31]*

4.5 Supply circuit

As suggested by the schematics in Fig. 4.2, Fig. 4.4 and Fig. 4.6, it is necessary to separate and filter the supplies of the individual CP-PLL sub-blocks to ensure its correct operation. As such, the supply circuit from Fig. 4.9 is proposed, wherein the voltages V_{DDL} and V_{DDH} are obtained from V_{DDM} using adjustable linear regulators [35], with large decoupling capacitors on the outputs. The internal voltages are distributed in a star connection, with additional filtering capacitors added for each sub-block [7].

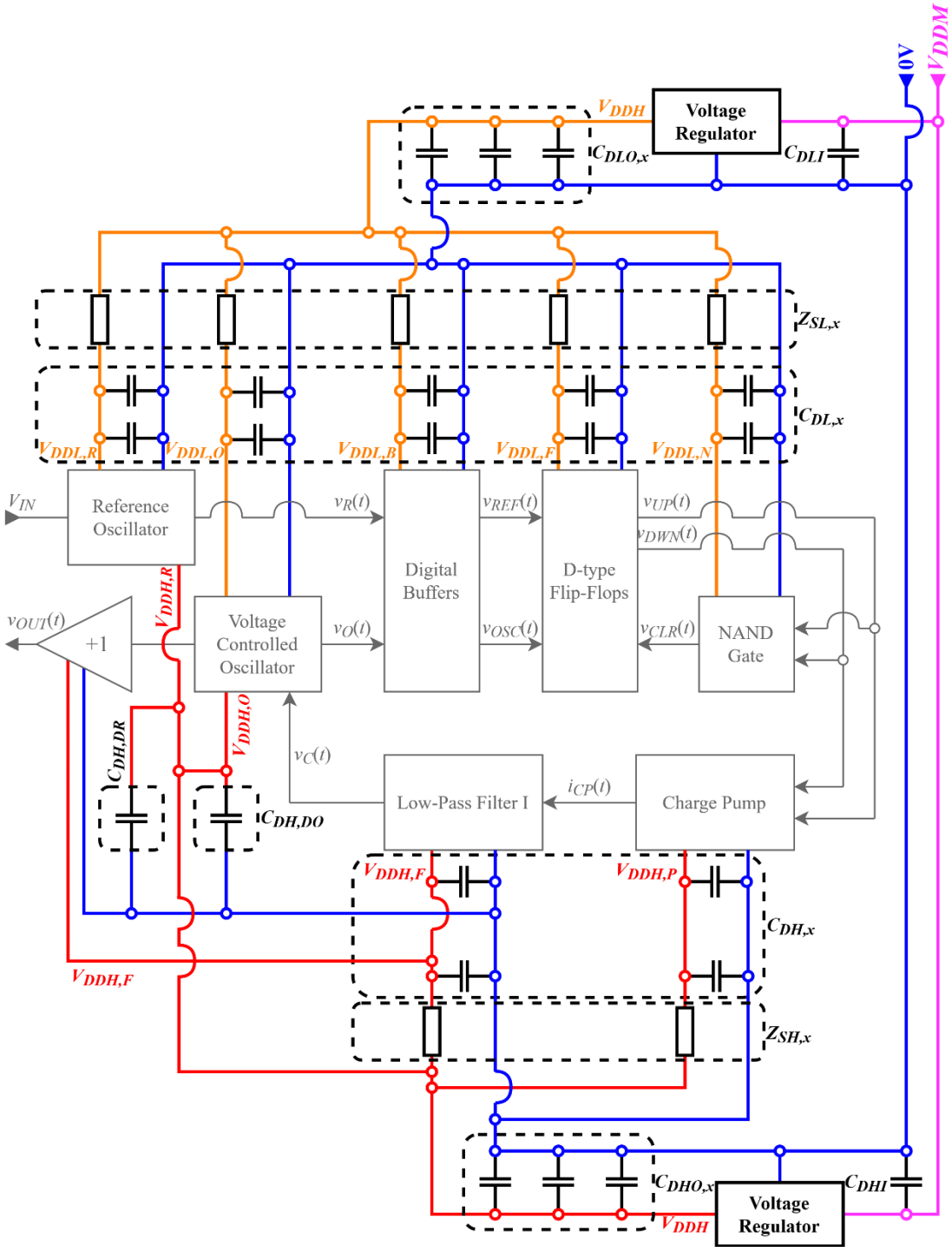


Figure 4.9 *CP-PLL supply circuit structure*

Chapter 5

Modeling, Design and Simulation of PLL Circuit

5.1 Laplace model of PLL circuit

For the frequency analysis of the CP-PLL (switch-mode circuit), it is modeled as continuous time linear time invariant system (Fig. 5.1). In order to create this model, the following simplifying hypotheses are considered [27],[36]:

- The PLL circuit is locked onto the reference signal, $v_R(t)$;
- The phases of the reference signal (φ_{ref}) and that of the VCO signal (φ_{osc}) have slow variations (frequencies much lower than the VCO), with low amplitude. These correspond to small-signal, low frequency conditions [15],[28];
- The effect of these slow variations on the CP-PLL signals is integrated in time. Therefore, all signals will be modeled as being continuous.

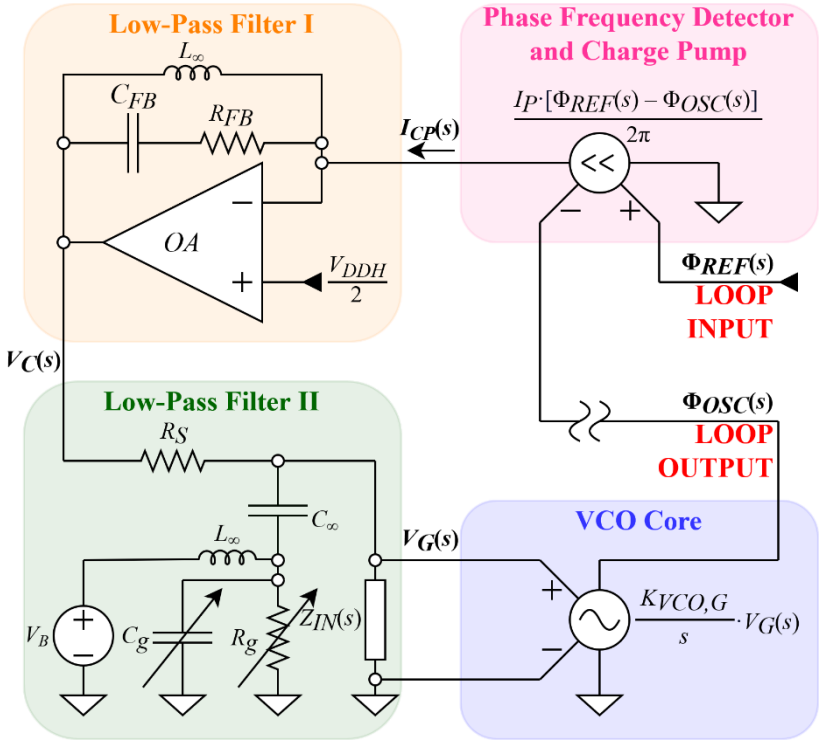


Figure 5.1 *CP-PLL equivalent Laplace circuit*

On the Laplace circuit from Fig. 5.1, the Open-Loop (OL) transmission can be calculated, with the loop being broken at the VCO output [15],[27],[36],[37]:

$$T(s) = \left.\frac{\Phi_{OSC}(s)}{\Phi_{REF}(s)}\right|_{\text{OL}} \tag{5.1}$$

Analyzing the circuit in Fig. 5.1, the following expression is obtained:

$$T(s) = -\frac{I_P}{2\pi}\cdot\frac{R_g}{R_g+R_S}\cdot\frac{1+sR_{FB}C_{FB}}{sC_{FB}\cdot\left[1+s\left(R_g||R_S\right)\left(C_g+C_T+C_{D1}\right)\right]}\cdot\frac{K_{VCO,G}}{s} \tag{5.2}$$

where $I_P/2\pi$ is the gain of the detector-pump structure (Fig. 5.1), according to Gardner's approximation [27]. Moreover, the expression was simplified assuming an infinite gain for *OA* (FTJ I) and a purely capacitive VCO input impedance, Z_{IN} ($C_T + C_{D1}$).

The minus sign in the expression of $T(s)$ is generated by the connections at the PFD-CP input – $\Phi_{OSC}(s)$ is tied to the inverting input (increasing it leads to a negative CP current, as can be deduced from Fig. 4.4 and Fig. 4.6). This connection is necessary to compensate for the negative value of the VCO gain $K_{VCO,G}$ (equation (4.3)).

In equation (5.2), a double pole in the origin (VCO and LPF I), a pole given by LPF II and a zero set by LPF I can be observed, leading to an increased instability risk. Therefore, in order to obtain a more accurate image of the PLL dynamic behavior, the Closed-Loop (CL) response is also evaluated [15],[27],[36],[37]:

$$H(s) = \left.\frac{\Phi_{OSC}(s)}{\Phi_{REF}(s)}\right|_{\text{CL}} = \frac{T(s)}{1+T(s)} \tag{5.3}$$

5.2 Voltage controlled oscillator design

The selection of the Voltage-Controlled Oscillator (VCO) components is critical for meeting most of the design requirements. The 1 MHz frequency and small signal operation is achieved using the values from Table 5.1 [6],[7],[25].

V_{DDL} = 2.7 V and resistances R_B, R_C are selected for a voltage gain large enough to ensure small-signal level on the MOS sensor, while R_C (2 kΩ nominal) is adjustable, to allow for tuning f_{osc}. V_{DDH} = 7 V is chosen considering sensor biasing in the depletion region (V_G = 4...6 V – Fig. 3.2). *Q* is a high-frequency device (BFP196 [38]), for low parasitic capacitances and reduced impact on f_{osc} (equation (4.1)). In the case of the coupled coils, a commercially available transformer is selected (PWB-2-CL [38]), but only half of its inductances are used (by tying the center tap). C_{D1} and C_{D2} (coupling) are larger than the other VCO capacitances. Finally, a 4 kΩ nominal value is used for the separation resistor R_S with the possibility to adjust, depending on R_g [6],[7],[25].

Table 5.1 *Types and values for the voltage-controlled oscillator components*

Element	V_{DDL}	V_{DDH}	Q	R_C	R_B	L_C	L_B	k	C_{D1}	C_{D2}	C_T	R_S
Type	2.7	7	BFP196	2...3	6.98	37.5	75	0.5	2	2	120	2...7
Unit	V	V	–	kΩ	kΩ	µH	µH	–	nF	nF	pF	kΩ

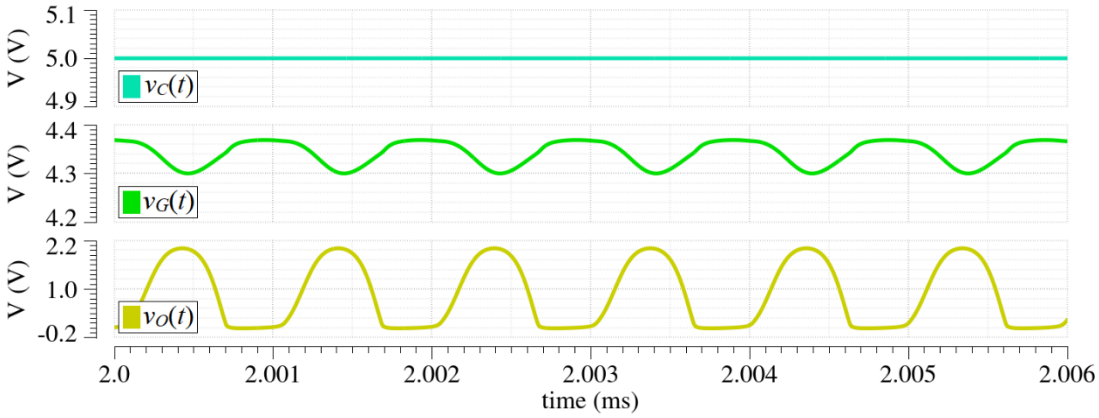


Figure 5.2 *Oscillator operation at constant control voltage*

The VCO from Fig. 4.4, with the components in Table 5.1, is simulated using the time-domain model of the sensor and v_C = const = 5 V. The resulting waveforms (Fig. 5.2) depict a small sensor signal ($v_G(t)$ – ~70 mV_{pp}) and $f_{osc} \cong 1$ MHz.

The simulation is redone for multiple values of v_C, resulting in the graphs from Fig. 5.3. These are plotted with respect to v_C, as well as the bias V_G of the nonlinear capacitance. Moreover, the VCO behavior was investigated with both the MOS sensor and the varicap diodes. Fig 5.3 evinces the effect of the R_g sensor resistance – the slope of the frequency-voltage characteristic decreases when it is plotted versus v_C (blue curves in Fig. 5.3). In other words, the resistive divider at the VCO input leads to a gain loss ($\max\{K_{VCO,C}\} < \max\{K_{VCO,G}\}$ – equations (4.2) and (4.3)).

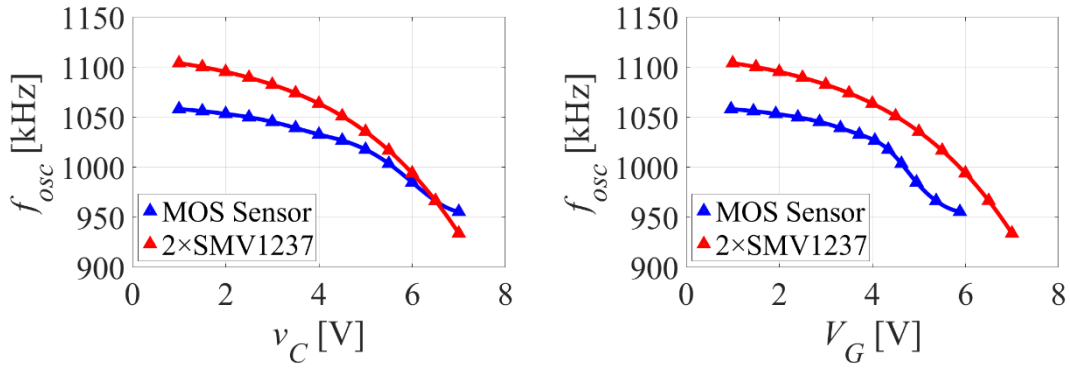


Figure 5.3 *Oscillator frequency dependence with respect to: (a) v_C (b) V_G*

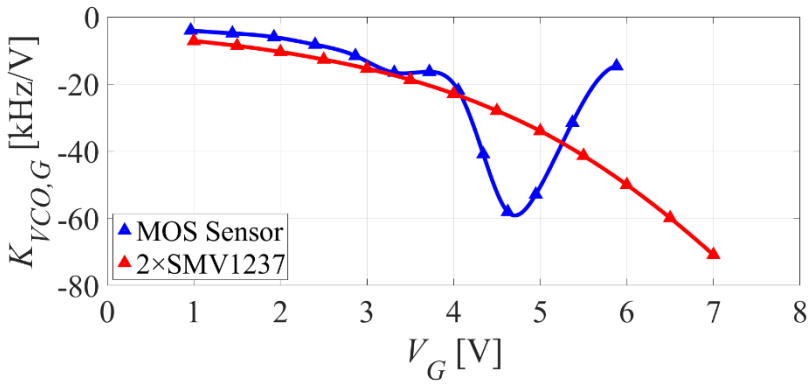


Figure 5.4 *Voltage-controlled oscillator gain versus sensor bias*

Based on the values from Fig. 5.3.b and the definition of the gain (eq. (4.3)), the $K_{VCO,G}$ plots from Fig. 5.4 are obtained. Comparing the blue graphs from Fig. 5.3.b and Fig. 5.4, it can be seen that, with C_T = 120 pF (Table 5.1), the 1 MHz frequency is achieved in the region where $K_{VCO,G}$ is close to its maximum ($V_G \cong 4.6$V).

It is important to note that, with the values from Table 5.1, the cut-off frequency of the LPF II formed at the VCO input (Fig. 4.3) is approximately 20 kHz. This leads to an increased CP-PLL response time. However, its value is still negligible compared to the sensor response time, which is in the order of tens of seconds [7],[10].

5.3 Detector-pump-filter design

The operation of the PFD and CP-LPF I is strongly interdependent – the manner in which $v_{UP}(t)$ and $v_{DWN}(t)$ are generated influences the variation of the $v_C(t)$ voltage. Consequently, these blocks are designed and simulated at the same time. In the PFD (Fig. 4.4), integrated circuits from the LVC family are used [40], as shown in Table 5.2. These have relatively low propagation and switching times and thus require larger d*i*/d*t* limiting resistances (1 kΩ) [7]. For the UP and DWN resistors, lower resistance values are selected, since these signals are connected directly to the gates of the CP switches. These devices have larger input capacitances than the LVC integrated circuits, thereby justifying the selection of a four times smaller value (255 Ω).

Table 5.2 *Types and values for the phase frequency detector components*

Element	Digital Buffers	D-type Flip-Flops	NAND Gate	$R_{L,R}$	$R_{L,O}$	$R_{L,N}$	$R_{L,UP}$	$R_{L,DWN}$
Type	SN74LVC125A	SN74LVC74A	SN74LVC1G00	1	1	1	255	255
Unit	–	–	–	kΩ	kΩ	kΩ	Ω	Ω

Table 5.3 *Types and values for the pump-filter structure*

Element	NMOS	PMOS	*OA*	R_{UPB}	R_{UP}	R_{DWN}	R_{FB}	C_{FB}	R_{DIV}	C_{DIV}
Type	FDC6301N	FDC6302P	OPA2830	50	2..4	2..4	0.2...1.2	2	100	1
Unit	–	–	–	Ω	kΩ	kΩ	kΩ	nF	kΩ	nF

The types and values for the CP-LPF I elements (Fig. 4.6), shown in Table 5.3, are chosen considering the 1 MHz operating frequency [6],[7]. Thus, for the active components, small parasitic capacitances and low response times are the key targets. Moreover, the supply voltages V_{DDL} = 2.7 V and V_{DDH} = 7 V (Table 5.1) are considered. Therefore, two digital transistors types are chosen: FDC6301N [41] for N_{DWN} (Fig. 4.6) and N_{UPB} (Fig. 4.8), FDC6302P [42] for P_{UP} (Fig. 4.6) [6],[7]. For *OA*, the high-speed operational amplifier OPA2830 is selected [43]. The same amplifier is used for the Voltage Follower which generates $v_{OUT}(t)$ (Fig. 4.1).

Resistances R_{UP} and R_{DWN} have the nominal value of 2 kΩ [6], in order to obtain equal CP currents (1.75 mA – expressions (4.5)). However, as shown by eq. (4.8), these resistors can be tuned to compensate for mismatches of the UP and DWN paths [21]. Thus, they will be adjustable up to 4 kΩ. R_{FB}, C_{FB} are selected for a stable CP-PLL behavior. R_{FB}, with a 200 Ω nominal value, can be adjusted in order to change the frequency of the zero given by LPF I (eq. (5.2)) in case of circuit instability.

R_{DIV}, C_{DIV} are selected for low consumption and for a reduction by >40 dB of the switching noise injected from V_{DDH} into V_{CM} (Fig. 4.6) – the cut-off frequency is ~3 kHz (~300 times smaller than the 1 MHz working frequency). Finally, R_{UPB} is set for a compromise between speed and consumption [6],[7]. With R_{UPB} = 50 Ω, the current draw is relatively high when N_{UPB} is turned on, $V_{DDH}/R_{UPB} \cong 140$ mA (Fig. 4.8). However, when the CP-PLL locks, the logic "1" pulses on $v_{UP}(t)$ are short. Thus, the current consumption of the level shifter at steady state will be much lower [6],[7].

The detector-pump-filter structure is simulated with $R_{UP} = R_{DWN} = 2$ kΩ, while applying inputs $v_R(t)$ and $v_O(t)$ with different phase shifts $\Delta\varphi = \varphi_{ref} - \varphi_{osc}$ (–π, 0, π). The $v_C(t)$ control voltage (Fig 5.5) does not remain constant at zero phase shift (ideal case) but decreases slowly. This variation is generated by the mismatch in the delays and switching times of the UP and DWN signal paths, as was suggested by eq. (4.8). This behavior is confirmed by the detailed waveforms from Fig. 5.6 ($\Delta\varphi = 0$).

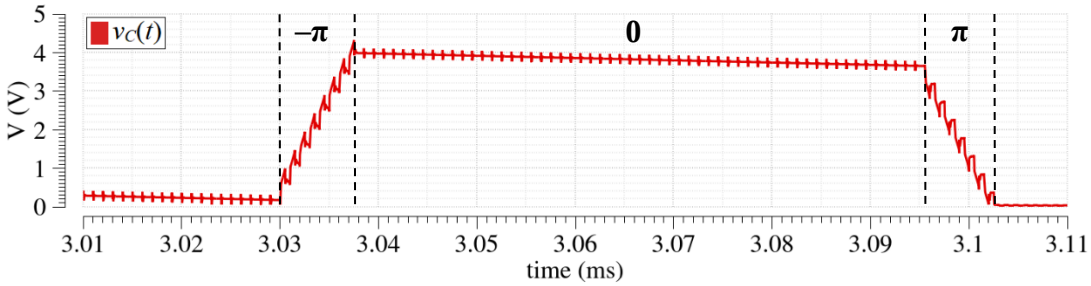


Figure 5.5 *Detector-pump filter operation at different phase shifts*

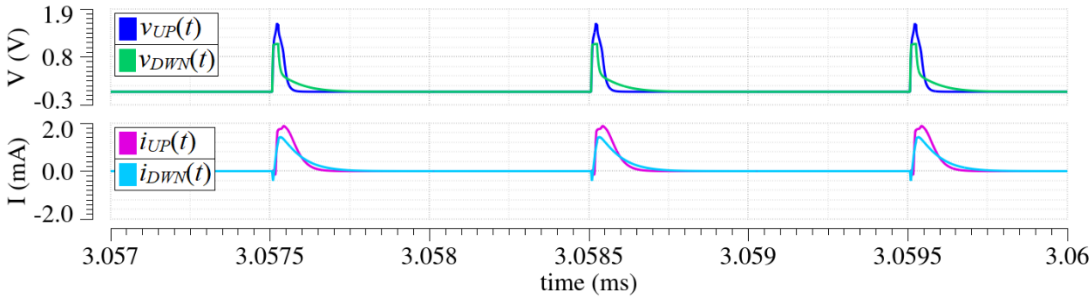


Figure 5.6 *Detector-pump-filter waveforms at zero phase shift*

Fig. 5.6 shows that the peak current value for $i_{UP}(t)$ is larger than for $i_{DWN}(t)$. Therefore, it is necessary to increase resistance R_{UP} in order to calibrate the circuit. To evaluate the effectiveness of the solution, the average pump current as a function of phase shift is used, calculated based on the average dv_C/dt variation:

$$\overline{I_{CP}(\Delta\varphi)} = -C_{FB} \cdot \overline{\frac{dv_C}{dt}(\Delta\varphi)} \tag{5.4}$$

With R_{UP} = 3.35 kΩ, the average pump current is zero for $\Delta\varphi = 0$ (Table 5.4).

Table 5.4 *Average charge pump current versus phase shift*

Quantity	$R_{UP} = R_{DWN} = 2$ kΩ			$R_{UP} = 3.35$ kΩ, $R_{DWN} = 2$ kΩ			***Unit***
Δφ	–π	0	π	–π	0	π	rad
$\overline{I_{CP}(\Delta\varphi)}$	-0.953	0.012	0.939	-0.970	0.000	0.555	mA

5.4 Supply circuit design

The simplified schematic of the supply circuit, with detailed linear regulators, is shown in Fig. 5.7. In this drawing, the total capacitances on the V_{DDL} and V_{DDH} lines were represented in a simplified manner (C_{DLT} and C_{DHT}, respectively). The values set for the circuit's components (Fig. 4.9, Fig. 5.7), are shown in Tables 5.5 and 5.6.

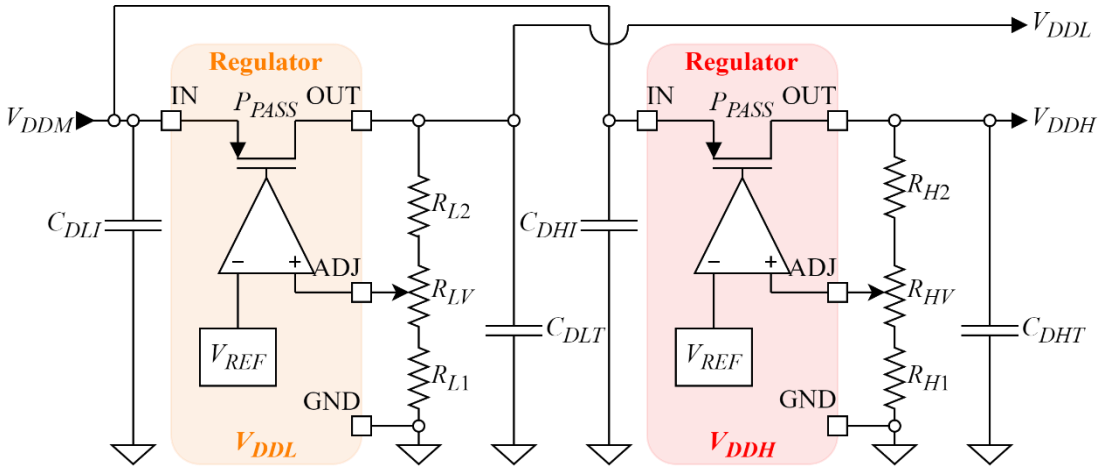


Figure 5.7 *Simplified supply circuit schematic*

Table 5.5 *Supply circuit regulators and resistances*

Element	*LDO* V_{DDL}	*LDO* V_{DDH}	V_{DDM}	R_{L1}	R_{LV}	R_{L2}	R_{H1}	R_{HV}	R_{H2}
Type	TPS7A4501	TPS7A4501	10	3.0	2.0	3.0	0.5	1.0	2.0
Unit	–	–	V	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ

Table 5.6 *Supply circuit reactive components*

Element	C_{DLI}/C_{DHI}	$C_{DLO,x}/C_{DHO,x}$	$C_{DL,x}/C_{DH,x}$	$C_{DH,DO}/C_{DH,DR}$	$Z_{SL,x}/Z_{SH,x}$
Value	10 µF	220 µF‖10 µF‖100 nF	10 µF‖100 nF	10 µF	0 Ω

TPS7A4501 was chosen, as its output voltage is adjustable between 1.21 V and 20 V – V_{DDL} and V_{DDH} can be obtained with the same type of regulator [35]. Resistances were selected in order to generate the V_{DDL} = 2.7 V and V_{DDH} = 7 V values required by the PLL blocks. Simulations show a power supply rejection ratio $PSRR$ > 40 dB [44] for the designed circuit – for V_{DDL}, V_{DDH} and frequencies from 1 Hz to 100 MHz.

5.5 Complete PLL circuit simulation

Firstly, the CP-PLL is simulated in the frequency-domain, using the Laplace model from Fig 5.1 and the respective MOS sensor model. The phase margins of the open-loop transmission (PM_T) and the closed-loop response (PM_H) in Table 5.7 are obtained. The usual stability criterion implies $PM_T > 0$, so that the signal does not return with 180° shift at the inverting loop input [15]. However, $PM_T < 0$ is observed. On the other hand, the circuit operates with a closed-loop and $PM_H > 0$ is a more relevant metric (indicating stability). Moreover, systems apparently unstable in open-loop can have stable closed-loop responses, especially if they contain integrators [45],[46],[47].

Table 5.7 *Phase margins vs. sensor bias*

V_B [V]	1.93	2.87	4.05	4.34	4.62	4.95	5.37	5.88
PM_T [°]	-27.6	-34.4	-39.4	-44.7	-47.1	-45.7	-40.7	-33.2
PM_H [°]	66.2	78.3	86.7	95.2	99.1	96.8	88.8	76.2

Afterward, the CP-PLL circuit is simulated in the time-domain, including all its designed blocks, with the exception of the Supply Circuit (nearly ideal behavior). For the REFO, the schematic from Fig. 4.2 is considered, without the MOS sensor but with the same component values as the VCO (Table 5.1). First, the varicap diodes are used in the VCO (Fig. 4.2), as per Calibration Method 1 (CM1), and V_{IN} voltages of 3...7 V are applied. Correct operation would lead to $v_C = V_{IN}$, as shown in eq. (4.4) [21]. Thus, the DC component of $v_G(t)$ (V_G) should be equal to that of $v_{GR}(t)$ from the REFO (V_{GR}). Even more, since the diodes have a large resistance, $V_{GR} = V_{IN}$ and $V_G = v_C$. However, the waveforms from Fig. 5.8 show an erroneous behavior – v_C is not equal to V_{IN}. Moreover, while f_{osc} follows f_{ref}, its waveform evinces significant jitter [21].

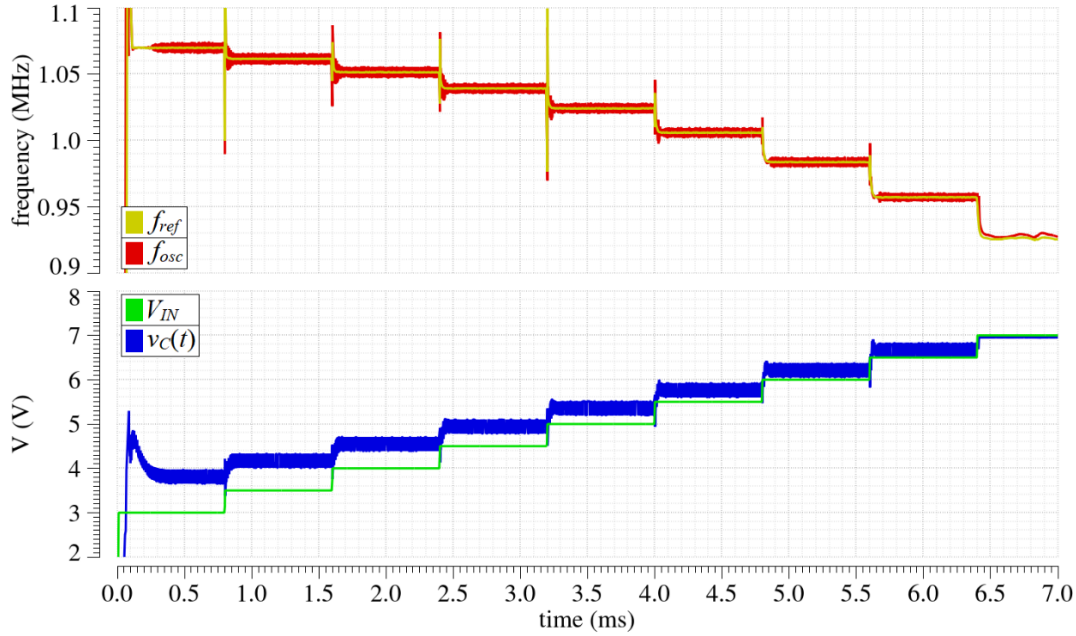


Figure 5.8 *CP-PLL operation with varicap diodes, prior to calibration*

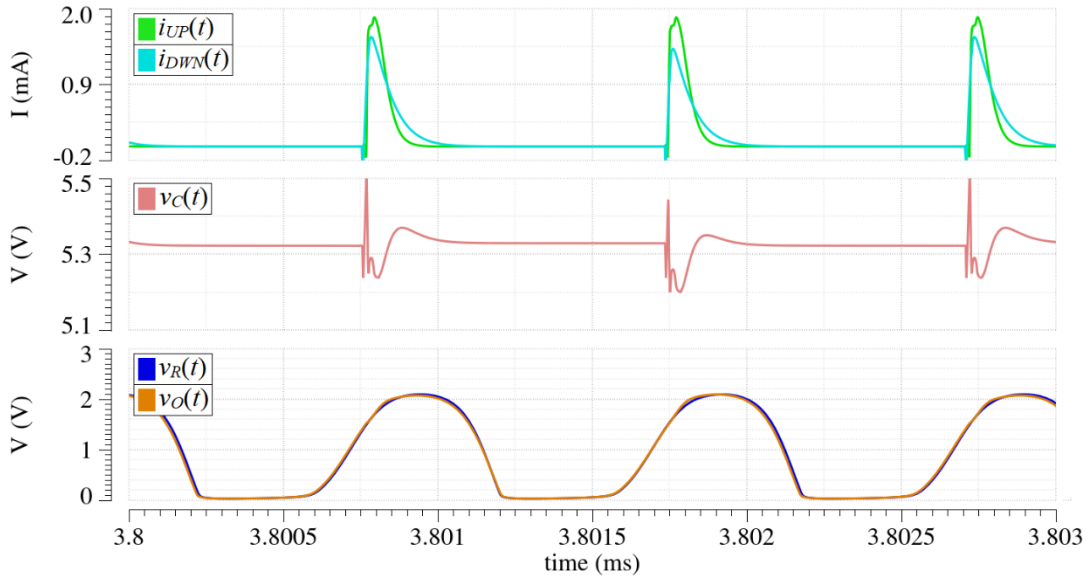


Figure 5.9 *CP-PLL operation with varicap diodes, prior to calibration (detail)*

The detailed waveforms extracted for V_{IN} = 5 V (Fig. 5.9) show that, similarly to Fig. 5.6, $i_{UP}(t)$ and $i_{DWN}(t)$ currents do not overlap. Consequently, a significant noise appears on $v_C(t)$, as a result of the voltage drop across R_{FB} [21]. This noise is injected in the VCO, leading to a shift in its frequency-voltage characteristic and the generation of $v_C - V_{IN}$ errors. An oscillating behavior of the frequency shift causes the observed jitter. [21]. Next, the VCO gain is extracted for the voltage values in Fig. 5.8, and by plotting the errors, a linear dependency on $1/|K_{VCO,G}|$ is observed (Fig. 5.10) [21].

For error correction, R_{UP} is increased to 3.1 kΩ (similarly to Table 5.4). In this manner, the error is reduced from hundreds of mV down to tens of mV, as shown in Table 5.8. Moreover, when simulating with MOS sensors in both oscillators (only possible in simulations), errors in the order of mV are also obtained [21].

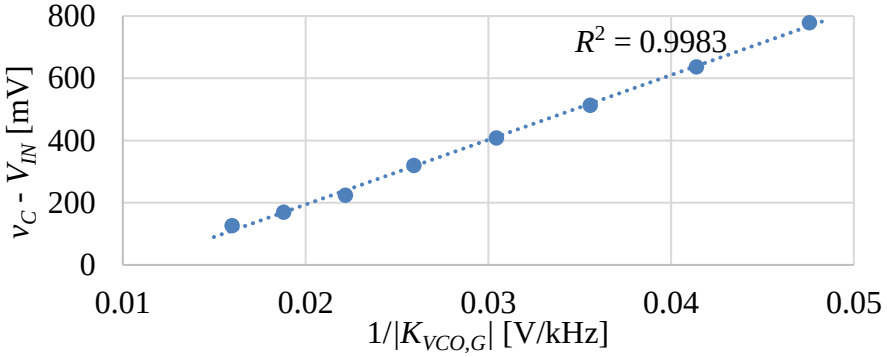


Figure 5.10 *Correlation of CP-PLL error with VCO gain*

Table 5.8 *PLL errors, before and after calibration with CM1*

***V_{IN}* [V]**	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5
***Uncalibrated* [mV]**	778	636	513	408	319	224	169	126
***Calibrated* [mV]**	10	7	4	2	1	-22	-23	-18
***MOS Sensor* [mV]**	0	-1	-3	-6	-3	-2	-2	-10

Chapter 6

Implementation and Experimental Validation of PLL Circuit

6.1 CP-PLL I – Implementation

The first implemented version of the conditioning circuit (CP-PLL I) is based on a simpler signal processing architecture. Compared to the topology whose design was presented in the previous chapters, CP-PLL I does not include:

- The d*i*/d*t* limiting solution for the digital circuits;
- Star connection on the supplies – moreover, V_{DDL} and V_{DDH} are external;
- Varicap diodes – it was assumed that the REFO could use a reference sensor;
- 4 kΩ separation resistor – the sensor parallel resistance R_g (Fig 3.3) was initially assumed very large, leading to the selection of R_S = 10 kΩ.

CP-PLL I was implemented on a two-layer Printed Circuit Board (PCB) using mostly SMD components [48] (type 0805, for the passives). The ground plane technique was used, in order to minimize the stray inductance of this connection [49]. Nevertheless, CP-PLL I did not function, because of a too high value for the separation resistor (compared to R_g) and the switching noise injected into the supplies.

6.2 CP-PLL II – Implementation and validation

The prototype circuit CP-PLL II is developed starting from the first version, with the following improvements, based primarily on experimental observations [7]:

- For simplicity, REFO is not included, $v_R(t)$ is given by a function generator;
- d*i*/d*t* limiting for the currents of the digital circuits (as in Fig. 4.4);
- The supplies of the blocks are separated and filtered. However, V_{DDL} and V_{DDH} are still generated by external supplies (not by regulators);
- R_S was reduced to 2 kΩ, for which correct PLL operation was observed;
- Slightly different values for some of the components.

The circuit obtained with these improvements is implemented on a breadboard using THD components [48], while for the SMD ones adapter PCBs are used.

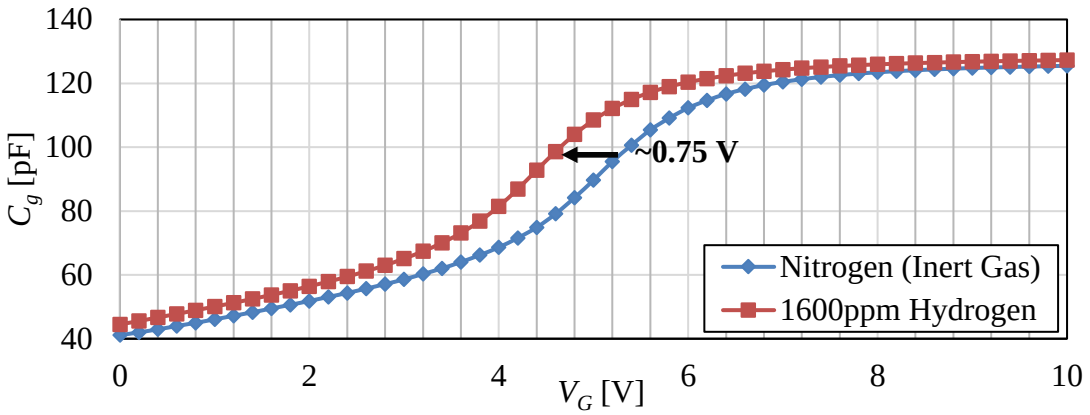


Figure 6.1 *$C_g(V_G)$ characteristics of S1 sensor, without and with hydrogen [7]*

For the measurements with CP-PLL II, three MOS sensors (named S1, S2, S3) are used, having the same structure as the device described in Chapter. The $C_g(V_G)$ plots of S1 are illustrated in Fig. 6.1, obtained with the Keithley 4200-SCS under the same conditions as the curves from Fig. 3.2 (100 mV_{pp}, 1 MHz, 100 °C) [7]. If an initial bias voltage V_G(0 ppm) ≅ 5.3 V is chosen, considering the associated constant capacitance (C_g ≅ 96.8 pF), V_G(1600 ppm) ≅ 4.55 V will be obtained as concentration rises. Thus, the voltage shift $\Delta V_{0\text{-}1600}$, indicating the presence of H_2, is roughly 0.75 V.

Next, the CP-PLL II accuracy in H_2 detection is verified. Thus, the $\Delta V_{0\text{-}1600}$ shift is measured for the three sensors (S1, S2, S3), both with the PLL and with the Keithley. The V_G(0 ppm) value is different for each sensor, selected for optimal sensitivity. Concentration is varied from 0 to 1600 ppm, increasing by 400 ppm every 6 minutes, in order to allow for system settling. During this process, the MOS sensor is connected to the PLL. Before and after this procedure, C-V plots are extracted with the Keithley (at 0 ppm and at 1600 ppm). The $\Delta V_{0\text{-}1600}$ values from Fig. 6.2 are thus obtained [7].

In Fig. 6.2, when measuring with CP-PLL II and sensor S1, the voltage drops by **0.77 V** across the entire concentration range. In this case, V_G(0 ppm) ≅ 5.3 V was considered, same as Fig. 6.1 (with a comparable shift of **0.75 V**) [7]. Furthermore, in the other two cases, the differences between the measurement methods are ≤110 mV. Therefore, the PLL topology is validated as a H_2 detection solution, with performances comparable to the characterization system, but obtained in a portable form.

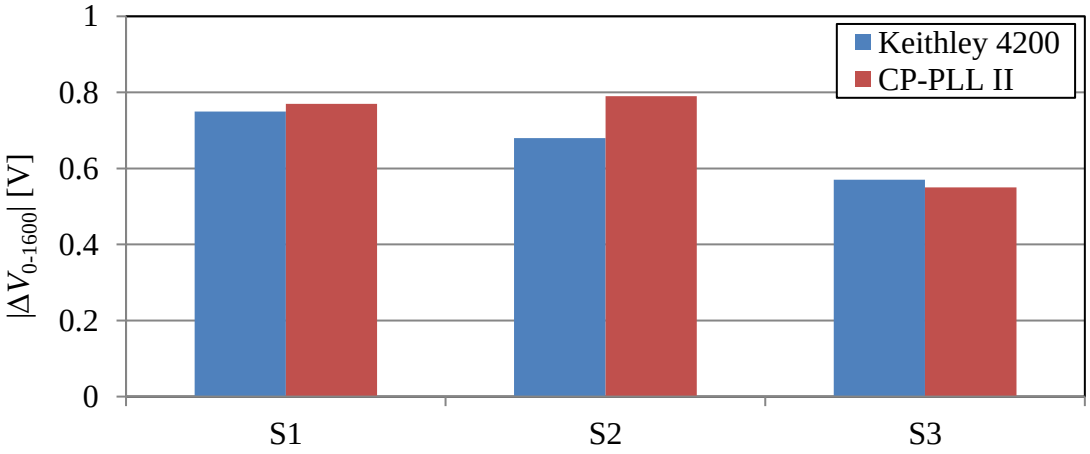


Figure 6.2 *Bias voltage shift, measured with Keithley 4200-SCS and CP-PLL II [7]*

6.3 CP-PLL III – Implementation and validation

The good results obtained with the CP-PLL II prototype proved the viability of the PLL topology as a signal conditioning circuit for the SiC-MOS sensor. Thus, the design process was restarted (as presented in Chapters 4 and 5), accounting for the experimental observations concerning the necessity to limit switching noise and the low sensor resistance. The CP-PLL III schematic from Fig. 6.3 is obtained by implementing the solutions for these issues, as well as other changes (such as the supply circuit).

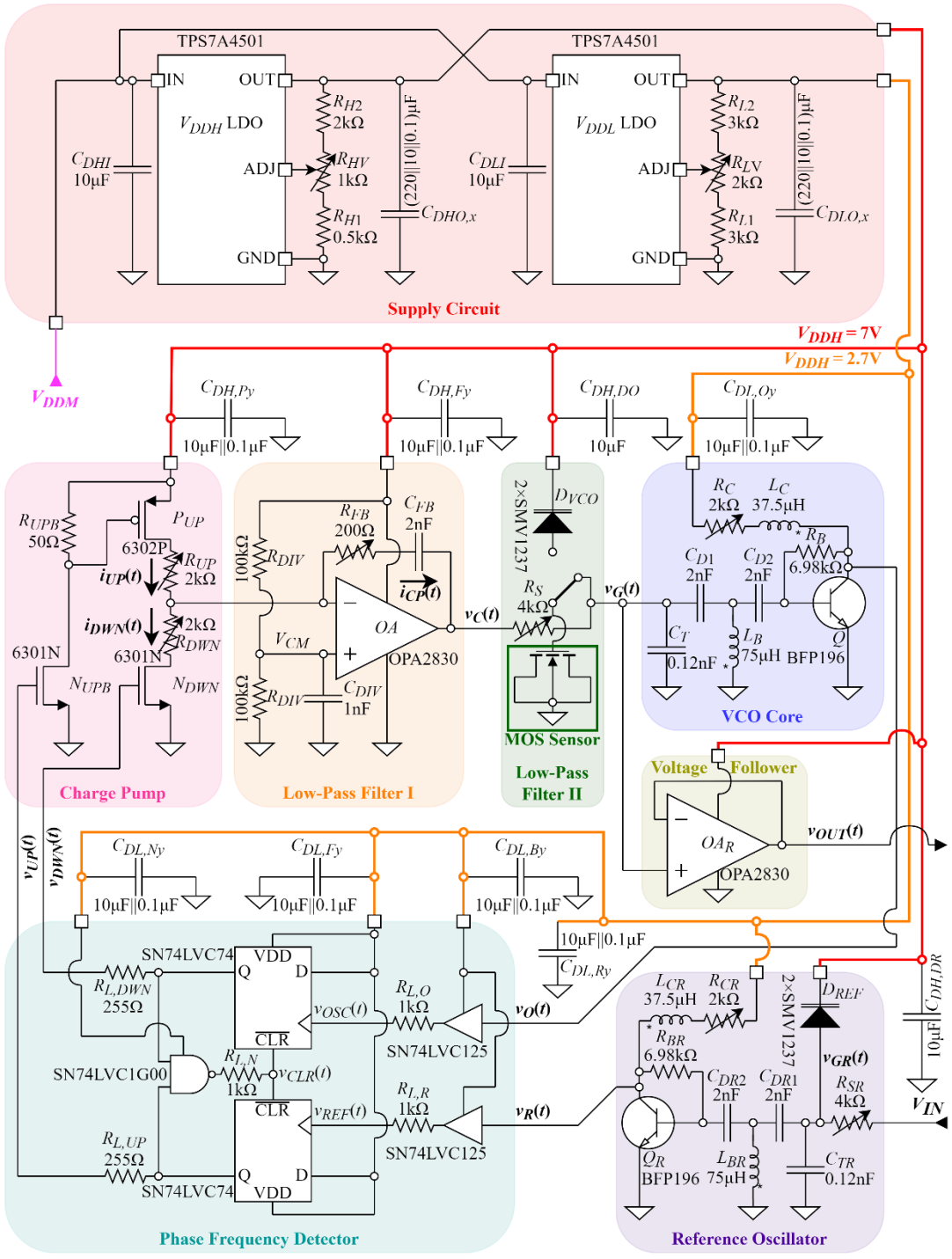


Figure 6.3 *The PCB implemented schematic of the CP-PLL III variant*

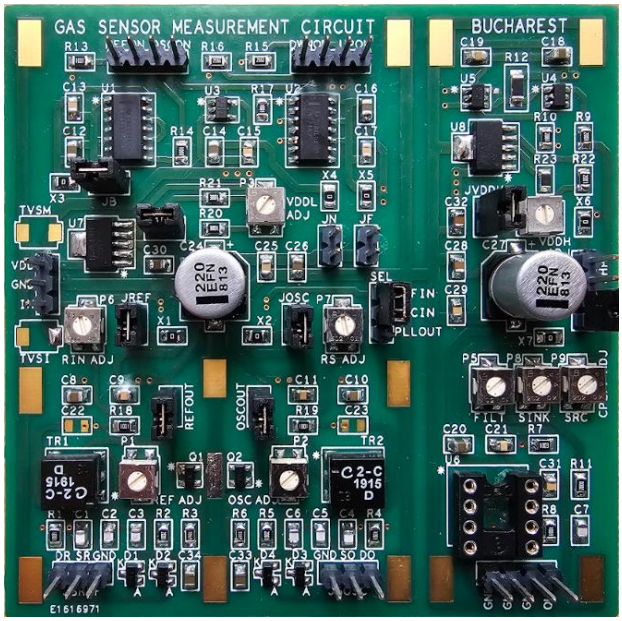


Figure 6.4 *Implemented CP-PLL III circuit*

The PCB in Fig. 6.4 is designed for the CP-PLL III, with two major directions in mind: star connections on the supplies (as in Fig. 4.9) and testability (creating the possibility of disconnecting PLL sub-blocks).

CP-PLL III validation starts by activating the main supply V_{DDM} and adjusting: V_{DDL} = 2.7 V as well as V_{DDH} = 7 V (Table 5.1). Then, the VCO is tested with varicap diodes connected and v_C = 2 V (Fig. 4.2). The waveforms in Fig. 6.5 are thus obtained, wherein the peak-to-peak amplitude of signal $v_{OUT}(t) \cong v_O(t)$ is ~75 mV_{pp} (small-signal condition).

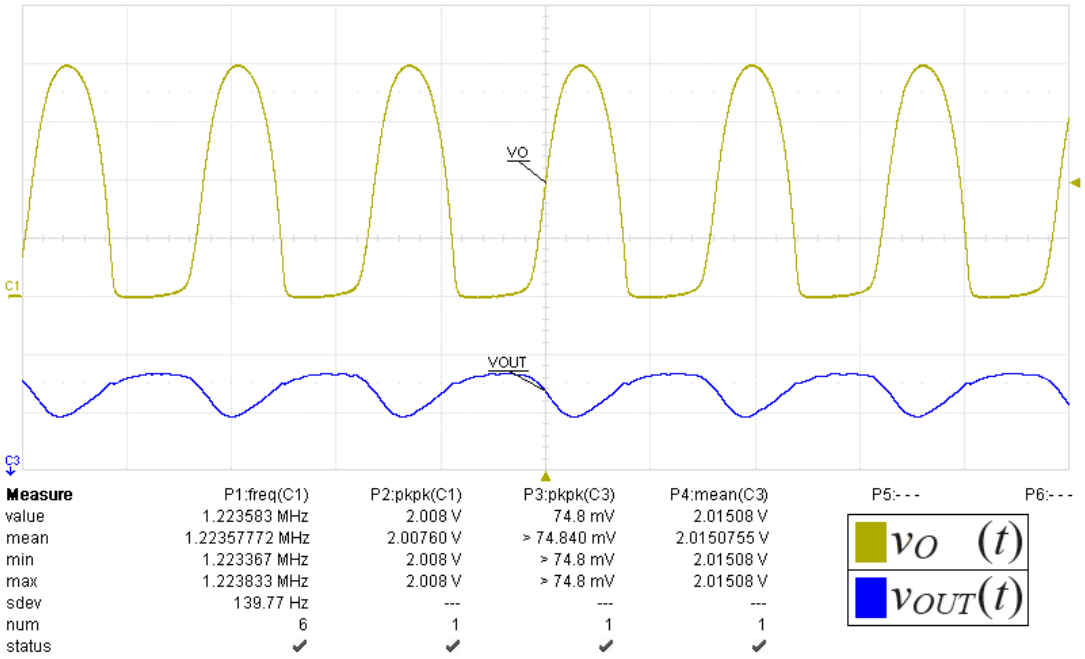


Figure 6.5 *Measured VCO waveforms for CP-PLL III circuit*

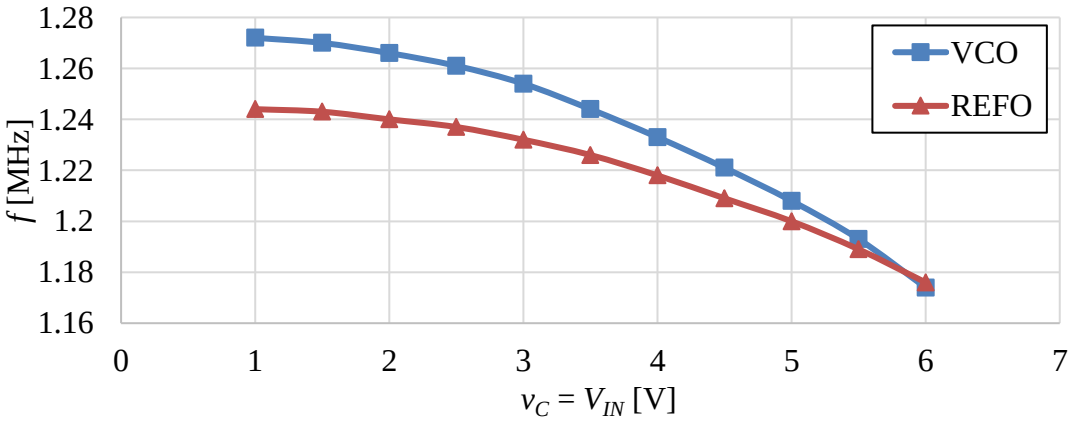


Figure 6.6 *Frequency-voltage characteristics of CP-PLL III oscillators*

A significant difference appears for $f_{osc} \cong 1.22$ MHz, ~20% higher than the target value (1 MHz). Therefore, both oscillators are tested (without varicap diodes) and $f_{ref} = 1.48$ MHz, $f_{osc} = 1.25$ MHz are obtained – for REFO, the change compared to simulations is even larger. Next, the calibration of the two oscillators is attempted, to equalize their frequencies. Thus, f_{ref} is reduced through increasing C_{TR} (Fig. 6.3) from 120 pF to 240 pF. Then, with the varicap diodes connected and $v_C = V_{IN} = 6$ V, R_C is adjusted to 2.63 kΩ, leading to $f_{osc} = f_{ref} = 1.17$ MHz. The measured frequency-voltage characteristics for the tuned oscillators are depicted in Fig. 6.6. Due to the differences between the two curves, Calibration Method 1 (CM1) cannot be utilized.

The waveforms from Fig. 6.7 are obtained by testing the entire CP-PLL III. Lock conditions are observed, given by $v_{OUT}(t)$ = constant and the short pulses seen on $v_{UP}(t)$ and $v_{DWN}(t)$. The current drawn by the locked CP-PLL III from V_{DDM} is ~17 mA.

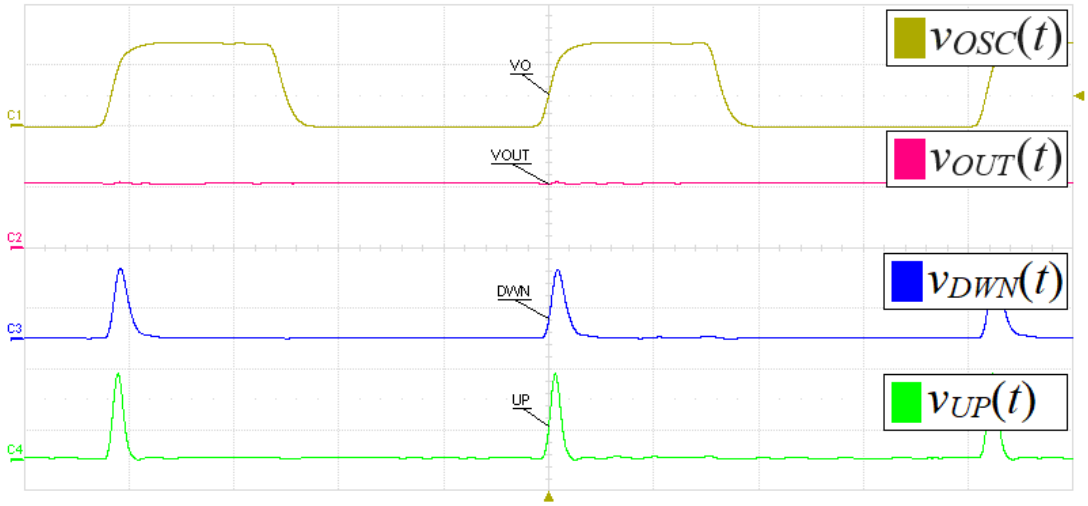


Figure 6.7 *Measured CP-PLL III circuit waveforms*

Given the validated PLL operation, Calibration Method 2 (CM2) is proposed:

1) With the VCO disconnected from the PLL, its $f_{osc}(v_C)$ curve is extracted;
2) For the entire CP-PLL, V_{IN} is varied and the $v_C(f_{ref})$ characteristic is extracted;
3) The two characteristics are represented in frequency-voltage coordinates. If the CP-PLL operates correctly, the two plots should be superimposed.

Calibration Method 2 is more complex, but it can also be used with the MOS sensor, as shown in Fig. 6.8 (R_C is set to 3 kΩ, in order to tune f_{osc} with the sensor).

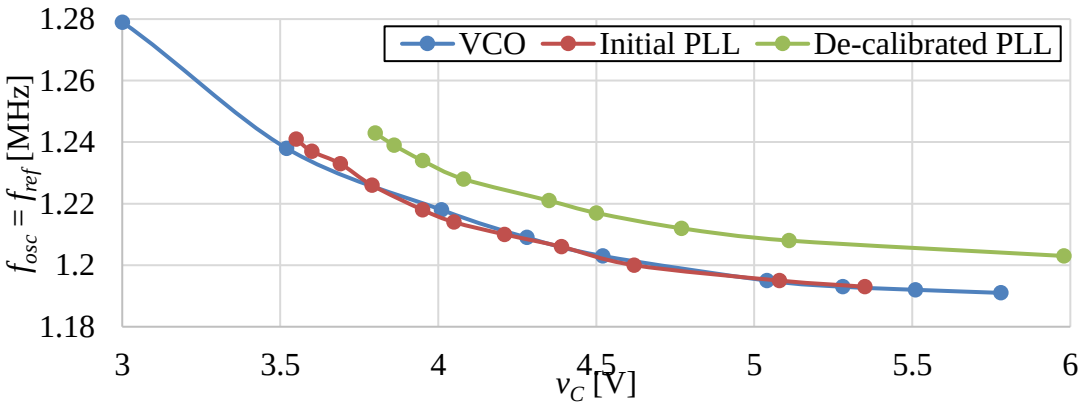


Figure 6.8 *Calibration Method 2 applied for CP-PLL III, with MOS sensor S4*

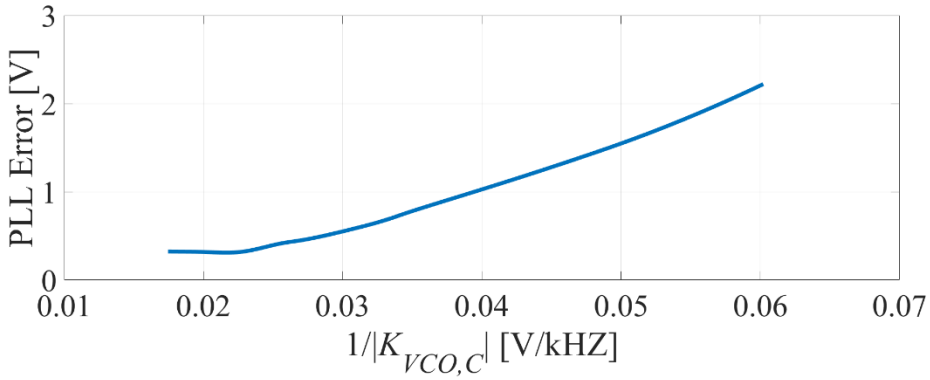


Figure 6.9 *De-calibrated PLL error versus the inverse of the VCO gain*

In Fig. 6.8, the VCO characteristic (blue) and that of the initial CP-PLL (red – R_{UP} = R_{DWN} = 2 kΩ) are overlapping. The errors between the two graphs, calculated using Matlab, are <100 mV for all evaluated v_C voltages. This result suggests that the CP-PLL III is already calibrated, without any tuning of the Charge Pump resistances. To validate the mismatch between the UP and DWN paths as an error source, the PLL is intentionally de-calibrated, by setting R_{DWN} to 4 kΩ (green – Fig. 6.8). In this case, the PLL curve does not overlap the VCO plot. Moreover, the VCO gain is evaluated and a linear error dependence on $1/|K_{VCO,C}|$ is observed (Fig. 6.9), similarly to Fig. 5.10.

Given the CP-PLL III is confirmed calibrated, H_2 detection tests are carried out. Firstly, the VCO is tuned so that the MOS sensor operates in the depletion region, for increased $K_{VCO,G}$ gain, as well as maximum H_2 sensitivity. In this case, an S4 sensor is used, with the $C_g(V_G)$ plots from Fig. 6.10.a. S4 is biased in the desired region by setting R_C to 2.81 kΩ: the VCO requires V_G = 3.3 V at f_{ref} = 1.204 MHz. The constant capacitance associated with V_G(0 ppm) = 3.3 V is ~107.05 pF. The voltage shift seen on the Keithley 4200-SCS is therefore $\mathbf{\Delta V_{0\text{-}1600}|_{Keithley} \cong 895\ mV}$. CP-PLL III generates a comparable value $\mathbf{\Delta V_{0\text{-}1600}|_{PLL} = 900\ mV}$ (Fig. 6.10.b). The difference between the two values is less than 1%. Consequently, the proposed Charge-Pump PLL topology is validated as a signal conditioning circuit for MOS sensors.

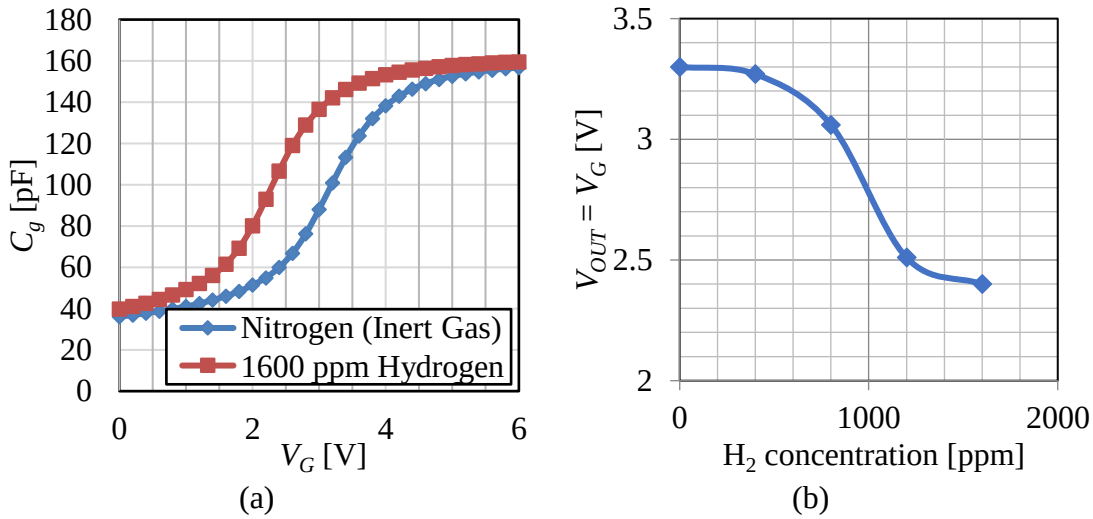


Figure 6.10 *H_2 detection with S4: (a) $C_g(V_G)$ (b) PLL voltage vs. H_2 concentration*

Chapter 7

Conclusions

7.1 Obtained results

The current doctoral thesis described the development of a signal conditioning (processing) circuit for MOS capacitor sensors used in H_2 detection. The process started with the innovative idea of using a well-known architecture, the Phase-Locked Loop, as an interface for non-linear capacitive sensors. Therefore, the Charge-Pump PLL (CP-PLL) topology was identified as optimal for the current application.

The circuit development followed the usual stages: sensor characterization (**Chapter 3**), development of the schematics of its blocks (**Chapter 4**), selection of component values and simulation (**Chapter 5**), PCB implementation and experimental validation (**Chapter 6**). Through this process, the main challenges in developing this type of circuit were identified, given the implementation using discrete components. Solutions were proposed for these limitations, either through schematic improvements or calibration of the implemented circuit. For the latter approach, two calibration methods were proposed, allowing for PLL error evaluation and correction. Results obtained through measurements using the final circuit variant (CP-PLL III, errors <1% in H_2 detection) validated both the viability of the PLL architecture as interface for nonlinear capacitive sensors, as well as the proposed design methodology.

All design requirements imposed at the beginning of **Chapter 4** are fulfilled in the final circuit variant (CP-PLL III), as demonstrated by Table 7.1.

Table 7.1 *Design requirements validation (CP-PLL III variant)*

No.	***Requirement***	***Result***	***Observation***
1	Sensor substrate at ground	✓	Armstrong topology used for the VCO
2	Bias voltage between 1...6 V	✓	CP and LPF I supplied by V_{DDH} = 7 V
3	1 MHz operating frequency	✓	Freq. of ~1.2...1.3 MHz, no effect on accuracy
4	Small-signal (≤100 mV_{pp})	✓	Sensor signal amplitude of 75 mV_{pp}
5	Operation with low R_g	✓	Correct lock obtained with R_S = 4 kΩ
6	Errors ≤100 mV	✓	≤100 mV in all tests (<10 mV cu H_2)
7	Possibility to calibrate	✓	VCO calibration was essential for testing

7.2 Original contributions

The Ph.D. thesis comprises the original contributions disseminated during the doctoral studies, through conference attendances, publication in journals, as well as through two patents:

1) Specialized literature synthesis and investigations regarding:
   - Data acquisition systems and sensor networks [12],[13].
   - Performances of conditioning circuits for sensors [10],[11],[12],[13].
   - Gas sensor, with focus on capacitive structures.
   - Signal conditioning (processing) circuits for capacitive sensors.
   - PLL architectures and block topologies for a Charge-Pump PLL.

2) Characterization and modeling of MOS capacitor hydrogen sensors:
   - Extraction of capacitance-voltage, resistance-voltage characteristics under different conditions (temperature, concentration) [3].
   - Investigation of the effect of humidity on sensor behavior [3].
   - Modeling techniques for non-linear devices [14],[15],[16],[17].
   - Development and validation of two Verilog-A models for SPICE simulation.
   - Modeling the sensor using two SMV1237 varicap diodes in parallel [1].
   - Discussion of two possible measurement principles using the MOS sensor: constant bias voltage or constant capacitance [3], [6].

3) Identification of the PLL architecture (more precisely, the Charge-Pump PLL) as an optimal implementation of the constant capacitance principle [1], [3].

4) Selection and development of principle schematics for the CP-PLL blocks, in order to ensure the operating conditions required by the SiC-MOS sensor and to allow for implementation using discrete components:
   - Adaptation of the Armstrong topology as Voltage-Controlled Oscillator and Reference Oscillator in the CP-PLL conditioning circuit [1],[3],[6].
   - Limiting the currents of the digital circuits in the Phase Frequency Detector, critical for reducing switching noise in the PCB implementation using discrete components. The trade-off between speed and noise [2],[3],[7],[8].
   - Development of a topology for the Charge Pump and Low-Pass Filter structure that allows for simple generation of constant currents, without using current sources [1],[3].
   - Elaboration of Calibration Method 1, based on replacing the sensor with varicap diodes and using two identical oscillators within the PLL [1].

5) Identification of the level shifter and driver circuit of the Charge Pump PMOS transistor as a critical block, with regard to its delay. Therefore, investigations were carried out in order to identify solutions for reducing the propagation delay of this block:
   - Comparison between topologies with an open-drain output stage [2],[7],[8] and those with a push-pull output stage [4],[5],[9].
   - Development of an improved push-pull output stage circuit [4].
   - Contributions to the creation of an improved open-drain circuit [2],[7],[8].
   - Selection of a simplified open-drain circuit, as a result of the limitations imposed by the implementation using discrete components [3].

6) Development of a dedicated supply circuit for the CP-PLL:
   - Investigation of two supply topologies for sensor signal conditioning circuits: chained supplies [11] and star connection [3].
   - Implementation for the CP-PLL of a star connection [3], with supply voltages generated using linear regulators, in order to minimize the noise introduced by switching circuits.

7) Modeling, design and simulation of CP-PLL conditioning circuit:
   - Modeling the PLL as a continuous time linear time invariant system.
   - Selection of the types and values of schematic components, based on circuit mathematical analysis and simulation results [1],[3].
   - Frequency-domain simulations, using the linear time invariant system model of the CP-PLL and the Verilog-A model for *AC* of the MOS sensor.
   - Time-domain simulations, using the CP-PLL schematic and the Verilog-A model for *transient* of the MOS sensor [1],[3].
   - Error reduction using Calibration Method 1 and identification of the Charge Pump speed mismatch as a source of imprecision [1].

8) Physical implementation and experimental validation of the CP-PLL circuit:
   - Implementation in two PCB variants and a prototype variant [3].
   - Voltage-Controlled Oscillator validation [3],[6].
   - CP-PLL signal conditioning circuit validation [3].
   - Elaboration of Calibration Method 2, relying on the identity between the characteristic of the Voltage-Controlled Oscillator and that of the CP-PLL.
   - Experimental confirmation of the speed mismatch between the two Charge Pump paths as an error source.
   - H_2 detection measurements (CP-PLL vs. characterization system) [3].

7.3 List of original publications

The original publications related to the doctoral thesis topic are listed, which contain the original contributions described in the previous section. These publications were cited in the previous chapters in the order the information appears in (the citations marked in green), but have been renumbered in the list below:

[1] **A. Enache**, F. Drăghici, G. Brezeanu, *A Calibration Technique of Charge-Pump PLL Readout Circuit for SiC-MOS Capacitor Hydrogen Sensors*, accepted for public defense at **2024 International Semiconductor Conference (CAS)**, Sinaia, Romania, 9-11th October 2024, **IEEE**.

[2] A.M. Drăgan, A. Neguț, **A. Enache**, I. Hurez, V. Anghel, G. Brezeanu, *In Focus: Data Hold Time for Temperature Sensors with High Speed I^2C Interface* in **Proceedings of 2023 International Semiconductor Conference (CAS)**, Sinaia, Romania, 11-13th October 2023, **IEEE**, **DOI: 10.1109/CAS59036.2023.10303655**.

[3] **A. Enache**, F. Drăghici, F. Mitu, R. Pascu, G. Pristavu, M. Pantazică, G. Brezeanu, *PLL-Based Readout Circuit for SiC-MOS Capacitor Hydrogen Sensors in Industrial Environments* in **Sensors**, 22(4), 1462, 14th February 2022, **ISI Q1 (2022)**, **WOS: 000769505800001**.

[4] **A. Enache**, A.M. Drăgan, A. Tache, *Digital Buffer Circuit*, **US10707872B1 Patent**, 7 July 2020.

[5] A.M. Drăgan, **A. Enache**, A. Neguț, A.M. Tache, G. Brezeanu, *An Improved I/O Pin for Serial Communication Interfaces* in **Romanian Journal of Information Science and Technology**, 22(2), pp. 158-180, 2019, **ISI Q1 (2024)**, **WOS: 000472166600006**.

[6] **A. Enache**, F. Drăghici, G. Pristavu, G. Brezeanu, *Voltage Controlled Oscillator for Small-Signal Capacitance Sensing* in **Proceedings of 2019 International Semiconductor Conference (CAS)**, Sinaia, Romania, 9-11th October 2019, **ISI**, **WOS: 000514295300068**.

[7] A.M. Drăgan, **A. Enache**, A. Neguț, A.M. Tache, G. Brezeanu, *A Fast Response Output Buffer for an I^2C High Speed Interface* in **Proceedings of the 2019 International Semiconductor Conference (CAS)**, Sinaia, Romania, 9-11th October 2019, **ISI**, **WOS: 000514295300029**.

[8] A.M. Drăgan, **A. Enache**, A. Neguț, A.M. Tache, G. Brezeanu, *An improved digital output buffer for a digital temperature sensor with an I2C high speed interface* in **Solid State Electronic Letters**, 1(2), pp. 147-151, July 2019, **SCOPUS**, **DOI: 10.1016/j.ssel.2020.01.003**.

[9] A.M. Drăgan, **A. Enache**, A. Neguț, A.M. Tache, G. Brezeanu, *A High Performance Mixed-Voltage Digital Output Buffer*, in **Proceedings of the 2018 International Semiconductor Conference (CAS)**, Sinaia, Romania, 10-12th October 2018, **ISI**, **WOS: 000514386700034**.

[10] I. Rusu, G. Brezeanu, G. Pristavu, F. Drăghici, **A. Enache**, B. Bucur, M.P. Bucur, R.G. Lucian, *Potențiostat de zgomot redus pentru măsurători amperometrice în soluții agitate magnetic*, **RO133208A2 Patent**, 29th March 2019.

[11] **A. Enache**, I. Rusu, B. Bucur, F. Drăghici, G. Pristavu, M.P. Bucur, F. Enache, G. Brezeanu, *Experimental characterization of a high accuracy amperometric sense and control circuit for three-electrode biosensors* in **Proceedings of the 2017 International Semiconductor Conference (CAS)**, Sinaia, Romania, 11-14th October 2017, **ISI**, **WOS: 000425844500037**.

[12] **A. Enache**, I. Rusu, F. Drăghici, G. Pristavu, G. Brezeanu, F. Enache, *High Accuracy Amperometric Sense and Control Circuit for Three-electrode Biosensors* in **Romanian Journal of Information Science and Technology**, 19(3), pp. 295-308, 2016, **ISI Q1 (2024)**, **WOS: 000405151400008**.

[13] **A. Enache**, I. Rusu, F. Drăghici, G. Brezeanu, G. Pristavu, F. Enache, *Smart Sensor for Chemical Compounds Concentration* in **Proceedings of the 2016 International Semiconductor Conference (CAS)**, Sinaia, Romania, 10-12th October 2016, **ISI**, **WOS: 000391323300041**.

[14] G. Pristavu, D.T. Oneață, R. Pascu, A.E. Marcu, M.C. Șerbănescu, **A. Enache**, F. Drăghici, G. Brezeanu, *Accurate Numerical Methods for Modeling Forward Characteristics of High Temperature Capable Schottky Diodes* in **Romanian Journal of Information Science and Technology**, 27(2), pp. 196-206, 2024, **ISI Q1 (2024)**, **DOI: 10.59277/ROMJIST.2024.2.06**.

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From these, papers [1-9] were published during the doctoral studies and are directly related to the Ph.D. topic. Publications [10-13] target sensor signal conditioning circuits as well, leading to accumulated experience in the field, and having a key role in establishing the thesis topic. Papers were also published as co-author on the topic of Schottky contact modeling [14-17]. The principle described in these publications was one of those considered for the nonlinear sensor modeling. Moreover, the experience in numerical methods from this research was useful in the development of the thesis.

Some of the listed papers were published as part of the requirements of two national research projects, for which there existed contributions as doctoral researcher:

• **PN-III-P1-1.1-TE-2021-0231 (TE17/2022)** – *Software Tool for Seamless Parameter Extraction and Characterization of Schottky Barrier Diodes based on Emerging Implicit Differentiable Models (SBD-SPECS)* – publications [13-16];

• **PN-III-P1-1.2-PCCDI-2017-0419 (71PCCDI/2018)** – *Sensors and Integrated Electronic and Photonic Systems for people and Infrastructures Security (SENSIS)* in sub-project *SiC-based Hydrocarbons Sensors for Security in Hostile Industrial Environments* – publications [3], [6];

7.4 Perspectives for further developments

For the proposed CP-PLL signal conditioning circuit, the most obvious potential development relates to its adaptation for other nonlinear capacitive sensors. For instance, depending on the sensor and the working frequency, the two oscillators may need to be resized. Moreover, if the desired frequency is too high, the noise reduction solution based on limiting the output currents of the digital circuits may have to be modified or removed altogether.

In fact, if higher working frequencies are desired, the most convenient solution would be to integrate, at least partially, the PLL circuit. In this manner, the switching blocks could be designed especially for this application, in order to obtain the optimal trade-off between speed and noise. Moreover, in the integrated approach, the improved level shifting and driving circuits (low propagation delays and high switching speeds) could be easily implemented. Consequently, the mismatch of the charge pump, a major error generator, could be significantly reduced. In this approach, the two oscillators must either use a topology without inductive components (but similar performances) or remain implemented with discrete components (as in the existing version).

Another research avenue, related to the CP-PLL implementation using discrete components, is to investigate solutions for increasing the matching of the oscillators. In the current version, the most probable sources of mismatch are the transformers and the transistors. Thus, potential solutions could imply designing dedicated transformers and using dual bipolar transistors (two identical devices in the same semiconductor die). Consequently, Calibration Method 1 (CM1), easier to execute than Calibration Method 2 (CM2), could also be used in measurements (not only in simulations).

Regarding the design methodology presented in the doctoral thesis, there is potential for further development in the area of frequency domain analysis. For the proposed continuous time linear time invariant system model of the CP-PLL, the correlation with time domain simulations was only partial. Thus, if a discrete time model were implemented (using the Z-transform), it is possible that a better correlation could be achieved. In this manner, the developed model could serve as a reliable predictor for the stability of the negative feedback-based PLL system.

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