Diana Dranga

[redacted]

Skilled engineer in functional verification, embedded, machine learning and scripting. Experience of 9+ in the semiconductor industry on different complexity levels and domains (automotive, space, security, etc).

TECHNICAL SKILLS

Protocols used: AXI, APB, AHB, ACE, AXI Stream, Wishbone, USB, RDMA, InfiniBand, Custom.
Subsystems: CPU, Network IP, Debug, peripherals.
Verification Tools: System Verilog/UVM.
Machine Learning tools: Python, TensorFlow.
HDL/HVL: Verilog, System Verilog.
Digital Simulators: QuestaSim/NCSim/VCS.
Software: Assembly/C/JAVA/CUDA.
Scripting: Python, Perl.
Versioning Tools: CVS, ClearCase, GIT.
Other Tools: Certitude, Atlassian Suite.
Others: Agile/SCRUM.

WORK EXPERIENCE

Senior Verification Engineer | Bucharest, Romania **Mar 23 – now**
Capgemini

- Worked on ADC unit level project, automotive security projects at different clients.
- Used System Verilog, C and UVM.
- Used a SCRUM/Agile approach in an international multidisciplinary team.

Senior Verification Engineer | Bucharest, Romania **Jan 22 – Mar 23**
Qualitest Corporation

- Working on for an American company which founded the x86 processor.
- Working with Remote Direct Memory Access (RDMA) and InfiniBand protocols.
- Working on cluster level with SV/UVM.
- Worked on XLR, CQ features of RDMA and coverage implementation.

Verification Engineer | Bucharest, Romania **Jul 21 – Jan 22**
Xperi Corporation

- Design and architect System level testbench (SV/UVM).
- Implemented testbench (70%).
- Worked on part of a Neural Engine with multiple engineers of different fields.
- Worked with DPI – C.
- SCRUM/Agile methodology.

Verification Engineer | Bucharest, Romania **Jun 20 – Jul 21**
Nobug Consulting

- Building a verification environment for an SPI Master Core
- Working on Amazon Kuiper project (low altitude satellites), using C, System Verilog, and a tad Assembly.
- Worked on Network Subsystem in C and SV/UVM.
- Building a verification environment for an SPI Master Core.
- Using GIT and Synopsys VCS suite.

Test Developer Engineer, Secure Software IP | Bucharest, Romania **Apr 20 – Jun 20**
NXP Semiconductors

- Written embedded C test for secure chips.
- Debugged issues using IAR Embedded Workbench.
- Used Git/GitHub for system versioning.

Digital Functional Verification Engineer, MCU16 | Bucharest, Romania **Nov 17 – Apr 20**
Microchip Technology Inc.

- Updated testbench and added new features, in System Verilog and Assembly at SoC level.
- Worked for multiple multi-core and single core projects. Processors were general purpose.
- Implemented, debugged, and solved important issue ranging from CPU, Debugger issues to peripherals.

- Participation in DVCON India 2019.

Verification Working Student, CCS | Bucharest, Romania **Sept 15 – Nov 17**
Infineon Technologies AG

- Written from scratch a verification environment for a module with Senior Engineer guidance.
- Updated testbench and added features for two different ARM modules, from what a module level point of view for CCS chips.
- Usage of Certitude.
- Verification of a watchdog module.

ADDITIONAL TECHNICAL PROJECTS

Artificial Intelligence: Convolutional Neural Networks algorithms **Jan 24 – June 24**

- Architected, implemented, debugged, and fine-tuned a Convolutional Neural Network algorithm. The algorithm's goal is to identify critical and non-critical information in a text. The dataset was created from scratch from online available PDFs.
- More information can be found at: https://www.mdpi.com/2832126

Artificial Intelligence: Large Language Models used in testbench generation **Jan 24 – Mar 24**

- Analysed the potential of Large Language Models (LLMs) in the verification field with promising results.
- Generated and correct a UVM APB testbench environment from scratch using the LLM.
- Two approaches used: one is text-prompt, and the other is image-based prompt. Both approaches provide favourable results.
- More information can be found at: https://doi.org/10.33436/v34i2y202406

Artificial Intelligence: Large Language Models used in System Verilog Assertions generation **Jun 24 – Sep 24**

- Analysed how the Large Language Models can generate different System Verilog Assertions.
- Presented key elements, success and issues the engineer must be sure to assess.
- More information can be found at: https://www.mdpi.com/2970558

University project USB Host functional verification **Jan 19 – Jun 19**

- functional verification of an USB module using UVM methodology and System Verilog
- creation of a simulation manager in Perl used for compilation, optimization, simulation, regression, and fault injection.

University project Filtering Algorithm using Computer Unified Device Architecture **Jan 17 - Jun 17**

- using NVidia CUDA cores located in a GPU920M and implementing a filtering algorithm.
- compare the CPU and GPU running time and resource needed.

LEADERSHIP AND AWARDS

Honourable mention at the Scientific Communications. **May 17**

- awarded for: filtering algorithm using Computer Unified Device Architecture.

Certificate in Advanced English **May 11**

First Certificate in English **May 10**

EDUCATION

Polytechnic University of Bucharest, Faculty of Electronics, Telecommunication, and Information Technology | Bucharest

Phd in Functional verification using AI (in progress) **Oct 19 - now**

Master of Engineer in Software **Oct 17 – Jun 19**

Bachelor of Engineering in Networks, Software and Communications **Oct 13 – Jul 17**