NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY POLITEHNICA BUCHAREST

Doctoral School of Electronics, Telecommunications and Information Technology

Decision No. 160 **from** 05-09-2024

Ph.D. THESIS SUMMARY

Florin-Silviu DUMITRU

CONTRIBUŢII LA ANALIZA ŞI PROIECTAREA MICROSTRUCTURILOR ELECTRONICE

CONTRIBUTIONS TO THE ANALYSIS AND DESIGN OF ELECTRONIC MICROSTRUCTURES

THESIS COMMITTEE

Prof. Dr. Ing. Gheorghe BREZEANU National University of Science and Technology POLITEHNICA Bucharest	President
Prof. Dr. Ing. Gheorghe ȘTEFAN National University of Science and Technology POLITEHNICA Bucharest	PhD Supervisor
Prof. Dr. Ing. Claudius DAN National University of Science and Technology POLITEHNICA Bucharest	Referee
Prof. Dr. Ing. Aurel-Ștefan GONTEAN Politehnica University of Timișoara	Referee
Assoc. Prof. Dr. Ing. Sorin Dan COȚOFANĂ Delft University of Technology	Referee

BUCHAREST 2024

Table of contents

Chapter 1

Introduction

As CMOS technology rapidly approaches atomic-scale dimensions, it faces increasingly severe challenges, including power density limits, rising leakage currents, reduced IC lifespans due to reliability concerns, declining yields, and unsustainable manufacturing costs. These challenges are driving renewed research efforts focused on novel materials, devices, architectures, and computing paradigms [1–7].

What is far more likely than silicon's replacement is silicon's augmentation using novel channel materials, contact technologies, and even combining silicon-based technology with nontraditional materials [8]. Unlike 3D materials such as silicon, 2D materials like graphene offer an inherently planar structure that allows for unprecedented electron mobility, thermal conductivity, and even manifest the electric field effect [1, 6, 9].

While changing silicon already implies nothing short of a *revolution* in microelectronics, it must also be mentioned that *only* adopting nanomaterials won't be enough. In addition to new materials, it is thought that new architectures, such as neuromorphic computing and in-memory computation, must be explored in order to further the progress of computing [4, 5, 7].

To summarize these ideas, limiting ourselves to the technological point of view, the enhancement of silicon must use less power and dissipate heat more efficiently. Lastly, what Moore coined 'device and circuit cleverness' [10] could be achieved using devices with more complex electrical characteristics than the basic transistor.

1.1 Presentation of the field of the doctoral thesis

The classic silicon-based semiconductor industry is approaching the limits of scaling for the CMOS transistor due to both power dissipation and to channel length limitations [5, 4, 3, 6]. The question regarding the limits of CMOS scaling was studied in depth by Dennard in [11] leading to the scaling procedure applied to CMOS devices for the following decades to be coined *Dennard scaling*.

In parallel, there is a continuous search for alternative materials which provide better performance than silicon with a focus on thermal conductivity, leakage current, carrier mobility, and most important of all exhibit the electric field effect at these dimensions. One such material is graphene, a zero gap semi-metal, which was successfully isolated for the first time in 2004 [1]. It is currently the material with the best reported thermal conductivity achieving $5.30 \pm 0.48 \times 10^3$ W/mK [12], exceeding the results of the best carbon nanotubes (SW-CNT) which achieved 3.5×10^3 W/mK [13]. From a leakage current perspective, given its semi-metal status, it typically exhibits poor I_{on}/I_{off} ratios in the range of 30 [1] up to 100 [14], but it was shown that by exploiting it's large confinement gap [15] significantly larger I_{on}/I_{off} ratios can be achieved for very narrow sub-10 nm wide devices [16]. This performance was achieved as a consequence of graphene's strong ambipolar electric field effect [1]. High-quality graphene also achieves gigantic mobilities of 2×10^5 cm^2 V^{-1} s^{-1} at room temperature for fragile suspended graphene and over 5×10^5 cm^2 V^{-1} s^{-1} when encapsulated in boron-nitride at low temperature [17].

For the above mentioned reasons it is now clear why 2D materials, such as graphene, are on the International Roadmap of Devices and Systems's (IRDS) roadmap as near term extensions to existing CMOS technology, as shown in Figure 1.1.

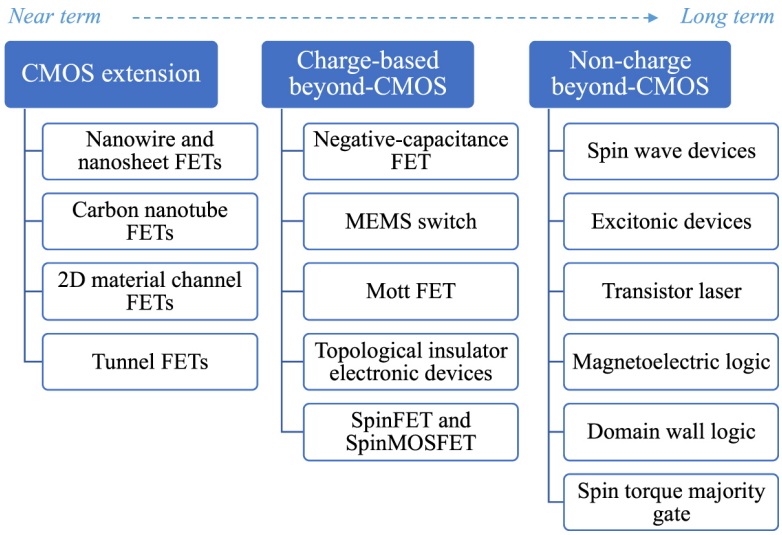


Fig. 1.1 Categories of emerging logic and information processing devices [6] by An Chen in "Beyond-CMOS roadmap-from Boolean logic to neuro-inspired computing," licensed under CC BY 4.0.

In addition to novel computing architectures, the adoption of graphene technology requires not only graphene-based Boolean logic [18–20], but also the development of fundamental digital and mixed-signal circuits typically found in microcontrollers, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), oscillators, and others.

1.2 Scope of the doctoral thesis

The scope of this thesis is to explore the potential of graphene to extend the capabilities of standard silicon-based CMOS technology. To achieve this, the research will focus on designing and analyzing device-level graphene-based microstructures for various analog and digital functions.

These tasks have been summarized as a list of objectives presented below.

1. Examine the design trade-offs and minimum requirements of the mixed-signal blocks, particularly if risk mitigation is required due to potential underperformance of graphene-based implementations. Simulations may be conducted using CMOS for technology-agnostic parameters. The limited analog performance of graphene will be considered when evaluating risk.

2. Design and simulate graphene-based device-level microstructures optimized for the implementation of general-purpose digital and mixed-signal circuits.

3. Obtain clear 'on' and 'off' states for the microstructures used in the implementation of the digital, mixed-signal, and neuromorphic blocks by manipulating their conductance using control voltages.

4. Propose digital, mixed-signal, and neuromorphic blocks to support the development of fully GNR-based integrated circuits (ICs) and application-specific ICs (ASICs)

5. Perform circuit-level simulations for the digital, mixed-signal and neuromorphic graphene-based circuits designed in order to confirm their correct operation.

6. Evaluate the potential of graphene-based neuromorphic blocks to extend the capabilities of standard silicon-based CMOS by comparing the proof of concept benchmark results of the FinFET and graphene-based circuits in terms of performance.

1.3 Content of the doctoral thesis

The remaining content of this thesis is structured as follows:

In Chapter 2 we present a detailed review of the literature covering the state of the art of graphene technology with emphasis on both graphene's intrinsic and engineered properties, as well as methods of manufacturing.

In Chapter 3 we present a graphene nanoribbon (GNR)-based 5-bit, current output, digital to analog converter (DAC) design. The basic building block of this DAC is a GNR device fulfilling the role of analog current source. Its specific non-rectangular shape, carved out of a bulk sheet of graphene, leads to a couple of consequences which make

it viable for use in analog design. The first is the opening of a bandgap, which enables us to modulate the current flowing through the device using a phenomenon familiar to use from classic CMOS technology, i.e., by using of the field effect. The second equally important consequence of the non-rectangular shape's geometry are the device's output and transfer characteristic which resemble the characteristics of a bipolar junction transistor (BJT) or CMOS implementation. The performance of this GNR-based DAC is compared to that of a 7 nm FinFET implementation that uses the same topology.

In Chapter 4 we explore the use of GNR-based devices for a more complex, hardware-based, machine learning application. To this end, we propose a graphene nanoribbon-based McCulloch-Pitts neuron (GNR-MCPN) implementation constructed exclusively using GNR devices. Its implementation includes digital cells, such as GNR-based logic gates (GNR-L) and GNR-based static random-access memory (GNR-SRAM), as well as analog cells, such as current sources and high-side and low-side switches. We validate the proposed neuron's functionality using a basic one-layer neural network capable of processing a 5 by 5 pixel matrix dynamically configured using its SRAM to detect vowels.

In Chapter 5 we present an ultra-low-power, GNR-based, current-starved, ring oscillator design. Oscillator output frequency tunability is achieved by driving the gate voltage of the current source device using a DAC. We validate our design against a 7 nm FinFET implementation in terms of output frequency tunability range, power consumption, and power efficiency.

In Chapter 6 we explore the segmentation technique for enhancing DAC resolution. This technique enables us to enhance the differential non-linearity (DNL) at the cost of increased decoder complexity and active area required. The performance comparison is performed using a standard CMOS technology across all intermediate degrees of segmentation possible between the purely binary and thermometric implementations, but it can readily be applied to GNR-based implementations or any other technology.

In Chapter 7 we explore the impact that operational amplifier non-idealities have on a $\Sigma\Delta$ analog to digital converter (ADC) modulator's performance. The $\Sigma\Delta$ ADC was chosen due to its ability to achieve high resolutions with modest analog operational amplifier specifications, especially if a 1-bit quantizer is used in the modulator, thus avoiding stringent linearity requirements on the quantizer. The outcome of this investigation are the slew rate and bandwidth requirements for achieving a resolution of 16 bits, laying the groundwork for implementing a GNR-based implementation for the $\Sigma\Delta$ modulator with minimal analog complexity.

Finally, Chapter 8 provides a short summary the thesis and seeks out relevant targets for future research.

Chapter 2

Graphene Technology

2.1 Introduction

Graphene, a 2D carbon allotrope with a hexagonal atomic arrangement, was long considered a theoretical material due to predictions of its thermodynamic instability in 2D crystals [21, 22]. This view, supported by the Mermin-Wagner theorem [23], which states that thermal fluctuations at finite temperatures would disrupt long-range order. However, in 2004, Geim and Novoselov isolated graphene using the 'Scotch tape' method [1], earning them the 2010 Nobel Prize in Physics. Their work confirmed graphene's semimetal nature and ambipolar electric field effect, enabling control of 2D electron and hole gases via gate voltage [1]. This breakthrough sparked extensive research into graphene's unique properties and potential applications [24].

2.2 Properties of graphene

In 1947, Wallace [25] applied band theory and the tight-binding approximation to link graphite's electrical, thermal, diamagnetic, and optical properties to underlying phenomena. He noted that large interlayer spacing justifies treating conduction as occurring within isolated hexagonal layers [25]. From this, key graphene properties were predicted: a unique band structure with Dirac points [25, 1, 26], zero-activation-energy semiconductor behavior [25], and strong in-plane conductivity with much lower interlayer conduction [25].

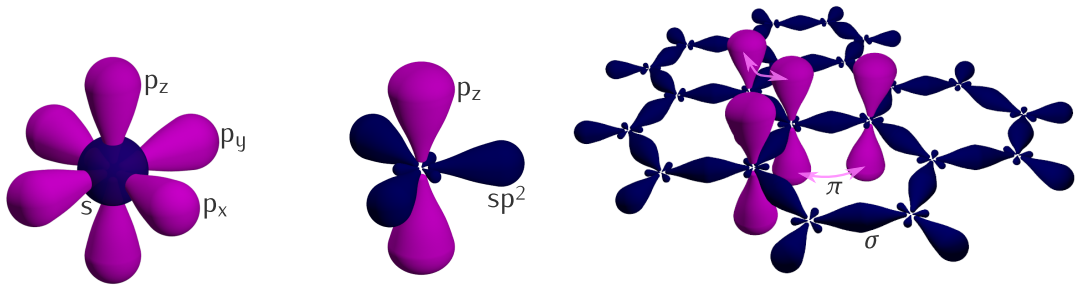
After graphene's isolation from graphite via the 'Scotch tape' technique [1, 27], experiments confirmed its remarkable thermal conductivity, current densities, tensile strength, ballistic transport, carrier mobility, ambipolar field effect, minimum conductance, and quantum Hall effect. We will discuss the most relevant properties for microelectronics in the following sections.

2.2.1 Crystalline structure: 2D or not 2D

Graphene is a 2D material comprised of carbon atoms arranged in a honeycomb-shaped lattice. To better understand graphene's electron structure we must first consider carbon's ground-state electron configuration, represented in Figure 2.1a (left), which is $1s^2 2s^2 2p^2$ with the four outer-shell electrons fulfilling the roles of valence electrons.

In graphene's case, each carbon atom undergoes sp^2 hybridization mixing one 2s orbital and two 2p orbitals, more specifically the p_x and p_y orbitals, to form three equivalent sp^2 hybrid orbitals accompanied by a $2p_z$ orbital [25], as shown in Figure 2.1a (right).

The hybrid sp^2 orbitals reside in the plane of the graphene sheet, are spaced 120° apart, and by overlapping with the sp^2 orbitals of the three neighboring carbon atoms form the covalent σ bonds of the graphene lattice. The remaining $2p_z$ orbital, which is perpendicular to the graphene sheet's plane, does not take part in the sp^2 hybridization, but instead overlaps with the $2p_z$ orbitals of neighboring atoms to form covalent π bonds [26]. These π bonds form a delocalized π-system above and below the graphene plane and grant graphene its conductivity. The geometry of the σ and π bonds of a graphene layer is represented in Figure 2.1b.



(a) Carbon ground-state and sp_2 hybrid orbitals by Ponor, licensed under CC BY-SA 4.0.

(b) Graphene - σ (blue) and π (purple) bonds by Ponor, licensed under CC BY-SA 4.0.

Fig. 2.1 Carbon ground-state and hybrid orbitals and their resulting bonds in graphene

Although a carbon atom has a measurable radius, graphene is considered 2D because its electrons remain confined to a plane, and stacking additional layers changes its properties [8, 14]. Predictions by Peierls, Landau, and Mermin suggested 2D crystals should be unstable [21–23], but graphene's atomic-scale ripples stabilize its structure [8]. By carving, rolling, or stacking graphene, one obtains fullerenes (0D), carbon nanotubes (1D), or graphite (3D).

2.2.2 Electronic properties

Layer Number Dependent Electronic Properties in Graphene

As more graphene layers stack, the electronic structure shifts toward that of bulk graphite, raising questions about when the 3D limit is reached [28]. Single-layer graphene, is a

zero-gap semiconductor with a linear Dirac-like spectrum near the Fermi energy [8]. This creates massless Dirac fermions [29, 14, 9] moving at a Fermi velocity of $v_F = 10^6 \mathrm{m/s}$, yielding very high electron mobility and conductivity[26].

Bilayer graphene is a semimetal with a tiny 1.6 meV band overlap and a parabolic spectrum, producing massive Dirac fermions that combine Dirac and Schrödinger characteristics [28, 9]. Uniquely, an electric field can open a band gap in bilayer graphene [26, 30, 31], the existence of this tunable gap enhances its potential for technological applications.

For three or more layers, the band overlap gradually shifts from 1.6 meV (bilayer) toward the 41 meV overlap of bulk graphite. By 11 layers, the overlap differs from bulk by less than 10 %, and layers 3 to 11 all exhibit semimetallic behavior. This arises from interactions of the B sublattice with next-nearest neighbor planes [28].

Graphene Monolayer Properties

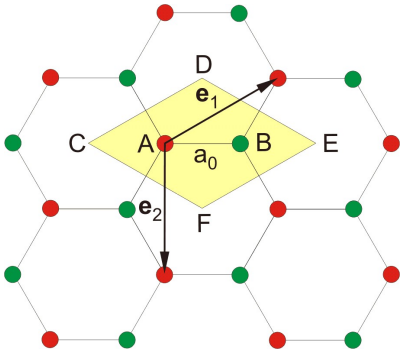
High-quality graphene on SiO_2 substrates exhibits mobilities up to $1.5 \times 10^4\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ to $4 \times 10^4\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ at $1 \times 10^{12}\ \mathrm{cm^{-2}}$, close to the $7.7 \times 10^4\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ of InSb, the highest-mobility known semiconductor [32, 33]. Scattering by substrate optical phonons limits performance, but suspending graphene 150 nm above the substrate increases mobility beyond $2 \times 10^5\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ at room temperature and $1 \times 10^6\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ at low temperature [17, 34]. Encapsulation in BN yields similar high mobilities [17].

Such low scattering enables ballistic transport [35], where electrons traverse without collisions, avoiding Joule heating. Here, conductance is governed by interface resistances and quantized transverse modes, as captured by the Landauer formula [36–38].

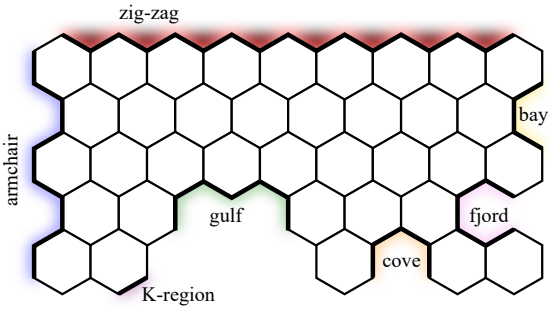
In ballistic conductors, all Joule heat dissipates at the contacts rather than along the channel [36]. Due to its superior electronic properties, graphene can sustain submicron ballistic transport [9, 26], and when placed on boron nitride substrates, it achieves micrometer-scale ballistic transport even at room temperature [17]. Graphene also supports current densities of $10^8\ \mathrm{A/cm^2}$ to $10^9\ \mathrm{A/cm^2}$, exceeding copper by orders of magnitude [1, 39, 40, 9], making it a promising candidate for future interconnects.

Geometry-induced Graphene Monolayer Properties: Narrowing things down

Graphene nanoribbons (GNRs) are monolayer nanostructures whose electronic properties depend on their edge geometry, differentiating them from 0D fullerenes and 1D nanotubes through the presence of open edges [8]. Literature distinguishes armchair-edge (AGNR) and zigzag-edge (ZGNR) types, as shown in Figure 2.2b, while more complex edge geometries are discussed in [41]. When GNRs have infinite length and widths exceeding two hundred unit cells (Figure 2.2a), their behavior aligns with standard zero-gap graphene [26].



(a) The hexagonal crystal structure of graphene with unit cell (CDEF) and the fundamental lattice displacements (e1, e2). by Ququ, licensed under CC-SA 3.0.



(b) Graphene edge names representation. by Andel, licensed under CC0 1.0.

Fig. 2.2 Graphene lattice unit cell and GNR lattice edges

By carefully engineering edge geometry and width, a bandgap can be created in graphene nanoribbons (GNRs) [8, 42, 43]. ZGNRs are always metallic due to unique edge states arising from their zigzag configuration [26, 43, 44]. In contrast, AGNRs show a width-dependent transition: if $N = 3M - 1$ (with M integer), they are metallic; otherwise, they are insulating [43]. The bandgap in AGNRs is inversely proportional to their width and is notably larger than typical semiconductor gaps, due to graphene's linear spectrum and high Fermi velocity [8, 14, 42, 15]. Experiments confirm this confinement gap and the ability to tune it by geometry, as shown in Figure 2.3 [42]. Sub-10 nm AGNRs achieve I_{on}/I_{off} ratios of 10^7 [16], illustrating how geometry governs their electronic properties [44]. This prompts exploration of non-rectangular GNRs, which may not fit the simple AGNR or ZGNR classifications.

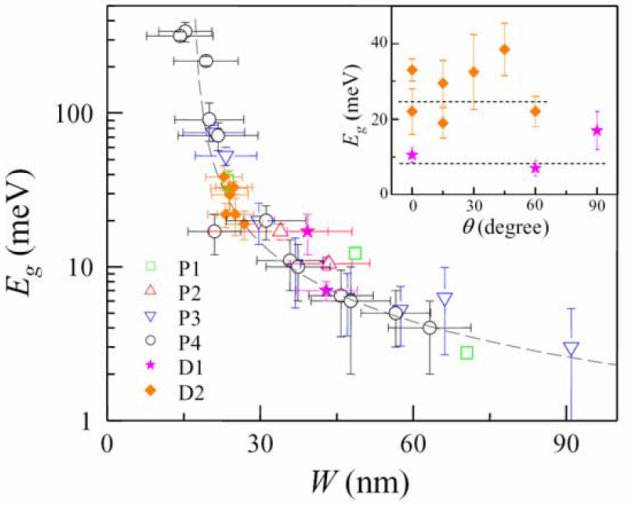


Fig. 2.3 Measured band gap as a function of device width. Reprinted figure with permission from [42]. Copyright 2024 by the American Physical Society.

2.2.3 Thermal properties

After its impressive current densities, graphene's thermal properties are equally remarkable. Suspended graphene monolayers achieve room-temperature thermal conductivities up to $(4.84 \pm 0.44\text{-}5.30 \pm 0.48) \times 10^3$ W/mK [12], exceeding that of CNTs and SWCNTs [13] and making graphene highly promising for thermal management. Figure 2.4 illustrates the measurement setup, where a laser heats a graphene monolayer mounted over a trench, allowing heat to flow to the sinks at both ends.

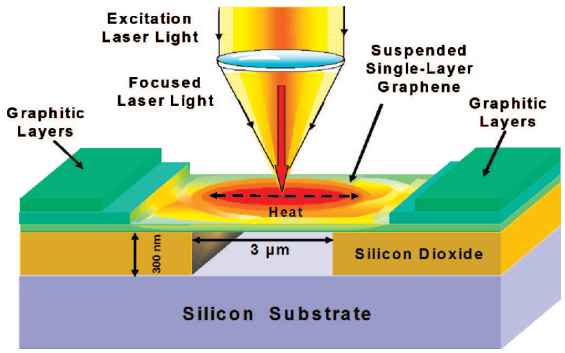


Fig. 2.4 Setup used for measuring the graphene monolayer's thermal conductivity. Reprinted with permission from [12]. Copyright 2024 American Chemical Society.

2.3 State-of-the-art fabrication technology

Two fundamental approaches exist for graphene fabrication: top-down and bottom-up. Top-down starts with bulk graphite and etches it, causing edge roughness [8], while bottom-up assembles structures from atomic levels, providing atomically precise edges and customizable geometries [45].

2.3.1 Top-down Synthesis

Micromechanical exfoliation, or the 'Scotch tape' technique [1], leverages van der Waals forces to isolate graphene layers from bulk graphite. Though unsuitable for mass production, it produces defect-free monolayers with high mobility [8]. Another method involves decomposing carbides: heating SiC surfaces forms a carbon interface layer that, when the second layer develops, yields epitaxial graphene exhibiting nearly isolated graphene properties [46].

Flattening CNTs (squashing) creates GNRs with atomically smooth edges [47], enabling sub-10 nm structures with substantial I_{on}/I_{off} ratios and band gaps. Electron beam lithography (EBL) can also fabricate narrow GNRs with confinement-induced band gaps [42] (Figure 2.3), achieving sub-10 nm resolution for multilayer graphene [48].

2.3.2 Bottom-up Synthesis

Chemical vapor deposition (CVD) on Cu [49] and Ni [50] substrates achieves large-scale graphene films. On Cu, the low carbon solubility enables self-limited growth, producing predominantly single-layer graphene over cm-scale areas [49]. CVD on Ni at ambient pressure yields continuous single- to few-layer graphene with 20 μm-wide regions, which can be transferred and patterned lithographically [50].

Atomically precise graphene nanoribbons (GNRs) can be fabricated by surface-assisted coupling of molecular precursors, followed by cyclodehydrogenation, as shown in [51, 52]. This bottom-up approach tailors edge geometries through precursor design, enabling structures with controlled chemical, electronic, and magnetic properties.

2.4 Data converter topologies

As graphene pushes electronics beyond silicon, analog-to-digital and digital-to-analog conversion becomes a key challenge. Real-world applications demand analog/digital interfaces, so focusing on ADC and DAC topologies that minimize analog complexity and shift more tasks to the digital domain can improve mixed-signal performance and shorten design cycles.

2.4.1 Digital to Analog Converters

The current-steering DAC is a simple, efficient solution that converts digital bits directly into currents, minimizing intermediate stages and circuitry. Its key challenges involve balancing linearity with decoder complexity, an aspect we aim to address using GNR-based implementations. These ultra-fast DACs support high-speed, multi-level communication schemes like PAM-4, which already achieves 112 Gbps chip-to-chip transmissions [53], and may scale to even more signal levels in the future.

2.4.2 Analog to Digital Converters

A ΣΔ ADC modulator requires less demanding analog circuitry than other ADC topologies, relying on oversampling and digital filtering rather than precise analog components. This reduces sensitivity to low I_{on}/I_{off} ratios and limited output resistance. By shifting complexity into the digital domain, errors are mitigated through digital filtering.

We will examine the minimum analog performance needed to achieve 16-bit resolution at 1 kHz bandwidth using a ΣΔ topology. Though graphene's intrinsic I_{on}/I_{off} ratios are modest (30-100) [1, 14, 54], its high 100 GHz cut-off frequency [54] suggests that a high oversampling ratio can compensate.

Chapter 3

Graphene Nanoribbons-Based 5-Bit DAC

McCulloch-Pitts neuron structures combine multiple synaptic inputs with a decision element (soma). We propose a 5-bit graphene nanoribbon (GNR)-based DAC serving as the summation element with programmable weights [55]. It employs GNR unit current cells and a GNR logic thermometric decoder. Using a MATLAB-based GNR Verilog-A model for SPICE analysis, we selected cell geometry and bias conditions from the GNR conductance map. Compared to a FinFET design, the GNR-based DAC reduces active area by a factor of three while maintaining similar DNL and INL performance at a supply of 0.2 V, achieving a DNL of -0.196 LSB to 0.088 LSB and INL of -0.809 LSB to 0.364 LSB.

This chapter is based on the following original publications:

F. -S. Dumitru, N. Cucu-Laurenciu, A. Matei and M. Enachescu, "Graphene Nanoribbons Based 5-Bit Digital-to-Analog Converter," in IEEE Transactions on Nanotechnology, vol. 20, pp. 248-254, 2021, doi: 10.1109/TNANO.2021.3063602.

3.1 Introduction

CMOS technology faces increasing challenges at atomic dimensions, including dominant static power consumption, rising costs, and reduced reliability. Alternatives include emerging devices such as NEMFETs [56] and graphene-based structures (GNRs) [57]. GNR logic gates have shown the potential for 100x lower power, 6x faster operation, and 100x smaller area than 7 nm FinFET CMOS [19, 57], opening avenues for low-power, high-speed McCulloch-Pitts neurons [58].

We focus on creating analog functions from GNR structures with digital inputs, implementing a GNR-based 5-bit DAC that provides programmable synaptic weights. By mapping GNR conductance via MATLAB and simulating in SPICE with a GNR Verilog-A model [59–61], we determined unit cell geometry, bias conditions, and derived a I_{ON}/I_{OFF} ratio of 24.3×. The resulting DAC achieves a DNL of -0.196 LSB to 0.088 LSB and an INL of -0.809 LSB to 0.364 LSB at only 0.2 V, meeting true 5-bit resolution.

3.2 Background

A thermometric DAC topology is chosen for its guaranteed monotonic output and superior DNL to that of binary-weighted approaches [62]. Figure 3.1 shows how a binary weight $B_0 ... B_{N-1}$ is converted into a thermometric code $D_0 ... D_{2^N-2}$, which switches $2^N - 1$ current sources on or off. Summing their currents yields the analog output I_{out}, accurately reflecting the synaptic weight value.

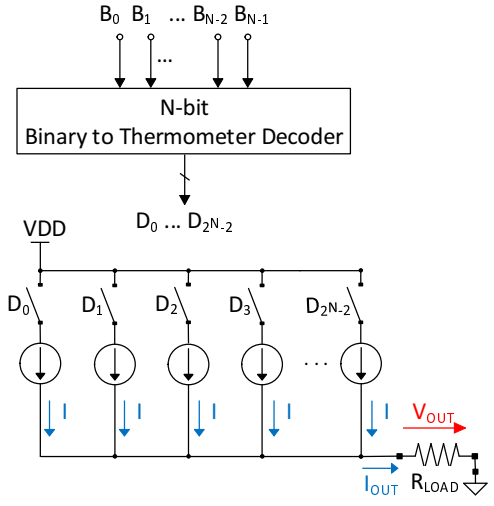


Fig. 3.1 DAC-based Programmable Synaptic Weight

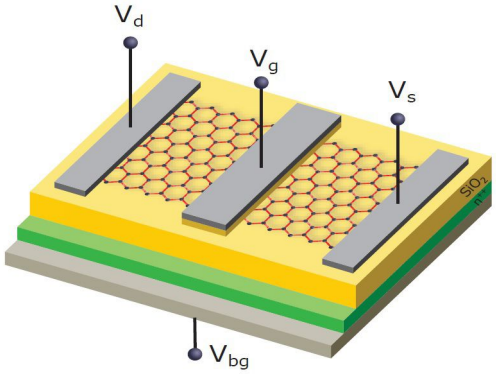


Fig. 3.2 GNR-based Fundamental Device [63]

We implement DAC-based programmable synaptic weights using the graphene device shown in Figure 3.2. This single-layer graphene nanoribbon (GNR) channel, biased

by V_{ds}, controls conductance via top and back gate voltages (V_g, V_{bg}) and geometry parameters, shown in Figure 3.3. These parameters include GNR total width W, length L, constriction width W_c and length L_c, bump width W_b and length L_b, top gate contact width $WV_{g1,2}$, and distances $PV_{g1,2}$ [2, 57].

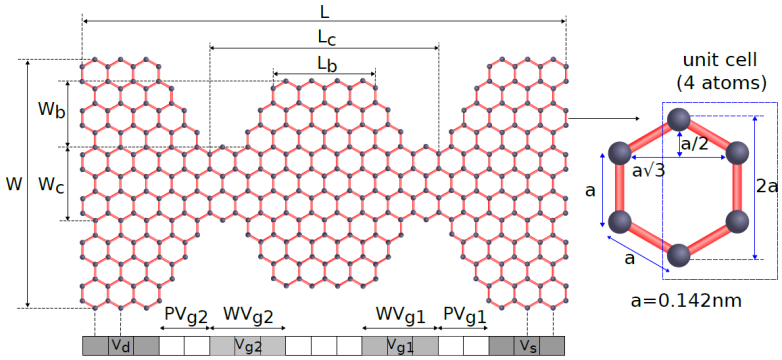


Fig. 3.3 GNR Geometry Description Parameters [57].

This fundamental GNR device has been proven capable of implementing a variety of functionalities, among which Boolean operations [57]. To perform a specific functionality, a GNR device instance that is specifically designed in terms of GNR geometry is employed [20].

3.3 GNR-based DAC for programmable synaptic weights

A thermometric current DAC requires $2^N - 1$ unit current cells plus a binary-to-thermometer decoder. While we do not implement the decoder here, GNR-based logic gates have been demonstrated [57], enabling a future GNR-based decoder. We focus on the GNR current cells, analogous to CMOS current sources, but relying on GNR properties rather than MOSFET square-law equations.

Key considerations include stable output current, high output resistance, and maximizing output voltage swing. We performed a design space exploration (DSE) of GNR geometry, contact configuration, and biasing to identify a device with the desired high output resistance and I_{ON}/I_{OFF} ratio.

Figure 3.4 shows the proposed GNR current source and its equivalent circuit. The device's drain connects to $V_{DD} = 0.2\,\text{V}$, and its source provides current I. Two top gates, tied together, control the 'ON'/'OFF' state, and the back gate is fixed at $V_{bg} = 0.3\,\text{V}$. After atomistic-level DSE, we chose the GNR geometry shown in Figure 3.4 c), with dimensions defined in multiples of the carbon atom spacing $a = 0.142\,\text{nm}$, ensuring high output resistance and suitable I_{ON}/I_{OFF} ratio.

Figure 3.5 a) shows the GNR's conductance map at $V_{DD} = 0.2\,\text{V}$, $V_{bg} = 0.3\,\text{V}$, and V_{g1}, V_{g2} ranging from $0\,\text{V}$ to $0.2\,\text{V}$. When $V_{g1} = V_{g2} = 0.2\,\text{V}$, the device is 'ON', exhibiting high conductance, and when $V_{g1} = V_{g2} = 0\,\text{V}$, it is 'OFF', exhibiting low conductance.

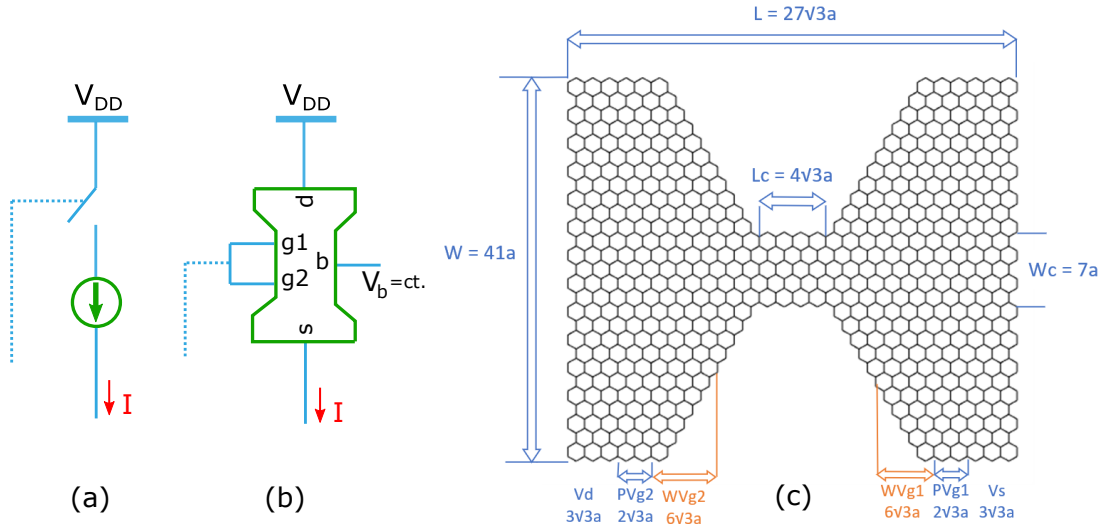


Fig. 3.4 Graphene-based Current Source Cell:
a) equivalent electrical circuit, b) GNR current source circuit, c) GNR geometry.

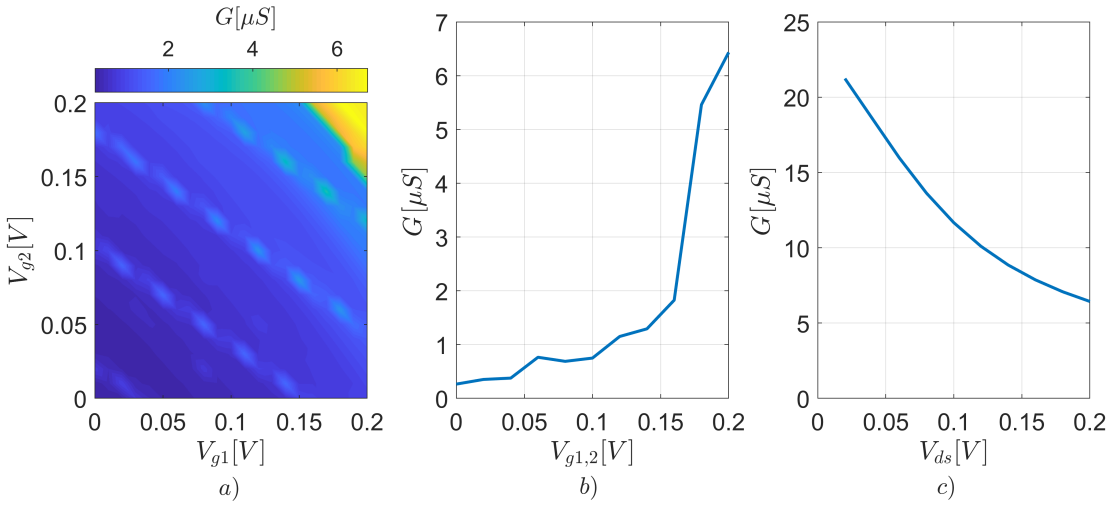


Fig. 3.5 Graphene Current Source Electrical Characteristics: a) Conductance Map,
b) Conductance Transfer Characteristic, c) Conductance Output Characteristic.

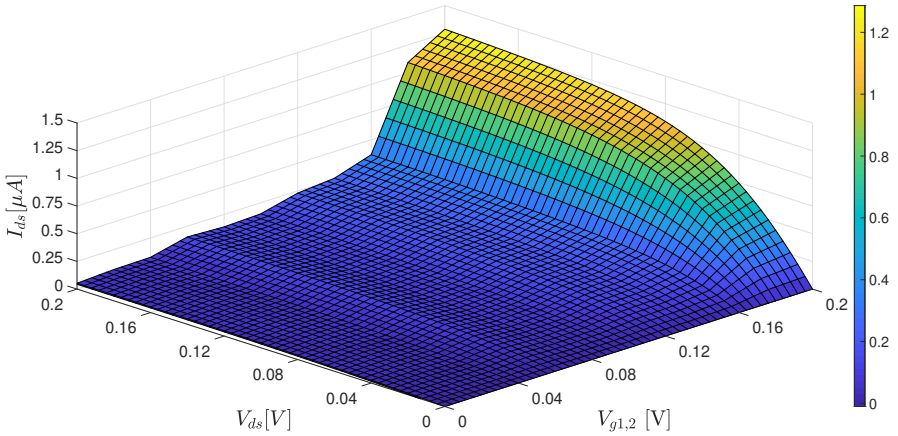


Fig. 3.6 GNR device I_{ds} current mapping as a function of V_{ds} and $V_{g1,2}$

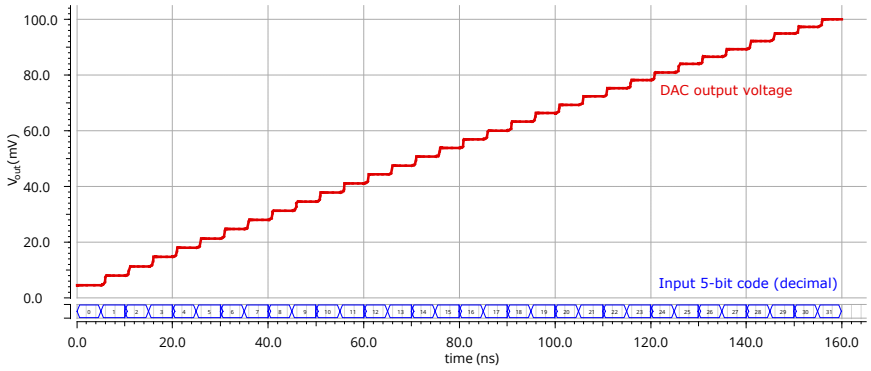


Fig. 3.7 5-bit GNR-based DAC Transfer Characteristic

Driving both gates with the same voltage achieves a 24.3× conductance variation between 0 V and 0.2 V, as shown in Figure 3.5 b). Sweeping V_{ds} from 0 V to 0.2 V, illustrated in Figure 3.5 c), shows that as V_{ds} increases, the GNR's conductance stabilizes near 6 µS, resembling the linear-to-saturation behavior of CMOS transistors.

Using this GNR device, we implemented a 5-bit DAC with 31 current cells driven by a GNR-based thermometric decoder, as shown in Figure 3.1. Operating at $V_{DD} = 0.2$ V, the DAC's output current flows through a $R_{LOAD} = 2.764$ kΩ resistor, generating the output voltage.

3.4 Simulation Results

3.4.1 GNR-based 5-bit DAC

When analyzing a DAC, the following aspects should be considered: (i) the resolution, which is evaluated using the INL and DNL, and (ii) the offset error. Figure 3.7 presents the relationship between the DAC's input code and analog output signal, i.e. the transfer characteristic.

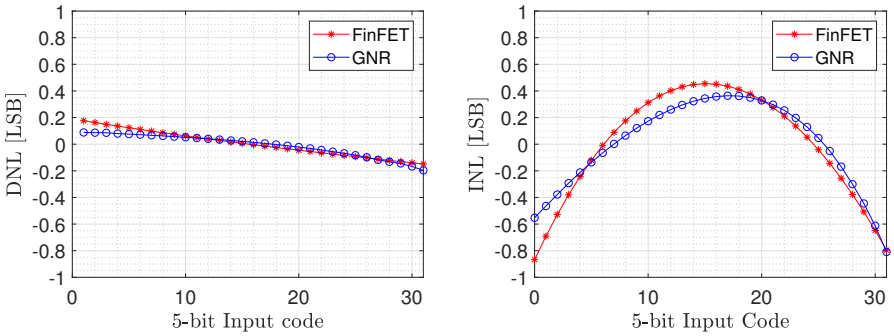


Fig. 3.8 DNL and INL plots for GNR versus FinFET comparison

The GNR DAC's resolution was assessed using DNL and INL derived from its transfer characteristic, shown in Figure 3.8, with an LSB of 3.10 mV determined from Figure 3.7. DNL ranged from -0.196 LSB to 0.088 LSB and INL from -0.809 LSB to 0.364 LSB, confirming monotonic behavior and true 5-bit resolution, as expected from a thermometric DAC [62].

3.4.2 GNR-based DAC versus 7 nm FinFET-based DAC

Comparing the GNR and FinFET 5-bit DAC implementations presented in Figure 3.8 and Table 3.1, both exhibit similar linearity. The FinFET design achieves DNL=-0.148 LSB to 0.176 LSB and INL=-0.796 LSB to 0.454 LSB with an offset of 0.11 mV, while the GNR DAC has slightly better INL variation. Under identical conditions, the GNR current source's I_{ds} varies 9 %, compared to 15 % for the FinFET, indicating higher GNR output resistance at ultra-low voltages.

Table 3.1 GNR DAC versus 7 nm FinFET DAC

	INL_{min} $[LSB]$	INL_{max} $[LSB]$	DNL_{min} $[LSB]$	INL_{max} $[LSB]$	Area $[nm^2]$
FinFET	-0.796	0.454	-0.148	0.176	3255
GNR	-0.809	0.364	-0.196	0.088	1199

3.5 Conclusions

By leveraging GNR-based devices, we implemented a 5-bit DAC for programmable synaptic weights in McCulloch-Pitts neurons, achieving ultra-low voltage operation (0.2 V) and a threefold reduction in active area compared to a FinFET variant. Using GNR unit current cells and a GNR logic thermometric decoder ensured a monotonic transfer function with 31 current sources, each mapped via MATLAB and simulated with a GNR Verilog-A model. This approach maintained comparable INL (-0.809 LSB to 0.364 LSB) and DNL (-0.196 LSB to 0.088 LSB) performance to the FinFET reference.

Chapter 4

Graphene Nanoribbons-Based McCulloch-Pitts Neural Network

In a rapidly advancing AI and ML landscape, we introduce a low-power, high-speed, mixed-signal GNR-based MCPN implementation with programmable synaptic weights and inhibitory inputs [64]. The MCPN comprises a weighted summation element and a decision element (soma). We employ three non-rectangular GNR devices as current source, low-side, and high-side switches, while programmable excitatory and inhibitory synapses use GNR SRAM cells and logic gates. The soma's threshold activation function is realized by a chain of GNR inverters with an adjustable threshold via a configurable resistive load. Benchmarking against a FinFET design for a 5x5 pixel pattern recognition task shows our GNR implementation uses 3.5$\times$ less power, is 20$\times$ faster, and occupies 3$\times$ less active area.

This chapter is based on the following original publications:

F. -S. Dumitru, M. Enachescu, A. M. Antonescu, N. Cucu-Laurenciu and S. D. Cotofana, "Graphene Nanoribbon Based McCulloch-Pitts Neural Network," 2024 IEEE 24th International Conference on Nanotechnology (NANO), Gijon, Spain, 2024, pp. 592-597, doi: 10.1109/NANO61778.2024.10628801.

4.1 Introduction

The McCulloch-Pitts neuron is a simple binary decision unit modeling a biological neuron. As shown in Equation 4.1, if the weighted sum of excitatory inputs x_i (with weights w_i) exceeds a threshold θ, the output is 1, otherwise 0.

$$f(x_1,\ldots,x_n) = \begin{cases} 1 & \text{if } \sum_{i=1}^{n} w_i \cdot x_i \geq \theta \\ 0 & \text{otherwise} \end{cases} \tag{4.1}$$

The complete McCulloch-Pitts neuron model expands Equation 4.1 by accounting for the existence of inhibitory inputs and is described in Equation 4.2, where $y_i = \{0,1\}$ represent the inhibitory inputs. We remark that triggering even a single of the inhibitory inputs will force the neuron's output to 0.

$$\tilde{f}(x_1,\ldots,x_n;y_1,\ldots,y_m) = f(x_1,\ldots,x_n) \cdot \prod_{j=1}^{m}(1-y_j) \tag{4.2}$$

4.2 GNR-based McCulloch-Pitts neural network

Each synapse in our MCPN can be excitatory with weight 0 or 1, or inhibitory, requiring two configuration bits. Configuration data is loaded into SRAM at power-on and updated as needed.

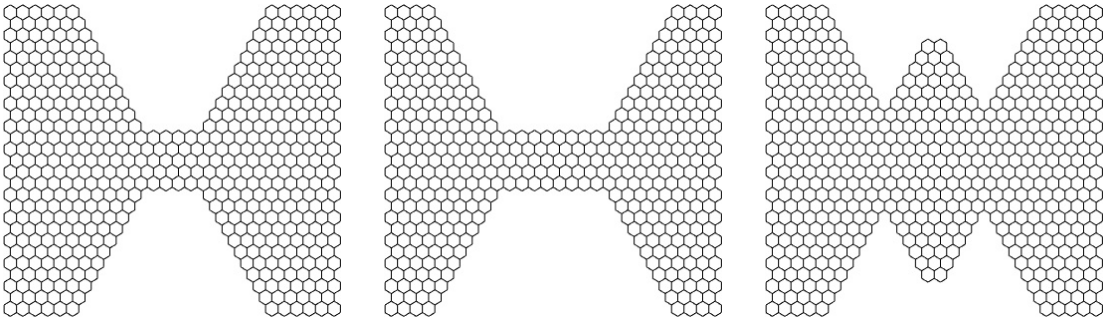
The GNR-based configurable synapse (green rectangle in Figure 4.4) includes three GNR devices: GNR_{DOWN} (low-side switch), GNR_{ISRC} (current source), and GNR_{UP} (high-side switch). Their geometries are detailed in Table 4.1 and illustrated in Figures 4.1b and 4.1c, with transfer and output characteristics shown in Figure 4.2.

GNR_{UP} functions like a PMOS switch, exhibiting high resistance when the gate is at VDD and low resistance at GND. It is controlled by a GNR-based 2-input NAND gate with inputs from the pixel's state and the synaptic weight stored in the GNR-based SRAM array. If both inputs are '1', GNR_{UP} closes.

Similarly, GNR_{DOWN} acts as an NMOS switch, showing high resistance at GND and low resistance at VDD. It is driven by a GNR-based 2-input AND gate with inputs from the pixel's state and the inhibitory bit in the GNR-based SRAM array. If both inputs are '1', GNR_{DOWN} closes.

4.2.1 GNR-based summation element

A simplified, one pixel row, representation of the proposed GNR-based summation element and its FinFET counterpart is illustrated in Figure 4.3. The nominal voltage of the devices in the GNR-based circuit translates into a VDD of 0.2 V, while in the FinFET circuit's case the VDD is 0.7 V.



(a) GNR_{ISRC} (b) GNR_{DOWN} (c) GNR_{UP}

Fig. 4.1 GNR-based neuron device topologies
a) GNR current source, b) GNR low-side switch , and c) GNR high-side switch

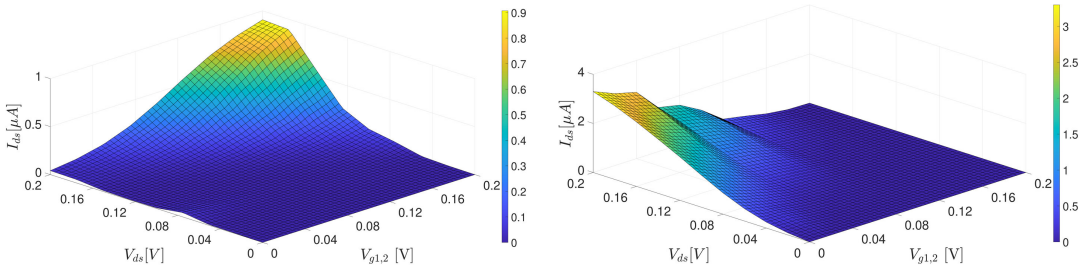


Fig. 4.2 3-D rendering combining transfer and output characteristics for GNR_{DOWN} (left) and GNR_{UP} (right) devices

In the GNR-based implementation, each pixel is managed by three analog devices and two logic gates, repeated five times to process a 5x5 pixel symbol with our analog neuron. In contrast, the FinFET counterpart from Figure 4.3b uses a similar setup but incorporates a diode-connected PMOS biased at a constant current to reference the current source PMOS devices.

The GNR_{ISRC} device acts as a current source when its gate is at VDD and switches to high resistance at GND (Figure 4.1a). To reduce leakage in the off state, a GNR_{UP} device is added in series. Unlike CMOS, the GNR_{ISRC} does not require a reference device and can be driven by logic gates or directly by VDD.

In the summation element, excitatory synapse currents pass through R_{LOAD} to set $SOMMA_{OUT}$. If any synapses are inhibitory and active, they shunt R_{LOAD}, preventing $SOMMA_{OUT}$ from exceeding the activation threshold. This analog approach leverages high-speed GNRs for fast MCPN responses, unlike other GNR-based spiking neurons that operate in milliseconds [65–67].

4.2.2 GNR-based activation function circuit

In our analog MCPN, illustrated in Figure 4.4b), a chain of inverters creates a step-function threshold activation, outputting 1 when the weighted sum exceeds θ and 0

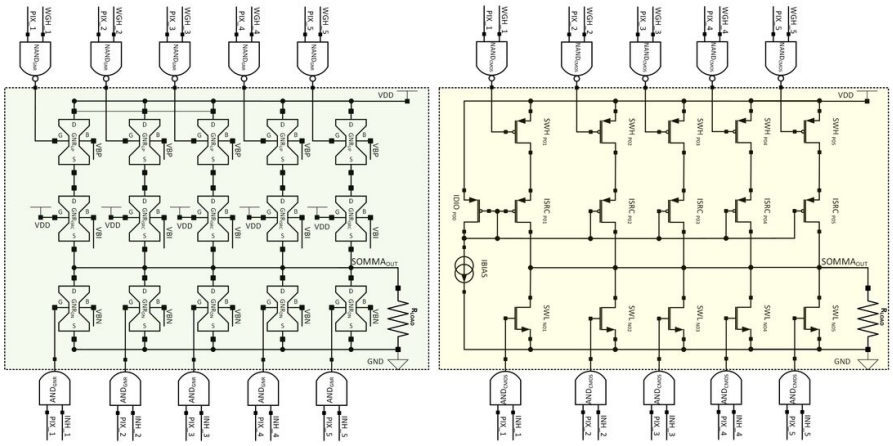


Fig. 4.3 Analog summation element implementation handling a single row of 5 pixels a) GNR (left) b) FinFET (right)

Table 4.1 Dimensions of GNR-based Neuron Structures

	(W,L)	(W_c,L_c)	(W_b, L_b)	(P_{V_G}, W_{V_G})
GNR_{ISRC}	$(41,27\sqrt{3})$	$(8,4\sqrt{3})$	$(0,0)$	$(2\sqrt{3},6\sqrt{3})$
GNR_{UP}	$(41,27\sqrt{3})$	$(14,8\sqrt{3})$	$(9,2\sqrt{3})$	$(12\sqrt{3},6\sqrt{3})$
GNR_{DOWN}	$(41,27\sqrt{3})$	$(8,8\sqrt{3})$	$(0,0)$	$(3\sqrt{3},6\sqrt{3})$

otherwise, with a 4 ps delay between input and output signals. To accommodate different numbers of active pixels, θ must be configurable. Instead of a fixed threshold, we adjust R_{LOAD} since $SOMMA_{OUT} = I_{TOT} \cdot R_{LOAD} = \theta$. This configurability is achieved by reusing the thermometric decoder from [55] with a resistor string, inserting GNR_{DOWN} switches between GND and each resistor node to linearly vary R_{LOAD}.

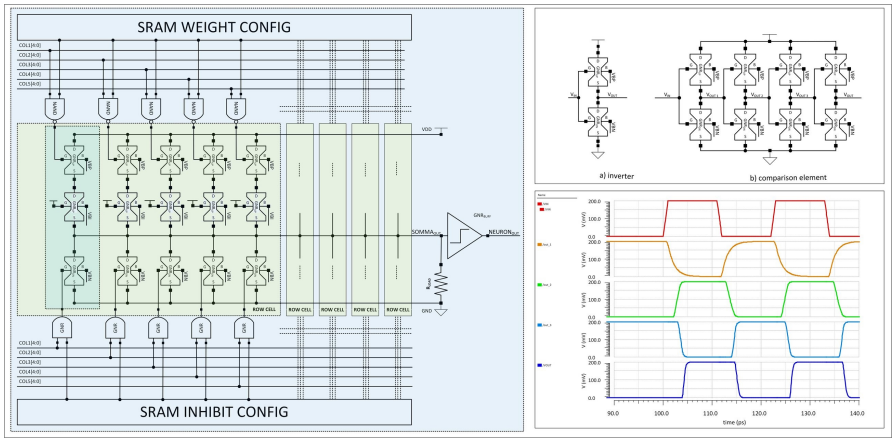


Fig. 4.4 GNR-based McCulloch-Pitts neuron

4.2.3 GNR-based neuron implementation

The GNR-MCPN implementation is illustrated in Figure 4.4. Each neuron consists of 25 synapses connected to the $SOMMA_{OUT}$ net and two SRAM cells (one for excitatory weights and one for inhibitory configurations), totaling 50 SRAM cells per neuron.

A neuron activates when enough excitatory synapses with a weight of 1 generate a total current I_{TOT} multiplied by R_{LOAD} that exceeds the threshold θ. Conversely, any active inhibitory synapse forces the neuron's output to zero.

While MCPNs are limited by having only binary inputs and weights, they are suitable for applications like black and white pattern detection. Implementing 5-bit synapse weights requires storing 1,550 bits for a single 25-synapse neuron. Additionally, each neuron uses 25 current source structures, compared to 31 in the 5-bit DAC from [55].

4.2.4 GNR-based neural network

The neural network used comprises a single fully-connected layer of five neurons, each independently configured to detect vowel patterns. While its simple topology limits recognition quality, it effectively showcases the GNR-MCPN's character recognition capabilities. This one-layer, fully-connected network with binary weights requires 250 SRAM bits for configuration.

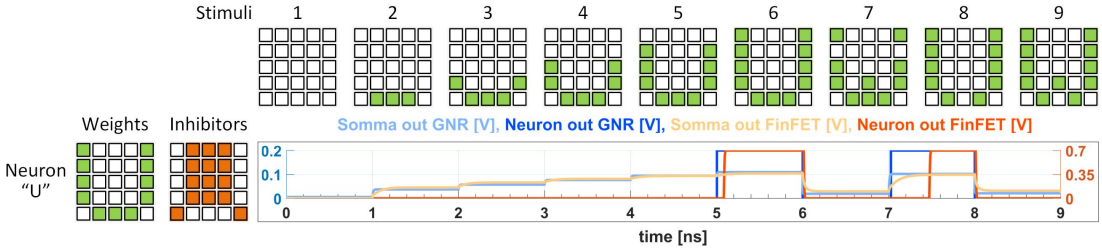


Fig. 4.5 Configuration, stimuli, and input waveforms for evaluation of vowel 'U'

4.3 Simulation results

To validate the GNR-MCPN, we simulated a neuron configured to detect the vowel 'U' (Figure 4.5). The neuron's configuration is shown on the left, with the *Weight* array representing excitatory inputs (green = 1, white = 0) and the *Inhibitors* array representing inhibitory inputs (orange = 1, white = 0). The network processes single-level, black and white pixels.

During the simulation, a 5x5 pixel input pattern undergoes nine phases (top of Figure 4.5). The summation element's analog output increases over the first seven patterns (traces $Somma_{out}GNR$ and $Somma_{out}FinFET$). At the sixth pattern, the threshold θ is exceeded, toggling $Neuron_{out}GNR$ and $Neuron_{out}FinFET$ high with 11 active pixels.

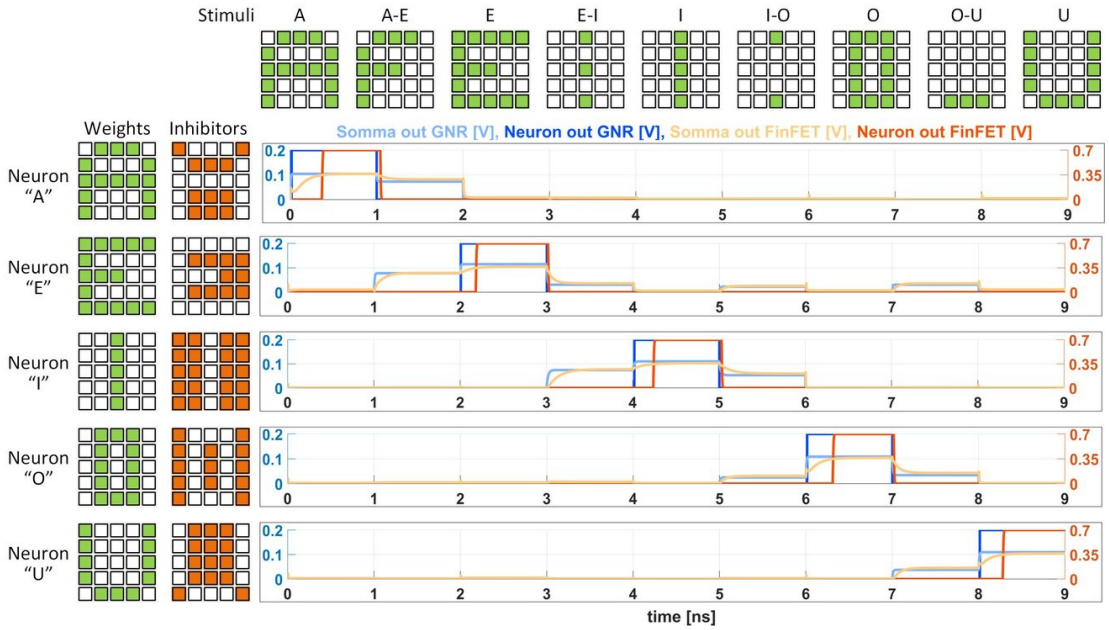


Fig. 4.6 Configuration, stimuli, and waveforms for evaluation of all vowels

Patterns seven and nine activate inhibitory pixels, reducing the summation output. The eighth pattern, with 10 active pixels, reaches the detection threshold. Thus, the 'U' threshold lies between 9 and 10 active pixels out of 11.

We validate the neural network by applying alternating vowels and intermediate symbols every 1 ns as shown in Figure 4.6. The GNR-based neuron toggles in 8 ps to 20 ps, approximately 20× faster than the FinFET's 140 ps to 360 ps. With equal bias currents, the GNR approach achieves 3.5× better power efficiency due to lower operating voltage. Additionally, the GNR design occupies about 3× less active area for the analog portion and 9× less for SRAM and control logic compared to FinFET.

4.4 Conclusions

In this chapter, we demonstrated a GNR-based MCPN delivering 3.5× lower power, 20× higher speed, and 3× less active area than the 7 nm FinFET analog equivalent in a neural network symbol recognition task, and 9× less area when considering SRAM and logic gates.

Chapter 5

Ultra-Low-Power Graphene-Nanoribbons-Based Current-Starved Ring Oscillator

Driven by the demand for ultra-low-power designs, graphene's properties—ballistic transport, flexibility, and bio-compatibility—make it ideal for nano-electronics. In [68], we investigated a GNR-based current-starved ring oscillator, leveraging GNRs' ultra-low voltage operation and attofarad-range intrinsic capacitances. Results show a 1.89× higher output frequency, 553.8× lower power consumption, and 812× improved power efficiency compared to conventional approaches.

This chapter is based on the following original publications:

F. -S. Dumitru, M. Enachescu, A. Antonescu, N. Cucu-Laurenciu, and S. Cotofana, "Ultra-Low-Power Graphene-Nanoribbons-Based Current-Starved Ring Oscillator," 2024 International Semiconductor Conference (CAS), Sinaia, Romania, 2024, pp. 167-170, doi: 10.1109/CAS62834.2024.10736700

5.1 Introduction

In a basic ring oscillator, the frequency f is determined by the number of stages N and the propagation delay per stage t_d (Equation 5.1). Additionally, the power consumption can be estimated using the inverter's load capacitance C_L, activity factor α, and supply voltage V_{supply} (Equation 5.2).

$$f = \frac{1}{2 \cdot N \cdot t_d} \tag{5.1}$$

$$P = \alpha \cdot N \cdot C_L \cdot V_{supply}^2 \cdot f \tag{5.2}$$

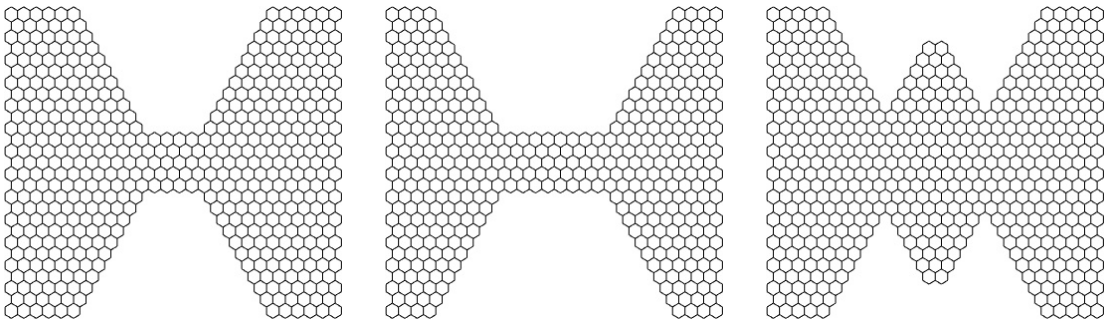
The main drawback of this implementation is the variability induced by t_d into the oscillation frequency, which will vary linearly with V_{supply} and non-linearly through drain currents I_{PMOS} and I_{NMOS} against process, temperature and V_{supply} variations, as shown in Equation 5.3.

$$t_d \approx \ln(2) \cdot \frac{C_L \cdot V_{supply}}{2} \cdot \left(\frac{1}{I_{PMOS} + I_{NMOS}} \right) \tag{5.3}$$

Propagation time variability is reduced using the current starving technique, which enforces a maximum current I_{bias} through inverter transistors with a series current source (Equation 5.4), while power consumption is still calculated using Equation 5.2.

$$f = \frac{I_{bias}}{2 \cdot N \cdot C_L \cdot V_{supply}} \tag{5.4}$$

A set of three GNR geometries, capable of fulfilling the roles of current source and low-side and high-side switches [64] is illustrated in Figure 5.1. The exact structure geometries, identified through iterative conductance map plot evaluations [57], are detailed in Table 5.1.



(a) GNR_{ISRC} (b) GNR_{DOWN} (c) GNR_{UP}

Fig. 5.1 GNR-based ring oscillator device topologies [64]
a) GNR current source, b) GNR low-side switch , and c) GNR high-side switch

Table 5.1 Dimensions of GNR structures for ULP GNR-based ring oscillator [64]

	(W,L)	(W_c,L_c)	(W_b, L_b)	(P_{V_G}, W_{V_G})
GNR_{ISRC}	$(41,27\sqrt{3})$	$(8,4\sqrt{3})$	$(0,0)$	$(2\sqrt{3},6\sqrt{3})$
GNR_{UP}	$(41,27\sqrt{3})$	$(14,8\sqrt{3})$	$(9,2\sqrt{3})$	$(12\sqrt{3},6\sqrt{3})$
GNR_{DOWN}	$(41,27\sqrt{3})$	$(8,8\sqrt{3})$	$(0,0)$	$(3\sqrt{3},6\sqrt{3})$

5.2 Designing a GNR current-starved ring oscillator

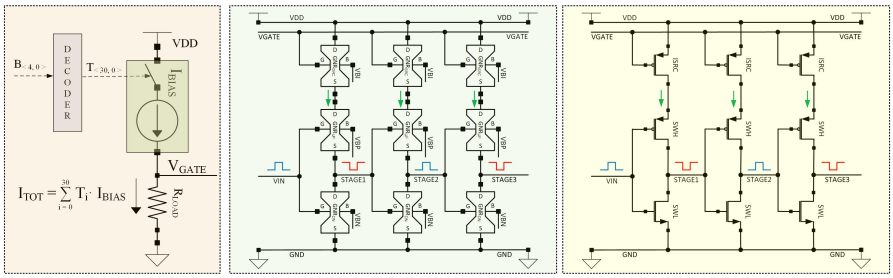


Fig. 5.2 a) 5-bit DAC (left) for frequency tuning b) GNR-based (middle) and FinFET (right) ring oscillator sections

The ring oscillator stages using GNR devices and FinFETs with a 5-bit DAC for frequency tuning are shown in Figure 5.2. The DAC is essential because GNRs lack a 180° phase-shift at low frequencies, preventing the use of traditional current mirrors. Instead, we modulate the GNR current by driving its gate with the DAC output [55].

The complete implementation of the GNR-based current-starved ring oscillator is shown in Figure 5.3 and is comprised of 8 inverter-like stages. The last 180° phase shift is ensured by a GNR NAND gate which constitutes the circuit's enable. The oscillator's frequency can be modulated by adjusting the current DAC input code, which, in turn, regulates the gate voltage of the current source device.

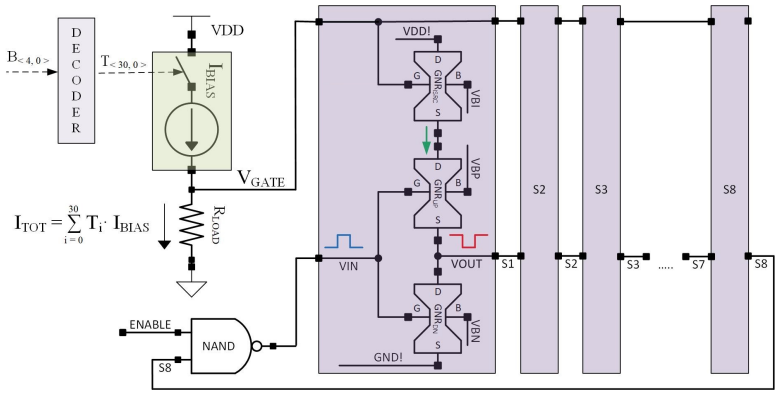
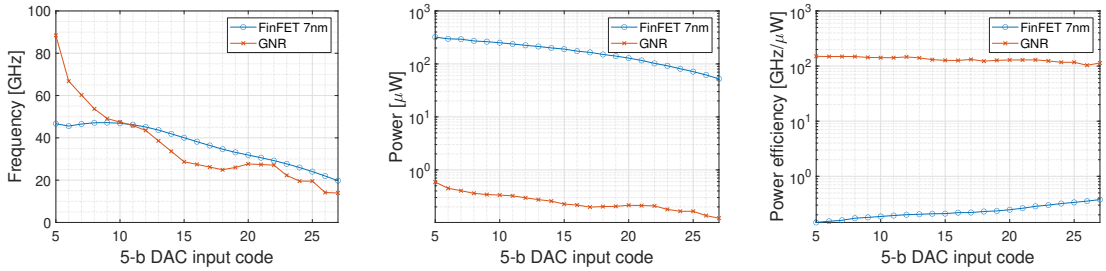


Fig. 5.3 Simplified GNR-based current-starved ring oscillator schematic

5.3 Results

Figure 5.4 presents the comparison of frequency range, power consumption, and power efficiency for both oscillators across different DAC input codes.



(a) *Frequency* (b) *Power* (c) *Power efficiency*

Fig. 5.4 Performance comparison of GNR-based and 7 nm FinFET ring oscillators: a) frequency, b) power, c) power efficiency

We limited the DAC input code range to keep the FinFET PMOS out of the linear and cut-off regions, ensuring effective current starving. Table 5.2 shows that the GNR-based and 7 nm FinFET ring oscillators have similar frequencies, primarily due to the GNR's low 1.2 µA current. However, the GNR oscillator achieves nearly three orders of magnitude lower power consumption and three orders of magnitude higher power efficiency than the FinFET version, thanks to smaller parasitic capacitances, despite comparable frequencies.

Table 5.2 GNR-based versus FinFET ring oscillator results

	Frequency [GHz]	Power consumption [µW]	Power efficiency [GHz/µW]
FinFET	19.7 - 46.7	52.2 - 321.2	0.14 - 0.40
GNR	13.9 - 88.4	0.12 - 0.58	113.7 - 150.4

5.4 Conclusion

We explored using graphene nanoribbons (GNRs) to create high-frequency, ultra-low-power internal oscillators for multi-technology ICs. By tuning the oscillator frequency through the gate of the GNR-based current source and applying the current starving technique to the ring oscillator topology, we significantly reduced dynamic power consumption. Compared to a 7 nm FinFET implementation, the GNR-based design achieved a 1.89× higher output frequency, reduced power consumption by 553.8×, and improved power efficiency by 812×.

Chapter 6

The Impact of Segmentation on Current-Steering DAC Performance

This chapter presents findings from [69, 70] on the impact of segmentation on differential non-linearity (DNL) and integral non-linearity (INL) in a 10-bit differential current-steering DAC, fabricated using a 40 nm, 2.5 V CMOS process. By simulating all segmentation levels between binary and thermometer implementations, we achieved DNL improvements from -0.467 LSB to 0.474 LSB down to -0.024 LSB to 0.026 LSB, while INL remained nearly constant at -0.376 LSB to 0.345 LSB. The DAC delivered a differential output current of ± 1 mA within an active analog area of 0.01 mm^2. All decoder variants necessary for driving the DAC's analog components were physically implemented, with their areas documented in Table 6.5. Additionally, theoretical DNL and INL results were validated against Monte Carlo simulations, maintaining accuracy within a 30 % margin of error across all 10-bit segmented DAC architectures.

This chapter is based on the following original publications:

F. -S. Dumitru, C. R. Ilie, M. Bodea, and M. Enachescu, "Exploring the effect of segmentation on a 10-bit DAC," Romanian Journal of Information Science and Technology, vol. 24, no. 2, pp. 129-142, 2021.

F. -S. Dumitru, C. R. Ilie and M. Enachescu, "Exploring the Effect of Segmentation on INL and DNL for a 10-bit DAC," 2020 International Semiconductor Conference (CAS), Sinaia, Romania, 2020, pp. 161-164, doi: 10.1109/CAS50358.2020.9268011.

6.1 Introduction

To efficiently estimate DNL and integral non-linearity (INL) without extensive Monte Carlo simulations, especially for fully thermometric converters, we utilize a unit current source variation-based method [71]. In [72], we explored all segmentation combinations for a 10-bit DAC. This chapter extends that work by: (i) detailing the area occupied by each decoder variant to understand the DNL vs. die area trade-off, (ii) presenting DNL and INL plots for all 10 DAC variants, and (iii) determining the RMS DNL and INL to evaluate the accuracy of the unit current source mismatch method. Our analysis showed relative errors of $-30.70\,\%$ to $-11.55\,\%$ for DNL and $-29.57\,\%$ to $-17.43\,\%$ for INL.

6.2 DAC Architectures and Characteristics

6.2.1 Binary-Weighted Architecture

In a binary-weighted DAC, the output current sums binary-weighted sources scaling the unit current I_U (Equation 6.1), with D_1 as the LSB and D_N as the MSB. These DACs face two main issues: (i) stringent matching requirements for monotonicity and (ii) significant glitch impulses when toggling many unit cells (MSBs) [73]. Although Gray code implementations are possible [74], they still rely on binary-weighted sources, leading to poor DNL performance.

$$I_{out} = \sum_{i=1}^{N} 2^{i-1} \cdot I_u \cdot D_i \tag{6.1}$$

6.2.2 Segmented Architectures

Segmentation addresses the drawbacks of binary-weighted DACs while using the same number of unit current cells. This method minimizes major carrier transition jumps by activating an additional thermometer cell and keeping previous sources on, rather than deactivating groups of current sources. Typically, 4 to 7 thermometer bits are used [75–77] to balance DNL performance and routing congestion. The optimal number depends on current source sizing and the technology node. Figure 6.1 illustrates a partially segmented DAC with 4 MSBs translated into thermometer codes. Table 6.1 details the number and weights of current sources for each DAC architecture. The naming convention in this chapter denotes the number of binary-weighted bits (B) followed by the number of thermometer bits (T) for each DAC implementation.

Summing up the number of cells used in any of the implementations below, these will add up to 1023 unit current cells (00B10T), therefore the active analog area is invariant of the degree of segmentation chosen.

Table 6.1 Current sources distributions with respect to various DAC architectures

DAC \ I_{SRC}	1x	2x	4x	8x	16x	32x	64x	128x	256x	512x
$10B00T$ $(binary)$	1	1	1	1	1	1	1	1	1	1
$08B02T$ $(hybrid)$	1	1	1	1	1	1	1	1	3	0
$07B03T$ $(hybrid)$	1	1	1	1	1	1	1	7	0	0
$06B04T$ $(hybrid)$	1	1	1	1	1	1	15	0	0	0
$05B05T$ $(hybrid)$	1	1	1	1	1	31	0	0	0	0
$04B06T$ $(hybrid)$	1	1	1	1	64	0	0	0	0	0
$03B07T$ $(hybrid)$	1	1	0	127	0	0	0	0	0	0
$02B08T$ $(hybrid)$	1	1	255	0	0	0	0	0	0	0
$01B09T$ $(hybrid)$	1	511	0	0	0	0	0	0	0	0
$00B10T$ $(unary)$	1023	0	0	0	0	0	0	0	0	0

6.2.3 Segmentation's Effect on DNL and INL

The degree of segmentation significantly influences DNL, as segmented architectures partly inherit the monotonicity inherent to thermometer DACs [73]. However, INL remains unaffected by segmentation [78] because it arises from random mismatches across all current sources, regardless of their arrangement or decoding strategy.

According to [78], Table 6.2 outlines the standard deviation equations for DNL and INL in binary, thermometer, and partially segmented DAC architectures. Here, σ_ε represents the unit current source's standard deviation in LSBs, B_1 the number of binary bits, and B the DAC's resolution. We further evaluate the accuracy of these formulas within deep submicron technologies.

Table 6.2 DNL, INL standard deviation equations for different DAC architectures

	Binary-weighted	Fully thermometer	Partially segmented
σ_{DNL}	$2^{\frac{B}{2}} \times \sigma_\varepsilon$	σ_ε	$2^{\frac{B_1+1}{2}} \times \sigma_\varepsilon$
σ_{INL}	$2^{\frac{B}{2}-1} \times \sigma_\varepsilon$	$2^{\frac{B}{2}-1} \times \sigma_\varepsilon$	$2^{\frac{B}{2}-1} \times \sigma_\varepsilon$

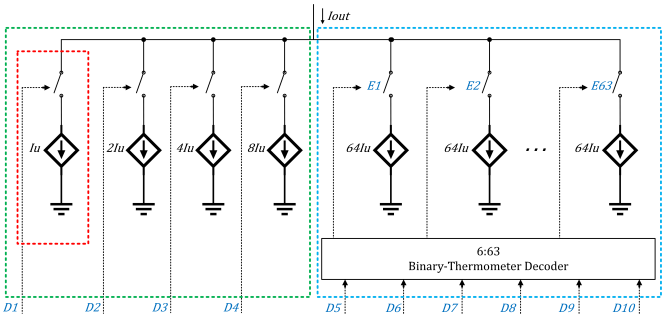


Fig. 6.1 Partially segmented architecture:
04B06T unit current cell (red), binary-weighted cells (green), segmented cells (blue)

6.3 10-bit Current Steering DAC Variants

6.3.1 Analog current source array implementation

To validate the formulas in Table 6.2 for 10-bit DACs in deep submicron technologies, we explored all segmented topologies from Table 6.1. For each segmentation case, we implemented both the analog current source array and the corresponding digital controller to evaluate their performance.

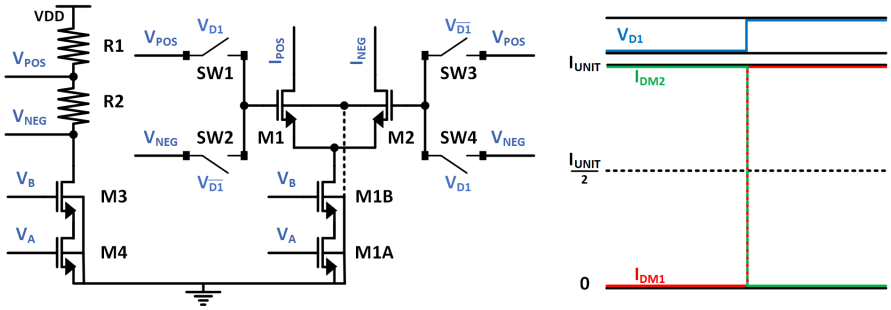


Fig. 6.2 Unit current source cell

To manage unit current source mismatch, which affects DAC INL and DNL performance, designers can adjust the device area and saturation voltage. The standard deviation of the output current, σ_ε, is proportional to $(W \cdot L)^{-1/2}$ and $(V_{GS} - V_{TH})^{-1}$ for the current source device M_{1A} (Figure 6.2), as shown in Equation 6.2.

$$\left(\frac{\sigma_\varepsilon}{I_u}\right)^2 = \frac{4 \cdot A_{VTH}^2}{W \cdot L \cdot (V_{GS} - V_{TH})^2}, \tag{6.2}$$

where A_{VTH} is a technological constant.

Segmentation significantly improves DNL by preserving the monotonicity of thermometer DACs in the segmented portion [73]. However, INL remains unaffected as it arises from random mismatches across all current sources, independent of their arrangement [78]. Table 6.2 outlines the standard deviation equations for DNL and INL in binary, thermometer, and partially segmented DAC architectures, where σ_ε is the unit

current source's standard deviation in LSBs, B_1 the number of binary bits, and B the DAC resolution. We further assess the validity of these formulas in deep submicron technologies.

Table 6.3 Unit current cell transistor dimensions

Device	Width [µm]	Length [µm]
M_1, M_2, M_{1B}, M_3	0.8	0.6
M_{1A}, M_4	0.8	10

To explain the unit current cell in Figure 6.2 and its role in the DAC, note the differential input stage with M_1 and M_2 that steers the tail current through either the left or right branch. The unit cell outputs, I_{POS} and I_{NEG}, are summed across the current source array to produce the DAC output currents. When D_1 is high, SW_1 and SW_4 close, directing the tail current through M_1; similarly, when D_1 is low, SW_2 and SW_3 close.

To enhance the DAC's dynamic behavior beyond the classic design [71], we implemented a moderate-swing technique [79], as shown in Figure 6.2. Here, the differential voltage V_{DIFF} between M_1 and M_2 equals the voltage drop across resistor R_2. We selected $V_{DIFF} = 500\,\text{mV}$ to minimize current source perturbation during switching and ensure the non-conducting device remains firmly in cut-off, preventing leakage currents.

The analog area for the current source array with 1023 unit cells is approximately 0.01 mm^2. Implemented in a 40 nm process, this design reduces die area by one order of magnitude compared to 180 nm [4] and 350 nm [5] designs, as detailed in Table 6.4.

Table 6.4 Analog area comparison

	[80]	[71]	This work
Technology [nm]	180	350	40
Area [mm^2]	0.35	0.6	0.01

6.3.2 Digital decoder physical implementation

The Binary-to-Thermometer (B2T) Decoder for the analog array's thermometer-coded section, shown in Figure 6.1, was implemented for binary bit lengths from 1 to 10 using RTL hardware description language. Input and output buffers ensured consistent loading conditions across all decoders.

All ten decoder variants were synthesized using a commercial 40 nm process standard cell library with diverse logic gates via Cadence Genus Synthesis Solution [81], targeting minimum area without latency constraints. The synthesized design areas are presented in Table 6.5.

For designs with fewer than 7 bits, the interconnect area is comparable to the logic gates area. However, for bit lengths of 7 and above, the standard cell area becomes dominant, reaching up to 68.5 % for the 10-bit fully-thermometer decoder. This demonstrates that decoders with 7 bits or more experience an exponential area increase due to rising complexity.

Table 6.5 Decoder area comparison

	Area [μm^2] post synthesis	Final area [μm^2] post place and route
0b	N/A	N/A
2b	6.2	-
3b	19.4	-
4b	46.2	-
5b	271	-
6b	518	452
7b	1020	981
8b	2711	2431
9b	6659	6122
10b	13616	14004

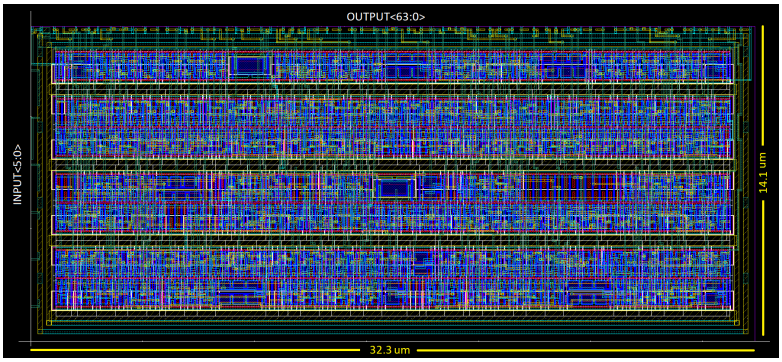


Fig. 6.3 6-bit Binary to Thermometer Decoder physical implementation

Area results indicated in Table 6.5 reveal a 4 % to 13 % area reduction for the 6-bit, 7-bit, 8-bit, and 9-bit B2T decoders implementations when compared to the post-synthesis results, while for the more interconnect congested 10-bit B2T decoder, a 3 % area increase is observed when compared to the post-synthesis results.

6.4 Simulation results

To simplify analysis, we use root mean square (RMS) characteristics to aggregate DNL and INL from all runs, enabling comparison of DNL improvements and INL stability. The RMS DNL and INL for the 10 implementations are displayed in Figures 6.4 and 6.5, respectively.

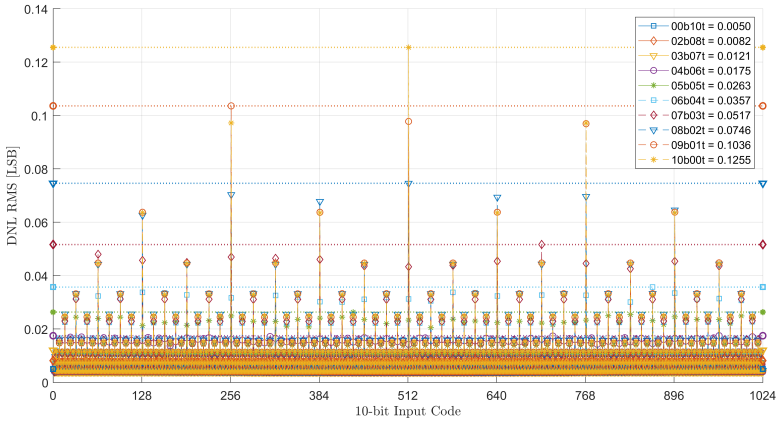


Fig. 6.4 Root mean square DNL versus segmentation

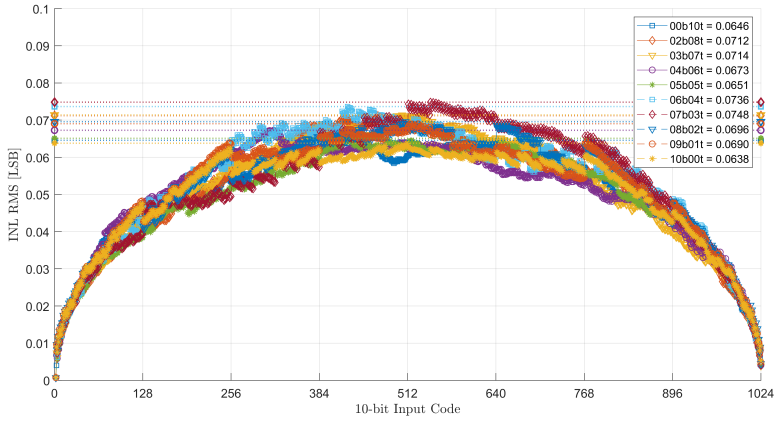


Fig. 6.5 Root mean square INL versus segmentation

The purely binary DAC (10B00T) exhibits a maximum RMS DNL of 125 mLSB, whereas the purely thermometer DAC (00B10T) achieves a much lower DNL of 5 mLSB. DNL improves consistently with increased segmentation, positioning segmented DACs between the binary and thermometer extremes.

The maximum RMS INL for the binary variant (10B00T) is 63.8 mLSB, and for the thermometer variant (00B10T) it is 64.6 mLSB. All 10 variants display similar INL results, with minor variations due to the finite number of simulation runs.

To streamline analysis, RMS DNL and INL are aggregated and shown in Figures 6.4 and 6.5. Theoretical and simulated standard deviations for DNL and INL, based on segmentation levels, are compared in Table 6.6, demonstrating a relative error within 30 %.

Table 6.6 Computed and simulated σ_{DNL} and σ_{INL}

No. Thermo. Bits	Computed σ_{DNL} [n]	Simulated σ_{DNL} [n]	Relative DNL error	Computed σ_{INL} [n]	Simulated σ_{INL} [n]	Relative INL error
0	181.12	125.5	−30.70	90.59	63.8	−29.57
2	128.08	103.6	−19.10	90.59	69.0	−23.83
3	90.56	74.6	−17.62	90.59	69.6	−23.17
4	64.03	51.7	−19.25	90.59	74.8	−17.43
5	45.28	35.7	−21.15	90.59	73.6	−18.75
6	32.01	26.3	−17.83	90.59	65.1	−28.13
7	22.64	17.5	−22.70	90.59	67.3	−25.70
8	16.01	12.1	−24.42	90.59	71.4	−21.18
9	11.32	8.2	−27.56	90.59	71.2	−21.40
10	5.66	5.0	−11.66	90.59	64.6	−28.68

Table 6.2 shows that theoretical formulas overestimate the DNL and INL standard deviations, with relative errors between −30.70 % to −11.55 % for DNL and −29.57 % to −17.43 % for INL. This approach allows predicting DAC DNL and INL based on a single unit current source, significantly reducing simulation time compared to sweeping all 2^n input codes, especially for segmented DACs.

6.5 Conclusions

We investigated the impact of segmentation on the DNL and INL of a 10-bit DAC by implementing all intermediate segmentation architectures. Simulation results, including DNL standard deviations, showed significant improvements in DNL while keeping INL approximately unchanged. Physical implementations of each DAC variant documented die area, and theoretical DNL and INL results remained within a 30 % margin of error compared to Monte Carlo simulations for all segmented 10-bit DAC architectures.

Chapter 7

The Impact of Non-Idealities on ΣΔ ADC Performance

This chapter examines discrete-time ΣΔ ADCs from [82], focusing on how non-ideal op-amp slew rate and gain affect a 16-bit, 1 kHz, differential, second-order, 1-bit sigma-delta modulator implemented in 180 nm technology. We analyze these parameters, which act as fully-differential, discrete-time integrators, and use SPICE simulations to validate the MATLAB results for each scenario.

This chapter is based on the following original publications:

F. -S. Dumitru, S. Mihalache and M. Enachescu, "OPAMP's finite gain and slew rate impact on a 16-bit ΣΔ ADC performance: A case study," 2017 International Semiconductor Conference (CAS), Sinaia, Romania, 2017, pp. 161-164, doi: 10.1109/SMICND.2017.8101187.

7.1 Introduction

The ΣΔ ADC is now the leading high-resolution ADC, easily surpassing the 12–14-bit range where other topologies fail [83, 84]. Beyond this resolution, architectures like SAR encounter challenging device matching requirements. Solutions such as expensive laser trimming reduce manufacturer profits and increase costs for users.

ΣΔ ADCs achieve high resolutions by minimizing the sensitive analog circuitry required for conversion. This chapter focuses on the analog specifications needed for op-amps to ensure proper modulator operation.

7.2 Design considerations of the ΣΔ modulator

Figure 7.1 depicts the system-level schematic of the ΣΔ modulator. It includes a non-ideal sampling and hold (S/H) circuit with a sampling switch and capacitor, introducing KT/C noise. The modulator utilizes two op-amps, where the first op-amp's performance is critical and its noise is modeled using a white noise source. Additionally, a relay functions as the quantizer, producing the pulse density modulated output signal. All other components are ideal auxiliaries necessary for the simulation.

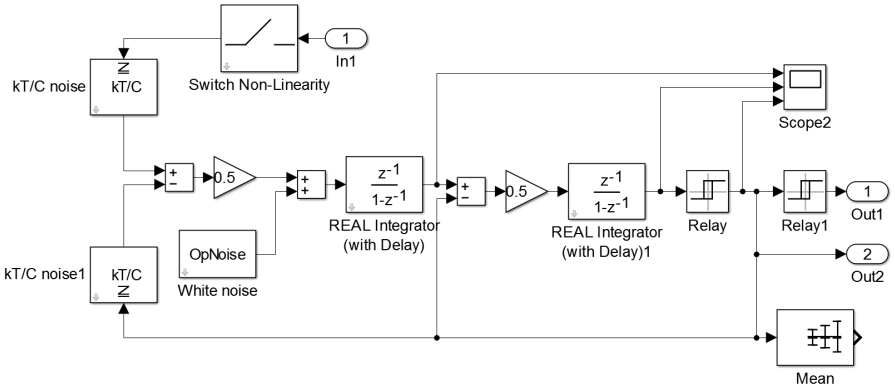


Fig. 7.1 Matlab Simulink second-order ΣΔ modulator

The influence of finite DC gain on the ΣΔ modulator, G, can be investigated by writing the equations of the Figure 7.2 integrator's transfer function for the case of an amplifier with finite gain.

$$H(z)_{ideal} = \frac{C_s}{C_i} \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{7.1}$$

$$H(z)_{finitegain} = \frac{C_s}{C_i} \cdot \frac{\left(\frac{a}{1+a+\frac{C_s}{C_i}}\right) \cdot z^{-1}}{\left(\frac{1+a}{1+a+\frac{C_s}{C_i}}\right) \cdot z^{-1}} \tag{7.2}$$

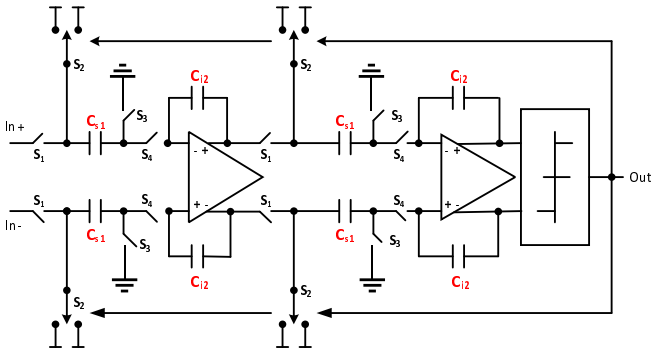


Fig. 7.2 ΣΔ Modulator top-level schematic

where C_s represents the value of the sampling capacitor and C_i the value of the capacitor on the integrator's feedback loop.

$$\frac{D_{out}}{e_Q} = \frac{1}{1+H(\omega)} \tag{7.3}$$

$$\frac{D_{out}}{e_Q} = \frac{1}{\infty} = 0 \quad for \quad G_{DC} = \infty$$

$$\frac{D_{out}}{e_Q} \approx \frac{1}{a} \quad for \quad G_{DC} = a$$

Designing an integrator with low DC gain increases in-band quantization noise. When the amplifier gain, G, exceeds the oversampling ratio (OSR), variations in G have minimal impact on the SNR. Conversely, if G is below the OSR, significant SNR degradation occurs with gain fluctuations. Therefore, it is best practice to maintain G well above the OSR, especially for ratios below 512×, as achieving such gains is relatively straightforward.

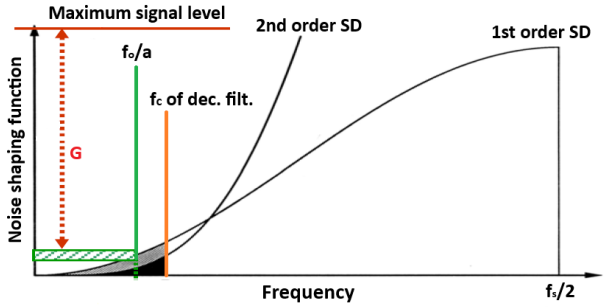


Fig. 7.3 Noise shaping function versus frequency for gain G < OSR

Figure 7.3 illustrates the impact of an integrator op-amp gain below the OSR. When gain G falls below the oversampling ratio, the noise floor sharply increases, degrading the modulator's SNR. Conversely, each doubling of G above the OSR results in only a modest 1 dB SNR improvement [85].

We assume our integrators use finite bandwidth op-amps that do not enter slew rate conditions, characterized by a first-order response and exponential settling [86].

Switched capacitor ΣΔ modulators benefit from relaxed op-amp requirements [87], needing only complete settling before comparator triggering. In contrast, continuous-time ΣΔ modulators must maintain linear behavior continuously, which is challenging.

By contrast, an additional delay appears corresponding to the slewing condition, and it is proportional to the difference of amplitude between the received samples the time constant becoming that given in Equation 7.4.

$$\tau = \frac{1}{2} \cdot f_s + t_{slew} \tag{7.4}$$

Therefore, the slew rate causes the settling time to increase, and, as a consequence, the analog outputs of the integrators are unable to achieve complete settling. Furthermore, the incomplete settling translates into a rapid degradation of the modulator's SNR, as quantization noise increases [85].

A limited slew rate extends settling time, preventing complete settling of integrator outputs and rapidly degrading the modulator's SNR due to increased quantization noise [85].

$$SR_{MIN} = 1.2 \times \Delta \times f_s \tag{7.5}$$

Compared to the analog requirements for op-amps in continuous-time ΣΔ or other Nyquist-rate ADC architectures, these requirements are relatively easy to meet.

We preliminarily conclude that ΣΔ converters have relaxed analog circuit demands.

However, failing to satisfy these demands will cause rapid performance degradation, as detailed in Section 7.2.

7.3 Simulation methodology and results

In this section, we compare the proposed ΣΔ modulator designed disregarding the minimum op-amp requirements with a version that satisfies the minimum specs.

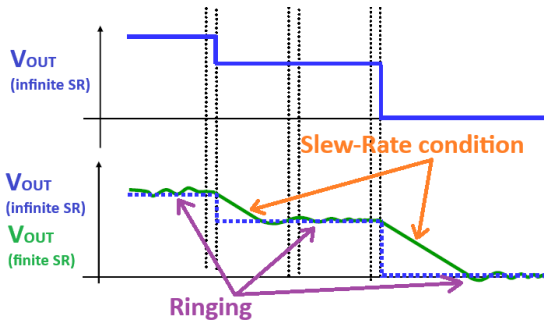


Fig. 7.4 Output of the integrator during slew rate condition

We examined a 16-bit, 1 kHz, differential, second-order discrete-time ΣΔ modulator using MATLAB Simulink for high-level simulations of its analog circuitry design space. For detailed analysis of slew rate and finite gain, the modulator was developed in Cadence Virtuoso with the 180 nm GPDK [88] technology. Cadence Spectre simulations validated the MATLAB results for each scenario. All simulations were conducted under typical corner conditions, using a 3.3 V supply and an ambient temperature of 27 °C.

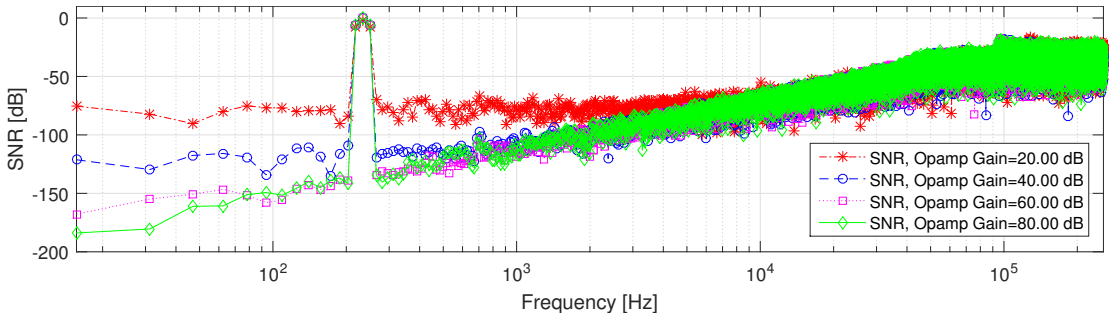


Fig. 7.5 Simulated SNR for different op-amp finite gains

Figure 7.5 presents simulation results for varying op-amp gains in a 16-bit, 1 kHz, differential, second-order, 1-bit ΣΔ modulator implemented in 180 nm technology. When the gain G exceeds the OSR of 256×, its impact on the modulator's SNR is minimal, with results around -180 dB at DC. Increasing G slightly lowers the SNR noise floor, but in practical modulators, op-amp noise would have a more significant effect.

Conversely, when G is below the OSR, the modulator's SNR is markedly affected. For instance, at $G = 20$ dB, the 3rd harmonic is -66 dB and the noise floor is -80 dB, compared to $G = 40$ dB with $G = -97$ dB harmonics and a -120 dB noise floor. Higher gains $G = 60dB$ and $G = 80dB$ further reduce harmonics to -102 dB and -104 dB and lower the noise floor below -160 dB.

These results confirm that when the op-amp gain falls below the critical value set by the OSR, ADC performance degrades significantly, reducing the modulator's ENOB from 16-bit to 10-bit. To ensure optimal performance, maintaining the op-amp's gain at least 10 dB above the OSR is recommended, as outlined in Table 7.3.

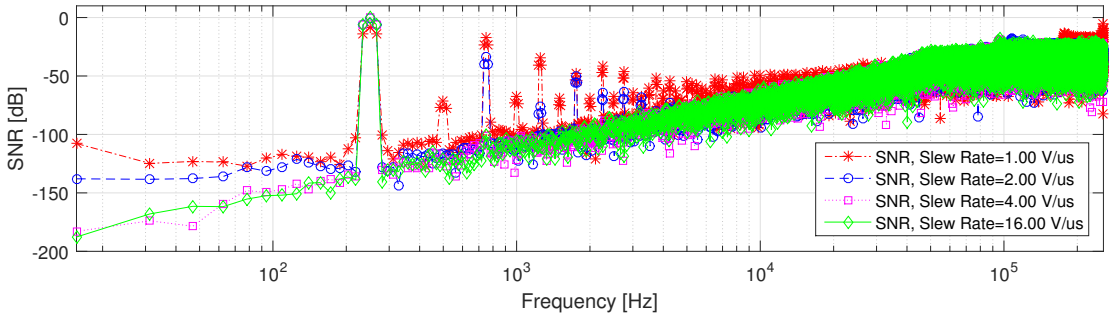


Fig. 7.6 Simulated SNR for different op-amp slew rates

Figure 7.6 illustrates how varying op-amp slew rates affect the ΣΔ modulator's performance. Low slew rates of 1 V/µs red ($\star$) and 2 V/µs blue $\circ$ cause significant

harmonic distortions at the input signal's harmonics 234.4 Hz and lower the SNR at DC. Specifically, a 1 V/µs slew rate results in large 2nd, 4th, and 6th harmonics, severely reducing the modulator's effective number of bits.

Conversely, higher slew rates of 4 V/µs magenta □ and 16 V/µs green ⋄ eliminate harmonic peaking and maintain a stable SNR, as shown in Table 7.3. These results confirm that sufficiently high slew rates ensure complete settling of internal analog nodes before the comparator triggers, thereby preserving the modulator's performance.

G [dB]	SNR [dB]	ENOB [bits]
20	66	10.71
40	97	15.88
60	102	16.37
80	104	16.54

Table 7.1 SNR results for all simulated gains

SR [V/µs]	SNR [dB]	ENOB [bits]
1	17	2.54
2	33	5.2
4	102	16.2
16	103	16.7

Table 7.2 SNR results for all simulated slew rates

Table 7.3 SNR results of gain and slew rate design space explorations

7.4 Conclusions

This chapter explores discrete-time ΣΔ ADCs, focusing on how non-ideal op-amp slew rate and gain affect a 16-bit, 1 kHz, differential, second-order, 1-bit sigma-delta modulator implemented in 180 nm technology. These op-amps function as fully-differential, discrete-time integrators. SPICE simulations were conducted to validate the MATLAB results for each scenario.

Chapter 8

Conclusions

This thesis presents the design and analysis of various electronic microstructures and circuits, with a focus on graphene-based technologies. Key achievements include the development of a GNR-based 5-bit current-steering DAC, which is utilized as a foundation for a proposed GNR-based McCulloch-Pitts neuron targeting neuromorphic computing, and the design of an ultra-low-power, current-starved GNR-based ring oscillator. Additionally, two technology-agnostic studies were conducted to investigate the impact of segmentation on DAC linearity and the effects of analog non-idealities on $\Sigma\Delta$ ADC performance. This summary highlights the thesis's main accomplishments and outlines potential avenues for future research.

8.1 Obtained results

Throughout this thesis, original contributions to the design and analysis of electronic microstructures and circuits are presented, focusing on graphene-based technologies and applicable to CMOS technologies.

In Chapter 3, a 5-bit graphene nanoribbon (GNR)-based digital-to-analog converter (DAC) is introduced, utilizing GNR unit current sources and a digital thermometric decoder for a compact, low-power implementation. SPICE simulations demonstrate significant area reduction while maintaining comparable INL and DNL to traditional FinFET-based designs.

Chapter 4 leverages the GNR-based DAC to propose a complete GNR-based McCulloch-Pitts Neuron (MCPN) for neuromorphic computing. The mixed-signal neuron features programmable synaptic weights, inhibitory inputs, GNR SRAM cells, and logic gates, with GNR-based inverter chains for threshold activation. Simulations show superior power, speed, and area performance over FinFET counterparts, validated by a 5x5 pixel pattern recognition application.

Chapter 5 explores GNR devices for ultra-low-power, high-frequency applications by designing a current-starved ring oscillator. The GNR-based oscillator achieves improved

frequency, power consumption, and power efficiency compared to a FinFET-based design, confirming GNRs' suitability for advanced low-power ICs.

Chapter 6 investigates the impact of segmentation on DNL and INL in a 10-bit, differential current-steering DAC. Simulations of various segmentation architectures reveal that increased segmentation enhances DNL while leaving INL largely unchanged. Physical implementations and Monte Carlo simulations validate the trade-off between DNL performance and decoder complexity, applicable across technologies.

Finally, Chapter 7 examines discrete-time ΣΔ ADC performance, focusing on non-ideal op-amp parameters such as slew rate and gain in a 16-bit, second-order modulator implemented in 180 nm CMOS. MATLAB and SPICE simulations assess the impact on SNR, providing insights for optimizing ADC performance amidst analog non-idealities.

This chapter summarizes the thesis's key accomplishments and suggests potential directions for future research.

8.2 Original contributions

1. Designed and simulated graphene-based microstructures optimized for the implementation of general-purpose digital (GNR-based ring oscillator) and mixed-signal (GNR-based 5-bit DAC) circuits which fulfil the roles of high-side switch, low-side switch, and analog current source [2,3].

2. Obtained clear 'on' and 'off' states for the microstructures used in the implementation of digital (GNR-based ring oscillator), mixed-signal (GNR-based 5-bit DAC), and neuromorphic (GNR-based McCulloch-Pitts neuron) blocks designed by manipulating their conductance using control voltages [1,2,3].

3. Designed digital (GNR-based ring oscillator), mixed-signal (GNR-based 5-bit DAC), and neuromorphic (GNR-based McCulloch-Pitts neuron) blocks that support the development of fully GNR-based integrated circuits (ICs) and application-specific ICs (ASICs) [1,2,3].

4. Performed circuit-level simulations for all of the proposed digital (GNR-based ring oscillator), mixed-signal (GNR-based 5-bit DAC), and neuromorphic (GNR-based McCulloch-Pitts neuron) graphene-based blocks for the design and validation of their correct operation [1,2,3].

5. Evaluated the potential of graphene-based neuromorphic (GNR-based McCulloch-Pitts neuron) blocks to extend the capabilities of standard silicon-based CMOS by comparing the proof of concept benchmark (5 by 5 pixel pattern recognition application) results of the FinFET and graphene-based circuits (one layer fully-connected neural network) to highlight the performance improvements achieved [2].

6. Investigated the design trade-offs between the complexity and area occupied by the digital decoder and the linearity performance metrics of a segmented 10-bit DAC implementation as of function of it's degree of segmentation. Conclusions are technology-agnostic and apply to both CMOS and graphene-based technologies [4,5].

7. Investigated the minimum analog performance requirements in terms of the gain and bandwidth imposed on the operational amplifiers used in the analog modulator of a ΣΔ ADC for achieving 16-bit resolution. Conclusions are technology-agnostic and apply to both CMOS and graphene-based technologies [6].

8.3 List of original publications

Publications on the topic of this thesis:

1. Florin-Silviu Dumitru, Marius Enachescu, Alexandru Antonescu, Nicoleta Cucu-Laurenciu, Sorin Cotofana, "Ultra-Low-Power Graphene-Nanoribbon-Based Current-Starved Ring Oscillator," 2024 International Semiconductor Conference (CAS), Sinaia, Romania, 2024, pp. 167-170, doi: 10.1109/CAS62834.2024.10736700.

2. Florin-Silviu Dumitru, Marius Enachescu, A. M. Antonescu, N. Cucu-Laurenciu and S. D. Cotofana, "Graphene Nanoribbon Based McCulloch-Pitts Neural Network," 2024 IEEE 24th International Conference on Nanotechnology (NANO), Gijon, Spain, 2024, pp. 592-597, doi: 10.1109/NANO61778.2024.10628801.

3. Florin-Silviu Dumitru, Nicoleta Cucu-Laurenciu, Alexandru Matei, Marius Enachescu, "Graphene Nanoribbons Based 5-bit Digital-to-Analog Converter," in IEEE Transactions on Nanotechnology (TNANO), 2021, Vol. 20, pp. 248-254, ISSN 1536-125X, ISI WOS:000637526600002.

4. Florin-Silviu Dumitru, Carmen Raluca Ilie, Mircea Bodea, Marius Enachescu, "Exploring the Effect of Segmentation on a 10-bit DAC," in Romanian Journal of Information Science and Technology (ROMJIST), 2021, Vol. 24, 2, pp. 129-142, ISSN 1453-8245, ISI WOS:000668010700001.

5. Florin-Silviu Dumitru, Carmen Raluca Ilie, Marius Enachescu, "Exploring the Effect of Segmentation on INL and DNL for a 10-bit DAC," in Proceedings of the 43rd International Semiconductor Conference (CAS), Sinaia, Romania, 2020, pp. 161-164, ISBN 978-172811073-8, ISI WOS:000637264600036.

6. Florin-Silviu Dumitru, Serban Mihalache, Marius Enachescu, "OPAMP's Finite Gain and Slew Rate impact on a 16-bit Sigma Delta ADC Performance: A case study," in Proceedings of the 40th International Semiconductor Conference

(CAS), Sinaia, Romania, 2017, pp. 161-164, ISBN 978-150903986-9, ISI WOS: 000425844500034.

Other publications:

1. Serban Mihalache, Florin-Silviu Dumitru, Adriana Florescu, Sever Viorel Pașca, "Dithering Options for Integrated Relaxation Oscillators," in Revue Roumaine des Sciences Techniques - Serie Électrotechnique et Énergétique (RRST), Bucuresti, Romania, 2017, Vol. 62, 1, pp. 61-67, ISSN 0035-4066, ISI WOS:000399629400011.

2. Serban Mihalache, Florin-Silviu Dumitru, "Current-Mode Capacitance Multiplier with Reduced Parasitic Elements," in Proceedings of the 18th Mediterranean Electrotechnical Conference (MELECON), Limassol, Cyprus, 2016, pp. 1-6, ISBN 978-1-5090-0058-6, ISI WOS:000390719500001.

3. Florin-Silviu Dumitru, Serban Mihalache, Gheorghe Brezeanu, "A CMOS Resistorless Bandgap Reference with Minimized Current Consumption," in Proceedings of the 38th International Semiconductor Conference (CAS), Sinaia, Romania, 2015, pp. 289-292, ISBN 978-1-4799-8862-4, ISI WOS:000380566400058.

4. Serban Mihalache, Irina Flamaropol, Florin-Silviu Dumitru, Lidia Dobrescu, Dragos Dobrescu, "Automated Cooling Control System through Peltier Effect and High Efficiency Control using a DC-DC Buck Converter," in Proceedings of the 38th International Semiconductor Conference (CAS), Sinaia, Romania, 2015, pp. 281-284, ISBN 978-1-4799-8862-4, ISI WOS:000380566400056.

8.4 Perspectives for further developments

Below is a brief list of potential avenues for further research in the directions established in this thesis:

1. The implementation of GNR-based mixed-signal and analog subblocks such as op-amps, ADCs, voltage regulators.

2. The existing McCulloch-Pitts neuron implementation could be enhanced using multi-bit digitally configurable synapses.

3. Implementation of more complex neuron models which more closely resemble biological neurons.

4. The implementation of 'in-memory' computation, i.e., combining the functions of memory and computation within the same circuit, using GNR-based devices.

References

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D.-e. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *science*, vol. 306, no. 5696, pp. 666–669, 2004.

[2] Y. Jiang, N. C. Laurenciu, and S. Cotofana, "Non-equilibrium green function-based verilog-a graphene nanoribbon model," in *2018 IEEE 18th International Conference on Nanotechnology (IEEE-NANO)*. IEEE, Jul. 2018. [Online]. Available: http://dx.doi.org/10.1109/NANO.2018.8626396

[3] M. M. Waldrop, "The chips are down for moore's law," *Nature*, vol. 530, no. 7589, pp. 144–147, Feb. 2016. [Online]. Available: http://dx.doi.org/10.1038/530144a

[4] T. N. Theis and H.-S. P. Wong, "The end of moore's law: A new beginning for information technology," *Computing in Science &; Engineering*, vol. 19, no. 2, pp. 41–50, Mar. 2017. [Online]. Available: http://dx.doi.org/10.1109/MCSE.2017.29

[5] F. Peper, "The end of moore's law: Opportunities for natural computing?" *New Generation Computing*, vol. 35, no. 3, pp. 253–269, Jun. 2017. [Online]. Available: http://dx.doi.org/10.1007/s00354-017-0020-4

[6] A. Chen, "Beyond-cmos roadmap-from boolean logic to neuro-inspired computing," *Japanese Journal of Applied Physics*, vol. 61, no. SM, p. SM1003, Jun. 2022. [Online]. Available: http://dx.doi.org/10.35848/1347-4065/ac5d86

[7] J. Hecht, "Nanomaterials pave the way for the next computing generation," *Nature*, vol. 608, no. 7922, pp. S2–S3, Aug. 2022. [Online]. Available: http://dx.doi.org/10.1038/d41586-022-02147-3

[8] B. Bhushan, *Springer Handbook of Nanotechnology*, ser. Springer Handbooks. Springer Berlin Heidelberg, 2017. [Online]. Available: https://books.google.ro/books?id=MWc9DwAAQBAJ

[9] A. K. Geim, "Graphene: Status and prospects," *Science*, vol. 324, no. 5934, pp. 1530–1534, Jun. 2009. [Online]. Available: http://dx.doi.org/10.1126/science.1158877

[10] G. E. Moore, "Progress in digital integrated electronics," in *Proceedings of the International Electron Devices Meeting (IEDM)*. Washington, D.C.: IEEE, 1975, pp. 11–13.

[11] R. Dennard, F. Gaensslen, H.-N. Yu, V. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted mosfet's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, Oct. 1974. [Online]. Available: http://dx.doi.org/10.1109/JSSC.1974.1050511

[12] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, "Superior thermal conductivity of single-layer graphene," *Nano Letters*, vol. 8, no. 3, pp. 902–907, Mar 2008. [Online]. Available: https://doi.org/10.1021/nl0731872

[13] E. Pop, D. Mann, Q. Wang, K. Goodson, and H. Dai, "Thermal conductance of an individual single-wall carbon nanotube above room temperature," *Nano Letters*, vol. 6, no. 1, pp. 96–100, Dec. 2005. [Online]. Available: http://dx.doi.org/10.1021/nl052145f

[14] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature materials*, vol. 6, no. 3, pp. 183–191, 2007.

[15] Y.-W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," *Phys. Rev. Lett.*, vol. 97, p. 216803, Nov 2006. [Online]. Available: https://doi.org/10.1103/PhysRevLett.97.216803

[16] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science*, vol. 319, no. 5867, pp. 1229–1232, Feb. 2008. [Online]. Available: http://dx.doi.org/10.1126/science.1150878

[17] A. S. Mayorov, R. V. Gorbachev, S. V. Morozov, L. Britnell, R. Jalil, L. A. Ponomarenko, P. Blake, K. S. Novoselov, K. Watanabe, T. Taniguchi, and A. K. Geim, "Micrometer-scale ballistic transport in encapsulated graphene at room temperature," *Nano Letters*, vol. 11, no. 6, pp. 2396–2399, May 2011. [Online]. Available: http://dx.doi.org/10.1021/nl200758b

[18] Y. Jiang, N. C. Laurenciu, and S. D. Cotofana, "On carving basic boolean functions on graphene nanoribbons conduction maps," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2018, pp. 1–5.

[19] Y. Jiang, N. C. Laurenciu, and S. Cotofana, "Complementary arranged graphene nanoribbon-based boolean gates," in *Proceedings of the 14th IEEE/ACM International Symposium on Nanoscale Architectures*, 2018, pp. 51–57.

[20] Y. Jiang, N. Cucu Laurenciu, and S. D. Cotofana, "On Basic Boolean Function Graphene Nanoribbon Conductance Mapping." *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 5, pp. 1948–1959, 2019.

[21] R. Peierls, "Quelques propriétés typiques des corps solides," *Annales de l'institut Henri Poincaré*, vol. 5, no. 3, pp. 177–222, 1935. [Online]. Available: http://eudml.org/doc/78996

[22] L. D. Landau, "Zur theorie der phasenumwandlungen ii," *Phys. Z. Sowjetunion*, vol. 11, no. 545, pp. 26–35, 1937.

[23] N. D. Mermin, "Crystalline order in two dimensions," *Phys. Rev.*, vol. 176, pp. 250–254, Dec 1968. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.176.250

[24] M. Ashton, J. Paul, S. B. Sinnott, and R. G. Hennig, "Topology-scaling identification of layered solids and stable exfoliated 2d materials," *Physical Review Letters*, vol. 118, no. 10, Mar. 2017. [Online]. Available: http://dx.doi.org/10.1103/PhysRevLett.118.106101

[25] P. R. Wallace, "The band theory of graphite," *Phys. Rev.*, vol. 71, pp. 622–634, May 1947. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.71.622

[26] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, pp. 109–162, Jan 2009. [Online]. Available: https://link.aps.org/doi/10.1103/RevModPhys.81.109

[27] Y. Obeng and P. Srinivasan, "Graphene: Is it the future for semiconductors? an overview of the material, devices, and applications," *Interface magazine*, vol. 20, no. 1, pp. 47–52, Jan. 2011. [Online]. Available: http://dx.doi.org/10.1149/2.F05111if

[28] B. Partoens and F. M. Peeters, "From graphene to graphite: Electronic structure around the *k* point," *Phys. Rev. B*, vol. 74, p. 075404, Aug 2006. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.74.075404

[29] P. A. M. Dirac and R. H. Fowler, "The quantum theory of the electron," *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character*, vol. 117, no. 778, pp. 610–624, 1928. [Online]. Available: https://royalsocietypublishing.org/doi/abs/10.1098/rspa.1928.0023

[30] E. McCann, "Asymmetry gap in the electronic band structure of bilayer graphene," *Physical Review B*, vol. 74, no. 16, Oct. 2006. [Online]. Available: http://dx.doi.org/10.1103/PhysRevB.74.161403

[31] E. V. Castro, K. S. Novoselov, S. V. Morozov, N. M. R. Peres, J. M. B. L. dos Santos, J. Nilsson, F. Guinea, A. K. Geim, and A. H. C. Neto, "Biased bilayer graphene: Semiconductor with a gap tunable by the electric field effect," *Physical Review Letters*, vol. 99, no. 21, Nov. 2007. [Online]. Available: http://dx.doi.org/10.1103/PhysRevLett.99.216802

[32] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov, "Two-dimensional gas of massless dirac fermions in graphene," *Nature*, vol. 438, no. 7065, pp. 197–200, Nov 2005. [Online]. Available: https://doi.org/10.1038/nature04233

[33] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, and M. S. Fuhrer, "Intrinsic and extrinsic performance limits of graphene devices on sio2," *Nature Nanotechnology*, vol. 3, no. 4, pp. 206–209, Mar. 2008. [Online]. Available: http://dx.doi.org/10.1038/nnano.2008.58

[34] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, "Ultrahigh electron mobility in suspended graphene," *Solid State Communications*, vol. 146, no. 9, pp. 351–355, 2008. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0038109808001178

[35] S. V. Morozov, K. S. Novoselov, F. Schedin, D. Jiang, A. A. Firsov, and A. K. Geim, "Two-dimensional electron and hole gases at the surface of graphite," *Phys. Rev. B*, vol. 72, p. 201401, Nov 2005. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.72.201401

[36] S. Datta, *Lessons From Nanoelectronics: A New Perspective On Transport.* World Sci. Publ., 2012.

[37] S. Datta, *Electronic transport in mesoscopic systems*. Cambridge university press, 1997.

[38] R. Landauer, "Spatial variation of currents and fields due to localized scatterers in metallic conduction," *IBM Journal of Research and Development*, vol. 1, no. 3, pp. 223–231, 1957. [Online]. Available: https://doi.org/10.1147/rd.13.0223

[39] R. Murali, Y. Yang, K. Brenner, T. Beck, and J. D. Meindl, "Breakdown current density of graphene nanoribbons," *Applied Physics Letters*, vol. 94, no. 24, Jun. 2009. [Online]. Available: http://dx.doi.org/10.1063/1.3147183

[40] A. Behnam, A. S. Lyons, M.-H. Bae, E. K. Chow, S. Islam, C. M. Neumann, and E. Pop, "Transport in nanoribbon interconnects obtained from graphene grown by chemical vapor deposition," *Nano Letters*, vol. 12, no. 9, pp. 4424–4430, Aug. 2012. [Online]. Available: http://dx.doi.org/10.1021/nl300584r

[41] D. Lungerich, O. Papaianina, M. Feofanov, J. Liu, M. Devarajulu, S. I. Troyanov, S. Maier, and K. Amsharov, "Dehydrative π-extension to nanographenes with zig-zag edges," *Nature Communications*, vol. 9, no. 1, Nov. 2018. [Online]. Available: http://dx.doi.org/10.1038/s41467-018-07095-z

[42] M. Y. Han, B. Özyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Phys. Rev. Lett.*, vol. 98, p. 206805, May 2007. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.98.206805

[43] K. Nakada, M. Fujita, G. Dresselhaus, and M. S. Dresselhaus, "Edge state in graphene ribbons: Nanometer size effect and edge shape dependence," *Phys. Rev. B*, vol. 54, pp. 17 954–17 961, Dec 1996. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.54.17954

[44] L. Brey and H. A. Fertig, "Electronic states of graphene nanoribbons studied with the dirac equation," *Phys. Rev. B*, vol. 73, p. 235411, Jun 2006. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.73.235411

[45] J. Hass, R. Feng, T. Li, X. Li, Z. Zong, W. A. de Heer, P. N. First, E. H. Conrad, C. A. Jeffrey, and C. Berger, "Highly ordered graphene for two dimensional electronics," *Applied Physics Letters*, vol. 89, no. 14, Oct. 2006. [Online]. Available: http://dx.doi.org/10.1063/1.2358299

[46] J. Hass, W. A. de Heer, and E. H. Conrad, "The growth and morphology of epitaxial multilayer graphene," *Journal of Physics: Condensed Matter*, vol. 20, no. 32, p. 323202, Jul. 2008. [Online]. Available: http://dx.doi.org/10.1088/0953-8984/20/32/323202

[47] C. Chen, Y. Lin, W. Zhou, M. Gong, Z. He, F. Shi, X. Li, J. Z. Wu, K. T. Lam, J. N. Wang, F. Yang, Q. Zeng, J. Guo, W. Gao, J.-M. Zuo, J. Liu, G. Hong, A. L. Antaris, M.-C. Lin, W. L. Mao, and H. Dai, "Sub-10-nm graphene nanoribbons with atomically smooth edges from squashed carbon nanotubes," *Nature Electronics*, vol. 4, no. 9, pp. 653–663, Sep 2021. [Online]. Available: https://doi.org/10.1038/s41928-021-00633-6

[48] D. Kondo, H. Nakano, B. Zhou, A. I, K. Hayashi, M. Takahashi, S. Sato, and N. Yokoyama, "Sub-10-nm-wide intercalated multi-layer graphene interconnects with low resistivity," in *IEEE International Interconnect Technology Conference*. IEEE, May 2014. [Online]. Available: http://dx.doi.org/10.1109/IITC.2014.6831867

[49] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-area synthesis of high-quality and uniform graphene films on copper foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, Jun. 2009. [Online]. Available: http://dx.doi.org/10.1126/science.1171245

[50] A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, "Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition," *Nano Letters*, vol. 9, no. 1, pp. 30–35, Jan. 2009. [Online]. Available: http://dx.doi.org/10.1021/nl801827v

[51] J. Cai, P. Ruffieux, R. Jaafar, M. Bieri, T. Braun, S. Blankenburg, M. Muoth, A. P. Seitsonen, M. Saleh, X. Feng, K. Müllen, and R. Fasel, "Atomically precise bottom-up fabrication of graphene nanoribbons," *Nature*, vol. 466, no. 7305, pp. 470–473, Jul. 2010. [Online]. Available: http://dx.doi.org/10.1038/nature09211

[52] N. F. Kleimeier, A. Timmer, L. Bignardi, H. Mönig, X. L. Feng, K. Müllen, L. F. Chi, H. Fuchs, and H. Zacharias, "Electron dynamics in unoccupied states of spatially aligned 7-a graphene nanoribbons on au(788)," *Physical Review B*, vol. 90, no. 24, Dec. 2014. [Online]. Available: http://dx.doi.org/10.1103/PhysRevB.90.245408

[53] D. Boesing, "A cable backplane solution for 112 gbps pam4 architecture," https://blog.samtec.com/post/a-cable-backplane-solution-for-112-gbps-pam4-architecture/, 2020, accessed: 2024-08-23.

[54] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-ghz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, pp. 662–662, Feb. 2010. [Online]. Available: http://dx.doi.org/10.1126/science.1184289

[55] F.-S. Dumitru, N. Cucu-Laurenciu, A. Matei, and M. Enachescu, "Graphene nanoribbons based 5-bit digital-to-analog converter," *IEEE Transactions on Nanotechnology*, vol. 20, pp. 248–254, 2021. [Online]. Available: http://dx.doi.org/10.1109/TNANO.2021.3063602

[56] M. Enachescu, M. Lefter, A. Bazigos, A. M. Ionescu, and S. D. Cotofana, "Ultra low power NEMFET based logic." in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2013, pp. 566–569.

[57] Y. Jiang, N. C. Laurenciu, H. Wang, and S. D. Cotofana, "Graphene nanoribbon based complementary logic gates and circuits," *IEEE Transactions on Nanotechnology*, vol. 18, pp. 287–298, 2019.

[58] W. S. McCulloch and W. Pitts, "A logical calculus of the ideas immanent in nervous activity." *Bulletin of Mathematical Biophysics*, vol. 5, pp. 115–133, 1943.

[59] I. Karafyllidis, "Current Switching in Graphene Quantum Point Contacts." *IEEE Transactions on Nanotechnology (TNANO)*, vol. 13, pp. 820–824, 2014.

[60] S. Datta, *Quantum Transport: Atom to Transistor.* Cambridge University Press, 2005.

[61] I. Nikiforidis, I. Karafyllidis, and P. Dimitrakis, "Simulation and parametric analysis of graphene p-n junctions with two rectangular top gates and a single back gate." *Journal of Physics D: Applied Physics*, vol. 51, pp. 1–6, 2018.

[62] C. -H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2." *IEEE Journal of solid state circuits*, vol. 33, no. 12, pp. 1948–1958, 1998.

[63] H. Wang, N. C. Laurenciu, Y. Jiang, and S. D. Cotofana, "Atomistic-level hysteresis-aware graphene structures electron transport model," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2019, pp. 1–5.

[64] F.-S. Dumitru, M. Enachescu, A. M. Antonescu, N. Cucu-Laurenciu, and S. D. Cotofana, "Graphene nanoribbon based mcculloch-pitts neural network," in *2024 IEEE 24th International Conference on Nanotechnology (NANO)*, 2024, pp. 592–597. [Online]. Available: http://dx.doi.org/10.1109/NANO61778.2024.10628801

[65] H. Wang, N. C. Laurenciu, Y. Jiang, and S. D. Cotofana, "Ultra-compact, entirely graphene-based nonlinear leaky integrate-and-fire spiking neuron," in *IEEE ISCAS*, 2020, pp. 1–5.

[66] ——, "Graphene nanoribbon-based synapses with versatile plasticity," in *NANOARCH*, 2019, p. 1.

[67] ——, "Compact graphene-based spiking neural network with unsupervised learning capabilities," *IEEE Open Journal of Nanotechnology*, vol. 1, 2020.

[68] F.-S. Dumitru, M. Enachescu, A. Antonescu, N. Cucu-Laurenciu, and S. Cotofana, "Ultra-low-power graphene-nanoribbon-based current-starved ring oscillator," in *2024 International Semiconductor Conference (CAS)*, 2024, pp. 167–170.

[69] F.-S. Dumitru, C. R. Ilie, M. Bodea, and M. Enachescu, "Exploring the effect of segmentation on a 10-bit dac," *ROMANIAN JOURNAL OF INFORMATION SCIENCE AND TECHNOLOGY*, vol. 24, no. 2, pp. 129–142, 2021.

[70] F.-S. Dumitru, C. R. Ilie, and M. Enachescu, "Exploring the effect of segmentation on inl and dnl for a 10-bit dac," in *2020 International Semiconductor Conference (CAS)*, 2020, pp. 161–164. [Online]. Available: http://dx.doi.org/10.1109/CAS50358.2020.9268011

[71] C.-H. Lin and K. Bult, "A 10-b, 500-msample/s cmos dac in 0.6 mm/sup 2/," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 1948–1958, 1998.

[72] F.-S. Dumitru, C. R. Ilie, and M. Enachescu, "Exploring the effect of segmentation on inl and dnl for a 10-bit dac," in *2020 International Semiconductor Conference (CAS)*, 2020, pp. 161–164.

[73] B. Razavi, "The current-steering dac [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 10, no. 1, pp. 11–15, 2018.

[74] R. Jiang, G. Adhikari, Y. Sun, D. Yao, R. Takahashi, Y. Ozawa, N. Tsukiji, H. Kobayashi, and R. Shiota, "Gray-code input dac architecture for clean signal generation," in *2017 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*, 2017, pp. 669–674.

[75] B. Razavi, *Principles of Data Conversion System Design*, ser. Electrical engineering, circuits and systems. Wiley, 1995.

[76] M. Bodea, I. Mihut, L. Turic, and V. Tiponut, "Aparate electronice pentru masurare si control," *Bucuresti, Editura Didactica si pedagogica*, 1985.

[77] G. I. Radulov, "Flexible and self-calibrating current-steering digital-to-analog converters: analysis, classification and design," Ph.D. dissertation, Technische Universiteit Eindhoven, 2010.

[78] "Eecs instructional and electronics support - data converters – dac design," Lecture 14, University of California, Berkeley, 2017, eECS Instructional and Electronics Support. [Online]. Available: https://www.eecs.berkeley.edu/

[79] P. Palmers and M. S. J. Steyaert, "A 10-bit 1.6-gs/s 27-mw current-steering d/a converter with 550-mhz 54-db sfdr bandwidth in 130-nm cmos," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 11, pp. 2870–2879, 2010.

[80] J. Deveugele and M. Steyaert, "A 10-bit 250-ms/s binary-weighted current-steering dac," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 320–329, 2006.

[81] "Genus synthesis solution," Online, Jan. 2021, available: https://www.cadence.com/en_US/home/tools/digital-design-and-signoff/synthesis/genus-synthesis-solution.html.

[82] F.-S. Dumitru, S. Mihalache, and M. Enachescu, "Opamp's finite gain and slew rate impact on a 16-bit $\sigma\delta$ adc performance: A case study," in *2017 International Semiconductor Conference (CAS)*, 2017, pp. 161–164. [Online]. Available: http://dx.doi.org/10.1109/SMICND.2017.8101187

[83] S. Pavan, R. Schreier, and G. C. Temes, *Understanding delta-sigma data converters*. John Wiley & Sons, 2017.

[84] J. M. de la Rosa, "Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 1–21, 2010.

[85] H. Khorramabadi, "Ee 247 analysis and design of vlsi analog digital interface integrated circuits," *Lecture Notes*, 2009.

[86] D. A. Johns and K. Martin, *Analog integrated circuit design*. John Wiley & Sons, 2008.

[87] J. M. De la Rosa and R. Del Rio, *CMOS sigma-delta converters: Practical design guide*. John Wiley & Sons, 2013.

[88] D. S. Cadence, *Process Design Kit Reference Manual for Generic Process Design Kit 180nm Rev3.3*, 2008.