(+40)764269164 Bucharest, RO daniela.ciubar@gmail.com LinkedIn ORCID

Mihaela-Daniela Dobre (Ciubăr)

ELECTRONICS ENGINEER

Objective

Experienced electronics engineer with a strong academic foundation in analog/mixed-signal design and I/O circuit development, complemented by hands-on industry experience in verification and technical support. Seeking to contribute to innovative I/O design teams while deepening expertise through continued learning and research-driven problem solving.

Education

2016 - Present **Polytechnic University of Bucharest, Romania**
Ph.D. in Electronics Engineering

Thesis: "*Electrostatic Discharge and Latch-up Protection Structures for Nanometric Technologies*"
Advisor: Prof. Dr. Ing. Gheorghe Brezeanu

2014 – 2016 **MS in Electronics Engineering**
Specialization: Microsystems
Polytechnic University of Bucharest

Thesis: "Analiza Comparativă a Performanţelor Librăriilor de Pad-uri din Structura Circuitelor Integrate"/ "Comparative Analysis of Pad Library Performance in Integrated Circuit Structures"
Advisor: Prof. Dr. Ing. Gheorghe Brezeanu

2010 - 2014 **B.Sc. in Electronics, Telecommunications and Information Technology**
Specialization: Microelectronics, Optoelectronics & Nanotechnology
Polytechnic University of Bucharest

Thesis: "Măsurarea Temperaturii Tranzistoarelor MOS de Putere prin Parametrii Electrici Termo-Senzitivi" / "Temperature Measurement of Power MOS Transistors Using Thermo-Sensitive Electrical Parameters"
Advisor: Prof. Dr. Ing. Gheorghe Brezeanu

2010 - 2014 **B.Sc. in Electronics, Telecommunications and Information Technology**
Specialization: Teacher Training Department
Polytechnic University of Bucharest

2006 - 2010 **High School Diploma – Mathematics and Informatics**
"Mihai Viteazul" Theoretical High School, Caracal, Romania

Publications

Journal publications

Dobre M-D, Coll P, Brezeanu G, "CDM Protection Test Structure for I/O Cells in a Submicronic Technology," vol. Electronics, p. 4, 2021, https://doi.org/10.3390/electronics10040443.

Journal papers in review

M. -D. Dobre, C.-Y. Chang, C.-K. Chen, P. Coll and G. Brezeanu, "On-Silicon Characterization of CDM-ESD Protections in Nanometric ICs via vf-TLP".
Submitted to: IEEE Transactions on Device and Materials Reliability.

Conference papers

M. -D. Dobre and G. Brezeanu, "Pad cells performances in submicron technologies," 2016 International Semiconductor Conference (CAS), Sinaia, Romania, 2016, pp. 205-208, doi: 10.1109/SMICND.2016.7783087.

M. -D. Dobre, P. Coll and G. Brezeanu, "I/O library comparison methodology for 40nm CMOS technology," 2017 International Semiconductor Conference (CAS), Sinaia, Romania, 2017, pp. 183-186, doi: 10.1109/SMICND.2017.8101194.

R. -V. Petrica, M. -D. Dobre, P. Coll, F. Draghici and G. Brezeanu, "Comparison of Level Shifter Architectures: Application to I/O Cell," 2018 International Semiconductor Conference (CAS), Sinaia, Romania, 2018, pp. 209-212, doi: 10.1109/SMICND.2018.8539796.

M. -D. Dobre, P. Coll and G. Brezeanu, "I/O Cells Latch-up Immunity: Methodology for Compact Layout Rules in an Advanced CMOS Technology," 2020 International Semiconductor Conference (CAS), Sinaia, Romania, 2020, pp. 115-118, doi: 10.1109/CAS50358.2020.9268033.

M. -D. Dobre, P. Coll and G. Brezeanu, "A Study on ESD-CDM Cross-Power Domain Failures," 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Villasimius, SU, Italy, 2022, pp. 21-24, doi: 10.1109/PRIME55000.2022.9816786.

M. -D. Dobre, P. Coll and G. Brezeanu, "Validation Technique for Thin Oxide CDM Protections," 2022 International Semiconductor Conference (CAS), Poiana Brasov, Romania, 2022, pp. 131-134, doi: 10.1109/CAS56377.2022.9934740.

Work Experience

January 2015 - Present
I/O Design Engineer
Microchip Technology Inc., Bucharest Romania
Responsibilities:
- Design and simulate general-purpose I/O cells) across PVT corners using industry-standard EDA tools (Cadence Virtuoso, Spectre).
- Integrate on-chip ESD protection structures (SCR, ggNMOS, diode clamps) to ensure compliance with HBM, CDM, and MM standards.
- Perform Liberty (.lib) and IBIS (.ibs) characterization of I/O libraries, including corner case validation and signal integrity analysis.
- Support package-level integration, including pad placement optimization, bump assignment, and SI co-analysis with packaging teams.
- Conduct full LVS, DRC, ERC, and latch-up rule checks; participate in design reviews and post-silicon debug when required.
- Generate I/O views and models for integration into SoC-level floorplans and digital implementation flows.
- Collaborate with analog, ESD, and packaging teams to deliver reliable, manufacturable I/O solutions for production tape-out.
- Apply knowledge of interface standards (LVCMOS, SSTL, HSTL) and I/O timing/power modeling in design and verification processes.
- Grew the I/O team from 1 to 7 engineers, establishing workflows, mentoring junior designers, and aligning team goals with company-wide roadmaps.
- Promoted to I/O Team Manager in August 2023, overseeing project planning, resource allocation, and cross-functional collaboration.

Note: On maternity leave from December 2023 till October 2025.

November 2013 – December 2014
Component Verification Engineering – Working Student
Infineon Technologies, Bucharest Romania
Responsibilities:
- Performed functional testing and verification of high-side power switches in alignment with datasheet specifications.
- Conducted electrical measurements (e.g., R_{DSon}, I_{LIM}, V_{ON}) using lab instrumentation and automated setups.
- Documented test results and supported failure analysis for out-of-spec behaviors.
- Collaborated with design and validation teams to refine test coverage and improve verification efficiency.

June 2013 – August 2013
Summer Intern
Microchip Technology Inc., Bucharest Romania
Responsibilities:
- Designed and prototyped a PIC18F4550-based development board using Eagle (schematic, layout, PCB fabrication).
- Created a component library and programmed PIC MCUs in C.
- Gained exposure to project planning and cost estimation for small-scale hardware production.

December 2012 – June 2013
Technical Support Engineer
Titan International Wholesale, Bucharest Romania
Responsibilities:
- Handled client support tickets and coordinated issue resolution with vendors using internal reporting systems.
- Monitored network performance, assisted with billing updates and rate imports.
- Collaborated with technical and sales teams to generate traffic reports.

July 2012 – August 2012
Summer Intern
Orange, Bucharest Romania
Responsibilities:
- Assisted with purchase orders, invoice checks, and data entry in internal systems; supported device unlocking processes.

Languages

Romanian	Native language
English	Advanced Listening, Speaking, Reading and Writing.
French	Intermediate Listener, Novice Speaker, Intermediate Reading and Writing.

Computer skills

Technical & EDA Tools

- Cadence Virtuoso – analog/mixed-signal circuit design and simulation (I/O design, ESD structures)
- Eagle – PCB schematic and layout design
- Calibre – physical verification (DRC, LVS, ERC)

Modeling & Characterization

- SPICE – analog/mixed-signal simulation and validation
- Synopsys HSPICE / Primetime – for Liberty timing characterization
- IBIS model generation tools – Synopsys tools
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- Verilog – behavioral modeling

General Programming / Scripting

- C – microcontroller programming (PIC)
- Python/Tcl/Bash – scripting for automation and data processing
- LabVIEW / MATLAB (if used in lab measurements or data analysis during component verification)

Productivity / Collaboration

- Microsoft Office – reporting, documentation, communication
- JIRA – for technical support and issue tracking
- Confluence – collaborative documentation platforms