

Model F17 - Memoriul științific al studentului doctorand

MEMORIU ȘTIINȚIFIC

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Studii de doctorat

Perioada: 2016-2025

Conducător științific: Prof.dr.ing. Gheorghe BREZEANU

Domeniu: Inginerie Electronică, Telecomunicații și Tehnologii Informaționale

Titlul tezei de doctorat: Structuri de protecție la descărcări electrostatice și efectul de blocare (LATCH-UP) pentru tehnologii nanometrice / Electrostatic Discharge and Latch-up Protection Structures for Nanometric Technologies

Activitate științifică

A. Lista de lucrări științifice (articole în reviste sau volume)

1. **Dobre M.-D.**, Coll P., Brezeanu G., "CDM Protection Test Structure for I/O Cells in a Submicronic Technology," vol. Electronics, ISSN: 2079-9292, 2021, <https://doi.org/10.3390/electronics10040443>.
2. **M. -D. Dobre**, C.-Y. Chang, C.-K. Chen, P. Coll and G. Brezeanu, "On-Silicon Characterization of CDM-ESD Protections in Nanometric ICs via vf-TLP" – trimisă la IEEE Transactions on Device and Materials Reliability.

B. Participări la conferințe/workshop-uri

1. **M. -D. Dobre** and G. Brezeanu, "Pad cells performances in submicron technologies," 2016 International Semiconductor Conference (CAS), ISBN: 978-1-5090-1208-4, Sinaia, Romania, 2016, pp. 205-208, doi: [10.1109/SMICND.2016.7783087](https://doi.org/10.1109/SMICND.2016.7783087).
2. **M. -D. Dobre**, P. Coll and G. Brezeanu, "I/O library comparison methodology for 40nm CMOS technology," 2017 International Semiconductor Conference (CAS), Sinaia, Romania, 2017, Curran Associates – 978-1-5090-3986-9 (physical); 978-1-5090-3985-2 (electronic) pp. 183-186, doi: [10.1109/SMICND.2017.8101194](https://doi.org/10.1109/SMICND.2017.8101194).
3. **M. -D. Dobre**, P. Coll and G. Brezeanu, "I/O Cells Latch-up Immunity: Methodology for Compact Layout Rules in an Advanced CMOS Technology," 2020 International Semiconductor Conference (CAS), Sinaia, Romania, 2020, ISBN: 978-1-7281-1074-5 (POD); 978-1-7281-1073-8 (online), pp. 115-118, doi: [10.1109/CAS50358.2020.9268033](https://doi.org/10.1109/CAS50358.2020.9268033).
4. R. -V. Petrica, **M. -D. Dobre**, P. Coll, F. Draghici and G. Brezeanu, "Comparison of Level Shifter Architectures: Application to I/O Cell," 2018 International Semiconductor Conference (CAS), Sinaia, Romania, Print on Demand(PoD) ISSN: 1545-827X 2018, pp. 209-212, doi: [10.1109/SMICND.2018.8539796](https://doi.org/10.1109/SMICND.2018.8539796).

5. **M. -D. Dobre**, P. Coll and G. Brezeanu, "A Study on ESD-CDM Cross-Power Domain Failures," 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Villasimius, SU, Italy, 2022, ISBN:978-1-6654-6700-1, PoD ISBN:978-1-6654-6701-8, pp. 21-24, doi: [10.1109/PRIME55000.2022.9816786](https://doi.org/10.1109/PRIME55000.2022.9816786).
6. **M. -D. Dobre**, P. Coll and G. Brezeanu, "Validation Technique for Thin Oxide CDM Protections," 2022 International Semiconductor Conference (CAS), Poiana Brasov, Romania, 2022, ISSN: 2377-0678, PoD ISSN: 1545-827X, pp. 131-134, doi: [10.1109/CAS56377.2022.9934740](https://doi.org/10.1109/CAS56377.2022.9934740).

E. Proiecte de cercetare științifică

1. **Mihaela-Daniela Dobre** "Influence of pad cells on chip's functionality. Latch-up and prevention", PhD Exam1, University Politehnica, Doctoral School of Electronics, Telecommunications and Information Technology, April 2017.
2. **Mihaela-Daniela Dobre** "ESD Protection in PAD Cells", PhD Exam2, University Politehnica, Doctoral School of Electronics, Telecommunications and Information Technology, October 2017.
3. **Mihaela-Daniela Dobre** "I/O cells:State of the art", PhD Report1, University Politehnica, Doctoral School of Electronics, Telecommunications and Information Technology, June 2017.
4. **Mihaela-Daniela Dobre** "I/O Library Comparison Methodology for 40nm CMOS Technology", PhD Report2, University Politehnica, Doctoral School of Electronics, Telecommunications and Information Technology, December 2017.
5. **Mihaela-Daniela Dobre** "Latchup rules – methodology and implementation for 55nm technology I/Os", PhD Report3, University Politehnica, Doctoral School of Electronics, Telecommunications and Information Technology, June 2018.
6. **Mihaela-Daniela Dobre** "CDM Test-chip; Principle and Implementation", PhD Report4, University Politehnica, Doctoral School of Electronics, Telecommunications and Information Technology, November 2018.
7. **Mihaela-Daniela Dobre** "CDM Test chip: Results post ESD stress", PhD Report5, University Politehnica, Doctoral School of Electronics, Telecommunications and Information Technology, June 2019.

Student-doctorand

