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# Ph.D. THESIS SUMMARY

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# ELECTROSTATIC DISCHARGE AND LATCH-UP PROTECTION STRUCTURES FOR NANOMETRIC TECHNOLOGIES
# STRUCTURI DE PROTECȚIE LA DESCĂRCĂRI ELECTROSTATICE ȘI EFECTUL DE BLOCARE (LATCH-UP) PENTRU TEHNOLOGII NANOMETRICE

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# Contents

# CHAPTER 1

# Introduction

As CMOS (Complementary Metal Oxide Semiconductor) technologies scale into the nanometer regime, challenges related to electrostatic discharge (ESD) and latch-up become increasingly critical due to worsened parasitic effects and shrinking reliability margins. This research addresses these challenges by proposing and validating original testing methodologies and protection structures for ESD [1] [2] and latch-up [3] in advanced technology nodes. The work is structured chronologically, with each chapter aligning to a specific technology generation and corresponding reliability solution.

## 1.1 Objectives and Contribution of the thesis

This thesis addresses the escalating vulnerability of advanced CMOS technologies to ESD and latch-up events, focusing on sub-55 nm nodes where reduced oxide thickness and interconnect scaling exacerbate susceptibility. The primary objective is to develop and validate robust, area-efficient CDM-ESD (Charged Device Model - Electrostatic Discharge) and latch-up protection strategies tailored to 55 nm, 40 nm, and 28 nm technologies. Key goals include:

- Optimizing guard ring design using a Design of Experiment (DOE)-based methodology for latch-up immunity in 55 nm I/O (Input/Output) libraries.
- Implementing grounded-gate nMOS (ggnMOS) protection for CDM robustness at 40 nm across multiple power domains.
- Establishing safe ground resistance thresholds for long-wire CDM scenarios.
- Proposing vf-TLP (very fast Transmission Line Pulse)-validated CDM protection architectures for 28 nm thin-oxide nodes, including duo-diodes, trio-diodes, and ggnMOS.

The research employs a comprehensive methodology combining theoretical modeling, simulations, DOE-driven layout optimization, silicon prototyping, and FICDM (Field Induced CDM) experimental testing using Orion2 [4] CDM systems and vf-TLP setups. Stress conditions up to 2000 V were used to evaluate the performance of various protection topologies under realistic operating scenarios. Several original contributions have been made:

1. A systematic, DOE-based methodology was introduced for optimizing guard ring layouts to reduce area while maintaining latch-up immunity.
2. Optimal ggnMOS geometries for CDM-ESD protection were identified, with dimensional guidelines suited for 40 nm nodes.
3. Novel CDM protection strategies were proposed and validated using FICDM and vf-TLP methodologies.

4. Compact, cross-power domain protection schemes were demonstrated, improving reliability in multi-domain ICs (Integrated Circuits).
5. An empirical relationship between CDM stress levels and allowable ground resistance was established, offering practical routing guidance.

Collectively, these advancements provide scalable, area-efficient solutions for improving ESD and latch-up resilience in modern semiconductor designs.

## 1.2 Thesis structure

This thesis is structured into an introductory chapter, four main technical chapters, and a concluding chapter. Chapter 2 provides a review of the literature, outlining the evolution of latch-up and ESD protection methods, current reliability challenges in nanometric CMOS technologies, and the role of I/O cells as the integration point for protection structures. It also introduces key protection strategies aligned with this research. Chapter 3 focuses on latch-up immunity in 55 nm technology, presenting a DOE-based methodology for optimizing guard ring layouts to reduce silicon area while maintaining JEDEC (Joint Electron Device Engineering Council)-compliant protection. Chapter 4 addresses CDM-ESD protection in 40 nm CMOS, evaluating ggnMOS devices under various geometries and stress levels, and establishing layout guidelines with attention to ground resistance and cross-power domain interactions. Chapter 5 shifts to 28 nm technology, proposing protection schemes for long interconnect scenarios using diode-based and ggnMOS structures. Validation is performed through CDM stress testing (vf-TLP), with a focus on protecting thin gate oxides. The final chapter consolidates the thesis findings, highlights original contributions, and outlines future research directions.

# Chapter 2

# State of the Art

**Electrostatic Discharge** is a major reliability concern [5] in modern CMOS technologies, characterized using standardized models such as the Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM) [1] [6]. As CMOS scaling reduces gate oxide thickness and feature sizes, devices become more vulnerable to CDM events due to their fast voltage rise times and internal stress mechanisms. Unlike HBM or MM, CDM can impact any pin unpredictably, making it the dominant ESD failure mode in sub-65 nm nodes. This thesis focuses on evaluating ggnMOS and diode-based protection devices (Table 2.1) across 40 nm and 28 nm technologies. Both FICDM and vf-TLP testing are used: FICDM in Chapter 4 for formal stress validation, and vf-TLP in Chapter 5 for detailed transient analysis and optimization.

**Latch-up** in CMOS circuits is caused by the unintended activation of a parasitic p-n-p-n thyristor structure formed between n-type MOS (nMOS) and p-type MOS (pMOS) transistors in the well/substrate regions [7] [8]. This self-sustaining feedback loop, often

triggered by transient events like voltage overshoots, ESD pulses, or substrate noise, can result in high current flow between power and ground, leading to damage. To prevent latch-up, modern processes employ various strategies such as guard rings, well spacing, retrograde wells, and deep n-well isolation to suppress the gain or connectivity of parasitic transistors [9] [10]. Latch-up testing is standardized under JEDEC JESD78 [11]. The device must return to nominal current after stress to be considered latch-up free. Simulated validation in this research evaluates how layout features influence latch-up immunity by correlating test pass/fail outcomes with physical design parameters, providing design guidelines. Overall, robust latch-up prevention relies on a combination of optimized layout, circuit strategies, and compliance with standardized test protocols.

***Table 2.1*** *Comparison of ESD protection structures.*

| Feature / Device | ggnMOS | Diode-based Protection |
|---|---|---|
| **Trigger Mechanism** | Junction breakdown & snapback | Forward-biased diode conduction |
| **Response Speed** | Fast | Very fast |
| **Area Efficiency** | Moderate | High |
| **Leakage Current** | Low to moderate | Very low |

# Chapter 3

# A Methodology for Latch-up Rule Definition

The need to ensure latch-up immunity under all conditions has led foundries to impose conservative layout design rules (e.g. minimum spacing and guard ring requirements) that can significantly increase chip area in I/O circuits [12]. At the same time, the industry demands compact and cost-effective designs – I/O pad areas are often at a premium, and excessive guard banding or spacing reduces functional density [13]. Therefore, developing effective latch-up suppression and ESD protection strategies that meet reliability standards without undue area penalty is of paramount importance in advanced node chip design. In this chapter, the mechanisms and importance of latch-up protection are overviewed, and a new methodology to optimize latch-up immunity in CMOS I/O structures is proposed. The proposed steps to follow in order to achieve proper latchup protection, but at the same time minimize the area occupied by the guard rings acting as a shield:

1) Structure Definition: Propose the latch-up protection circuit.
2) Parameter Setup: Define key guard ring dimensions (e.g., GW_p_tap, GW_n_tap, Dp, Dn) with initial, minimum, and maximum values for optimization.

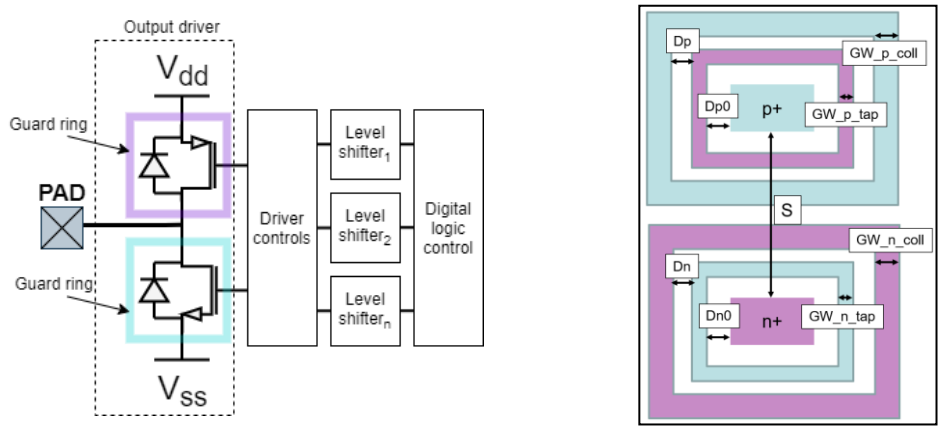
3) DOE Optimization: Apply Design of Experiment (DOE) techniques to systematically explore parameter combinations and reduce layout iterations.
4) Layout Design: Implement the optimized structure using CAD tools, translating parameters into a complete physical layout.
5) Post-layout Validation: Simulate the final layout to assess latch-up immunity and ensure compliance with performance and reliability targets.

Once Step 5 yields its initial set of results, the methodology specifies that this data, along with the simulation outcomes, should be used as input for the DOE. Depending on how the statistical analysis is structured, layout adjustments may be made (Step 4) or the process may be repeated. This methodology represents a structured approach to optimizing and validating a latch-up protection device at the layout level, employing statistical design techniques and thorough simulation validation.

The physical layout directly impacts the parasitic elements that govern latch-up behavior, such as the effective substrate and well resistances and the coupling between the parasitic bipolar transistors. To comprehensively evaluate latch-up susceptibility and optimize protection strategies, it is essential to understand and quantify the key parameters that influence latch-up triggering and sustainability. All the parameters are illustrated in Figure 3.1 and explained in Table 3.1. By adjusting these structural parameters, one essentially controls how easily the parasitic latch-up path can form. For instance, a wider guard ring provides a lower-resistance path to the supply, thus siphoning off injected current more effectively (increasing the latch-up trigger current required) [14]. A larger spacing between the nMOS and pMOS active regions (with guard rings in between) reduces the coupling between their parasitic transistors [10], but excessively large spacing might not be needed if a guard ring is already catching most carriers. Therefore, finding the minimum acceptable spacing and guard ring width is a matter of balancing these parameters against latch-up susceptibility. Understanding how these variables interact is essential for optimizing latch-up immunity. Implementing a full factorial sweep of all latch-up-related layout parameters in silicon is impractical due to the combinatorial explosion of test structures and limited test chip area. Using a DOE software tool (JMP from SAS [15] in this case), this thesis proposes a disciplined approach to design and analyze latch-up experiments. By using DOE, engineers can derive meaningful conclusions about latch-up protection mechanisms with a minimum set of silicon structures. The result is a data-driven optimization of latch-up design rules, which is particularly valuable in advanced nodes where trade-offs between area and reliability are delicate. The next section will present three layout implementations, based on the first DOE response.

Following the initial DOE iteration described in the previous subsection, three primary structures were selected for the first layout implementation, as outlined in Table 3.1. These included: one structure with all parameters set to the minimum values allowed by foundry design rules, a second structure based on an existing, practically tested I/O driver; and a third structure representing an intermediate configuration between the two. While final latch-up verification must be performed on silicon according to JEDEC JESD78 standards, this thesis demonstrates that simulation plays a crucial role in identifying potential latch-up risks during the design phase. Given the complex 3D

parasitic interactions involved, traditional circuit simulations (e.g., HSPICE) often fall short, as standard PDKs (Process Design Kits) typically omit substrate and parasitic bipolar effects. Advanced methods like TCAD (Technology Computer-Aided Design) offer accurate modeling of latch-up behavior by solving semiconductor transport equations but are limited to small structures due to their high computational demands [16]. To bridge this gap, this research utilized layout-aware tools such as Ansys Totem [17] [18], which can extract substrate resistances and simulate pseudo-latch-up conditions by injecting transient currents at sensitive nodes. Totem enables guard ring effectiveness analysis and layout-based latch-up risk assessment, complementing DRC (Design Rule Checks) [18]. While these simulations do not replace physical testing, they were instrumental in this thesis for validating compact guard ring rules and highlighting weak substrate coupling areas. The simulation results guided design optimizations, ultimately ensuring that the fabricated structures met latch-up immunity requirements during JEDEC-compliant stress testing. This methodology highlights the value of simulation not as a substitute, but as a powerful pre-silicon design assurance strategy.




(a) (b)

***Figure 3.1*** *(a) A simplified schematic of an I/O structure and a principal positioning of the guard rings; (b) Notation and position of each guard ring.*

A key takeaway is the successful application of a Design of Experiment (DOE) methodology to latch-up rule optimization, which allows engineers to systematically explore and refine layout guard ring rules for I/O cells. By using DOE-driven test chips and statistical analysis, one can derive compact layout rules tailored to a specific process – achieving area reduction in I/O structures without compromising on the strict JEDEC latch-up standards [12]. The specific study in 55 nm CMOS demonstrated that substantial reductions in guard ring spacing are possible with no latch-up failures, when the right combination of guard ring width, placement, and other parameters is employed. This methodology, being iterative and data-centric, is a template that can be extended to other technologies and even other reliability concerns.

The current research demonstrates (in an advanced 55 nm CMOS node) how guard ring design and layout rules can be further optimized using a structured Design of Experiment (DOE) methodology. By systematically exploring parameter interactions and layout configurations, this work achieves effective latch-up protection while minimizing area consumption. The novelty lies in applying statistical optimization to a problem

traditionally addressed through empirical or rule-based methods. This chapter has addressed the industry-driven need for enhanced latch-up and ESD robustness in 55 nm CMOS technology node.

***Table 3.1*** *Three layout structures with assigned latch-up parameter values.*

| **Definition** | **Paramenter** | **Layout 1** | **Layout2** | **Layout3** |
|---|---|---|---|---|
| Guard ring widths Tap → inner guard ring; Col → outer guard ring | **GW_p_tap [µm]** | 0.14 | 0.21 | 0.21 |
| | **GW_n_tap [µm]** | 0.14 | 0.46 | 0.46 |
| | **GW_p_col [µm]** | 0.14 | 0.21 | 0.21 |
| | **GW_n_col [µm]** | 0.15 | 0.46 | 0.46 |
| Active to inner guard ring | **Dp [µm]** | 0.32 | 0.32 | 0.32 |
| | **Dn [µm]** | 0.32 | 0.32 | 0.32 |
| Distance from inner to outer guard ring | **Dp0 [µm]** | 0.19 | 0.3 | 0.3 |
| | **Dn0 [µm]** | 0.19 | 0.561 | 0.561 |
| Fingers for each of inverter's transistors | **m_P** | 1 | 1 | 30 |
| | **m_N** | 1 | 1 | 24 |
| Inv1 to inv2 | **D [µm]** | 0.5 | 0.5 | 0.5 |
| Distance p+ to n+ | **S [µm]** | 2.65 | 15.112 | 15.112 |
| | **Area [µm x µm]** | 5.9 x 43.9 | 16.7 x 60.1 | 76.6 x 165.4 |

# Chapter 4

# Experimental Structures for CDM-ESD Robustness Assessment

Studies have shown that CDM failures "often occur at signal interfaces between power domains" [19] if those interfaces lack dedicated protection. Similarly, long or resistive ground networks can exacerbate CDM damage: a high CDM discharge current flowing through a large VSS net resistance induces a significant local ground bounce, overstressing device gates [20]. This work targets improved CDM robustness for two scenarios in a 40 nm CMOS technology. The aim is to: (1) Develop a local CDM protection strategy at a cross-power domain interface using a dedicated device to clamp dangerous voltage differentials (Module 1); (2) Implement a global CDM robustness evaluation strategy for long on-chip wires by quantifying the maximum ground network resistance that still prevents CDM damage (Module 2).

A test-chip approach is used, as circuit simulation tools often cannot accurately predict CDM breakdown in nano-scale devices. The chosen 40 nm test-chip includes structures implementing each strategy. Both modules were fabricated and subjected to standardized CDM testing. The same methodology, illustrated in Figure 4.1, is proposed for both modules. The objective is to validate the protection effectiveness and to extract

design guidelines (optimal device dimensions for cross-domain clamps, and safe ground line resistance limits) that ensure CDM robustness in this technology.

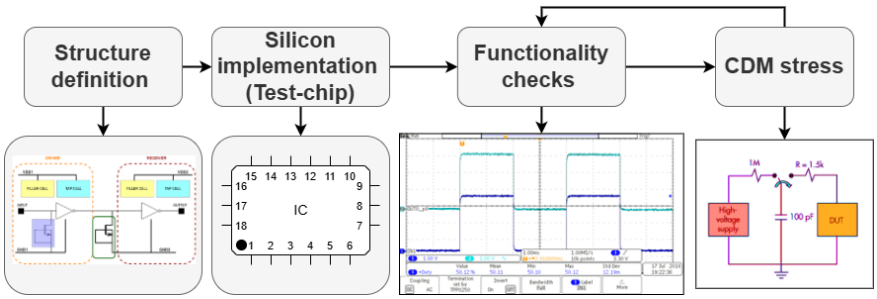



***Figure 4.1*** *Methodology proposed for this research.*

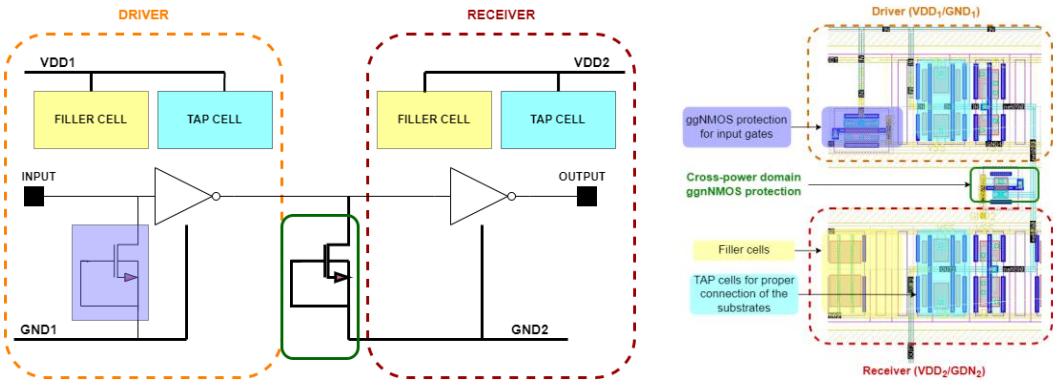
## 4.1 Proposed Architectures

**Cross-power-domain (CPD)** interfaces arise when signal transitions between circuits operating on different supply and ground domains [21]. During a CDM event, mismatched discharge timing between domains can expose thin-oxide gates to damaging voltage differentials. To mitigate this, a grounded-gate nMOS (ggnMOS) device is used in this work as a localized clamp, protecting the receiver's gate oxide by providing a low-impedance discharge path to its ground domain. The study focuses on the most vulnerable CPD configuration—completely separate VDD and VSS domains [21].

To evaluate clamp effectiveness, a dedicated test structure (Module 1) was implemented, consisting of 55 driver-receiver inverter pairs (from separate domains), each protected by a different ggnMOS variant spanning five channel lengths (40–80 nm) and eleven widths (120 nm–1 µm), along with one unprotected reference cell. Each pair forms an independent test cell with a shared input and isolated output. Figure 4.2 illustrates this setup: (a) shows the schematic of a single driver-receiver pair with ggnMOS protection; (b) presents the corresponding layout snippet, where the ggnMOS (highlighted in purple) is placed near the receiver input, and tap/filler cells are shown in yellow and teal; (c) displays the complete 5×11 matrix layout, arranged such that each row represents a constant channel length and each column a constant width. The full matrix measures 38.18 µm × 36.38 µm and enables a systematic, layout-efficient evaluation of ggnMOS sizing impact on CDM robustness.

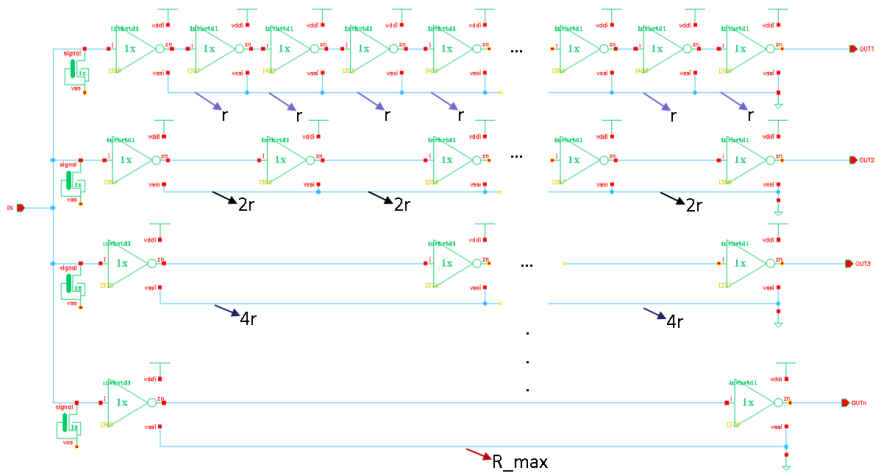
The second challenge investigated in this chapter is the impact of long interconnects and ground (VSS) resistance on CDM robustness. Even within a single power domain, extended or narrow ground paths can cause significant transient voltage drops during a CDM event ($V = I \cdot R$), elevating the local ground potential and exposing downstream gate oxides to damaging overstress [20]. This phenomenon, known as the high D/R (driver/receiver) VSS route problem, becomes increasingly relevant in advanced floorplans with long distribution networks and layout discontinuities. To quantify this effect, **Module 2** was designed to empirically determine the maximum tolerable ground-track resistance in 40 nm technology. The setup—illustrated in Figure 4.3—consists of multiple rows of inverter chains with systematically increasing interconnect resistance. A small ggnMOS clamp is included only at the input of each row to protect the initial gate,

while downstream inverters rely solely on the inherent resistance of the ground path. The resistance-doubling layout allows identification of the failure threshold by observing which outputs fail after CDM stress is applied at the input. This approach isolates the influence of VSS resistance and provides a concrete design guideline for ground network robustness in nanometric nodes [22].

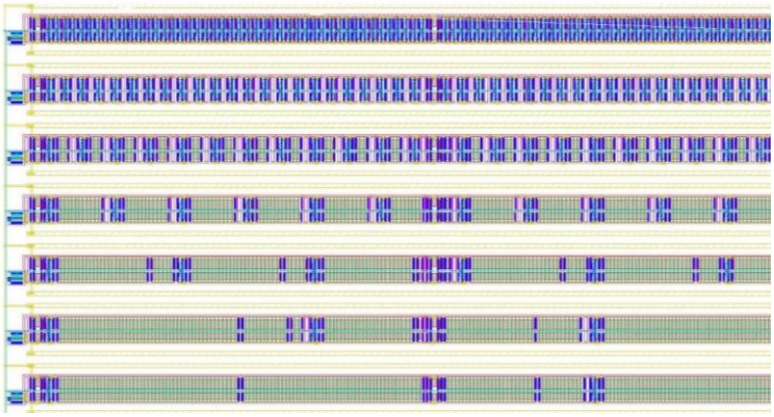



(a)

***Figure 4.2*** *Module 1: (a) Schematic and (b) Layout or one driver-receiver pair.*




(a)



(b)

***Figure 4.3*** *Module 2: Proposed (a) schematic and (b) Layout.*

Table 4.1 summarizes the characteristics of the twelve test rows implemented in Module 2, each designed to evaluate the effect of increasing ground resistance on CDM

robustness. Each row consists of a chain of inverters powered through a supply track of specific length and resistance. The number of inverters decreases progressively as the length and resistance of the VSS line increase, following a resistance-doubling principle. Row 1 begins with 2,346 inverters connected to a short 0.41 µm supply track with 0.57 Ω resistance, while Row 12 contains only 2 inverters connected through a 997.6 µm track with a total resistance of 1,387.17 Ω. This arrangement allows for a systematic investigation of the failure threshold by observing how CDM-induced stress affects functionality across a wide range of ground path resistances. The sharp increase in resistance from one row to the next enables fine granularity in identifying the critical point beyond which CDM failure becomes likely.

Figure 4.4 illustrates the layout for the entire test-chip, containing both proposed modules. Due to the high number of IOs, the package chosen for this testchip is LQFP100 (Low-Profile Quad Flat Package with 100 pins).

***Table 4.1*** *Module 2 design parameters per row.*

| Row number | No. of inverters | Supply track length [µm] | Resistance [Ω] |
|---|---|---|---|
| 1 | 2346 | 0.41 | 0.57 |
| 2 | 1172 | 0.82 | 1.14 |
| ... | | | |
| 12 | 2 | 997.625 | 1387.17 |

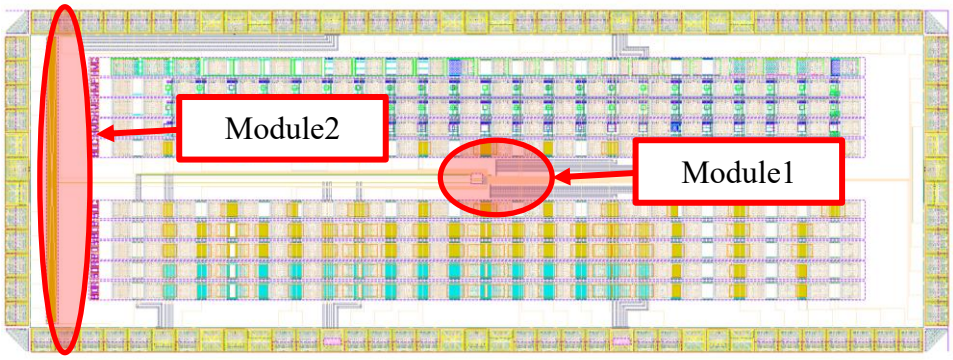



***Figure 4.4*** *Layout implementation of the entire test chip.*

## 4.2 Experimental results

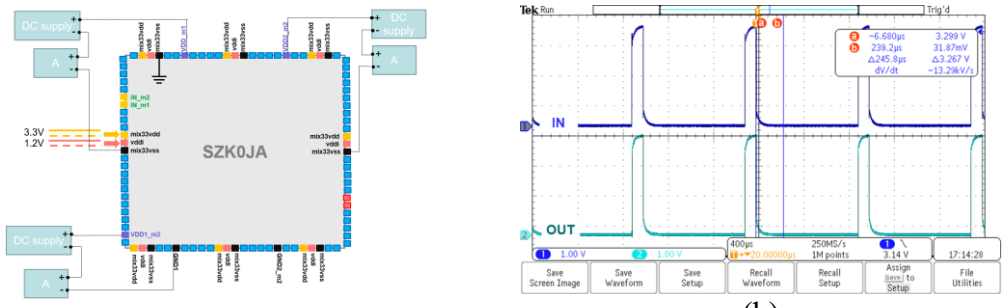
This pre-stress verification confirmed that all test structures in both modules were fully functional under normal operating conditions, ensuring that any subsequent failures could be confidently attributed to CDM stress rather than pre-existing logic or connectivity issues. Figure 4.5 depicts (a) the proposed setup and (b) the oscilloscope capture of functional behavior.

Following pre-stress verification, both Module 1 and Module 2 were subjected to standardized Field-Induced CDM (FICDM) stress tests using the Orion2 system, in accordance with ANSI (American National Standards Institute), ESDA (Electrostatic Discharge Association) [23] [24], JEDEC [11], and AEC (Automotive Electronics Council) [25] guidelines. Stress was applied exclusively through the test-chip's core

supply and ground pins (pin 94 and pin 31, respectively), at four voltage levels: 500 V, 1 kV, 1.5 kV, and 2 kV. Each voltage level was tested on separate samples to isolate single-event effects and avoid cumulative damage. In Module 1, the objective was to observe whether ggnMOS devices effectively protected the receiver input gates during a CDM event, while Module 2 evaluated whether varying ground path resistances led to localized overvoltage and failure. Each pin received three positive zaps per sample, and functionality was re-verified after each stress level. This approach ensured controlled, repeatable CDM exposure and enabled a clear correlation between design parameters and observed failure behavior.

After each CDM stress event, the full set of 55 CPD cells in Module 1 was re-tested for logic functionality using the same procedures outlined in the initial verification phase. To ensure accurate comparison, testing conditions—including equipment, PCB, socket, environment, and personnel—were kept identical. Any deviation in output behavior (e.g., stuck-at faults or waveform distortion) indicated CDM-induced damage.

As expected, the unprotected structure failed, underscoring the necessity of incorporating CDM protection between domains with separate supplies and grounds. Figure 4.6(a) illustrates one typical failure modes: some outputs became completely unresponsive, while Figure 4.6(b) depicts failures that were observed in some ggnMOS-protected cells starting at 500 V: which shows that channel length had a greater influence on CDM robustness than width. Devices with 60–70 nm gate lengths offered optimal protection, while the shortest (40 nm) and longest (80 nm) devices were less effective. Although wider devices generally had little impact, very wide clamps required longer gate lengths to remain functional. Beyond 1 kV, all clamp variants began to fail, with complete breakdown observed by 1500–2000 V—none of the tested ggnMOS sizes could sustain such high CDM levels. These results validate that mid-range channel lengths are most effective for CPD protection in 40 nm CMOS, though even optimized ggnMOS clamps have limits when exposed to extreme CDM stress.

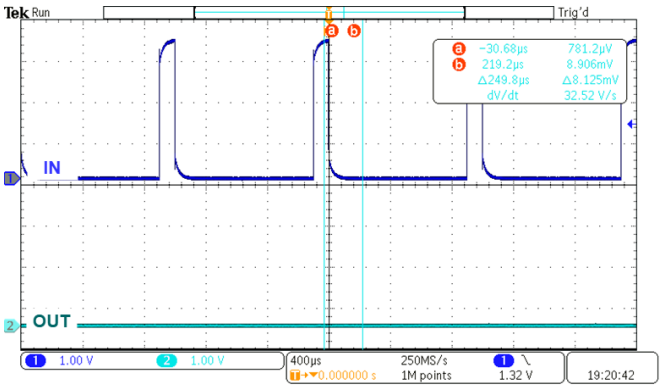



(a) (b)

***Figure 4.5*** *(a) Test setup; (b) Oscilloscope waveforms.*

Post-stress analysis of **Module 2** revealed a clear correlation between ground path resistance and CDM-induced failure. At 500 V stress, even the highest-resistance row (~1.38 kΩ) remained functional. Functional verification across all rows and 13 samples, established that no failures occurred up to 1 kV—validating that even high-resistance paths can tolerate standard CDM levels. However, at 1.5 kV, failures began to appear in both moderate (~1.14 Ω) and high-resistance (~1.38 kΩ) rows, with consistent failure in

the latter at 2 kV. Results indicate a critical ground resistance threshold between ~0.7–1.3 kΩ beyond which CDM robustness deteriorates significantly. These findings confirm that for 40 nm technology, a resistance ≤ 0.7 kΩ ensures 2 kV protection, while up to 1.3 kΩ is acceptable for 1 kV—offering concrete design rules for future power distribution networks.




(a)

| W/L [nm] | 40 | 50 | 60 | 70 | 80 |
|---|---|---|---|---|---|
| 120 | ✗ | ✓ | ✓ | ✓ | ✗ |
| 200 | ✗ | ✓ | ✓ | ✓ | ✗ |
| 300 | ✓ | ✗ | ✓ | ✓ | ✗ |
| 400 | ✓ | ✓ | ✓ | ✓ | ✗ |
| 500 | ✓ | ✓ | ✓ | ✓ | ✗ |
| 600 | ✗ | ✗ | ✗ | ✓ | ✓ |
| 700 | ✗ | ✗ | ✓ | ✓ | ✓ |
| 800 | ✗ | ✗ | ✓ | ✓ | ✓ |
| 900 | ✗ | ✗ | ✓ | ✓ | ✓ |
| 1000 | ✗ | ✗ | ✓ | ✓ | ✗ |

(b)

***Figure 4.6*** *(a) Functionality tests for Module 1 performed on one sample after CDM stress. Transient waveforms after stress at 2000 V stress (W=1000nm; L=40nm); (b) Results after CDM-ESD at 500V stress.*

**Module 1**: The CPD protection study provided a clear design guideline: to ensure robustness against standard 500 V CDM stress in 40 nm technology, the ggnMOS clamp should have a channel length of at least 1.5× the minimum (i.e., ≥60 nm if L_min = 40 nm). Devices with longer channel lengths (60–80 nm) remained functional even at minimum width, while those with 40 nm lengths showed occasional failures at small widths, indicating that short-channel effects reduce effectiveness. Although increasing width offered little benefit at 500 V, it contributed to resilience at higher stress levels by supporting greater current conduction. Therefore, a conservative design might select a ggnMOS with ~60 nm length and moderate width (0.5–1 µm) for margin. However, protection beyond 500 V is unrealistic in this configuration—no ggnMOS variant prevented failure at 1 kV or above—highlighting the need for advanced techniques outside this study's scope to meet higher CDM targets. These findings refine earlier CPD protection recommendations by quantifying behavior specifically in 40 nm nodes. Table 4.3 compares the results from Module 1 with prior studies, offering a comprehensive overview of ESD protection strategies across different nodes, devices, and methodologies. While previous works such as [19] , [26] , [27] and [28] explored ggnMOS or GCT-nMOS protections using vf-TLP or MM stress (typically ≤750 V), and [29], [30], [31] examined RC clamps or distributed protections at similar stress levels, none combined ggnMOS-based protection, FICDM methodology, and testing up to 2000 V in a 40 nm cross-domain interface. Notably, [31] explored FICDM in 180 nm with capacitive decoupling, and [30] assessed non-pad-based protection at 45 nm, but neither addressed the combined criteria met in this work. This thesis fills a critical research gap

by demonstrating that ggnMOS protection—properly designed and placed between domains—can maintain CDM robustness under severe stress using advanced FICDM techniques.

**Module 2**: The results of the long-wire module establish a clear CDM safe-operating area for ground resistance in 40 nm technology. For standard CDM requirements (500–1000 V), designs can tolerate up to ~1.3 kΩ of ground resistance, while achieving higher robustness (≥2 kV) necessitates reducing resistance to ≤600–700 Ω. Practically, this translates to limiting ground line lengths to ~500 µm for minimum-width metal or employing wider/thicker routing and additional vias. The consistent failure of the highest-resistance row (1.38 kΩ) at 2 kV, despite passing at 1 kV, highlights the nonlinear nature of CDM-induced gate breakdown once a critical ground bounce voltage is exceeded. These findings align with oxide breakdown physics and support actionable design rules—such as specifying a maximum allowable impedance between any two ground points—to control on-chip CDM vulnerability. Table 4.2 compares this study's findings to similar works [32] [33] [34] [35] across various nodes, packaging types, and stress methods. While prior studies often focused on older nodes (e.g., 130 nm, 90 nm) or used less rigorous testing (e.g., vf-TLP), this work stands out by validating CDM robustness at 40 nm using FICDM, a more accurate, field-representative method. Despite the sensitivity of 40 nm technologies, this study demonstrates comparable or better tolerance than earlier nodes, proving that with careful ground routing, strong CDM protection is still achievable. These findings address an important omission in the existing literature and offer practical, forward-looking guidelines for ESD-aware floor planning.

In conclusion, this chapter presented two complementary strategies to enhance CDM-ESD robustness in advanced 40 nm CMOS I/O structures. The comparative results highlight this study's novelty in combining aggressive 40 nm scaling, ggnMOS-based CPD protection, and high-voltage FICDM testing. The methodologies and test structures used here were previously peer-reviewed and published [22] [36] , laying the foundation for the extended analysis in this thesis. These contributions have already influenced internal design practices for 40 nm I/O libraries and inform automated EDA (Electronic Design Automation) verification flows. In conclusion, this chapter bridges the gap between circuit-level ESD strategies and full-chip CDM reliability by offering practical, experimentally validated design rules that can guide robust ESD protection in nanometric CMOS nodes. The next chapter builds on this foundation by transitioning to 28 nm technology and introducing vf-TLP methodology for more granular, waveform-level analysis of CDM stress response.

***Table 4.2*** *Performance analysis with similar studies for long wires module.*

| Other Studies | Technology Node | Package Used | CDM Stress Method | CDM Stress Voltage | Maximum Ground Wire Resistance |
|---|---|---|---|---|---|
| [32] | 250 nm | LQFP64 | vf-TLP | 750 V | 1 kΩ |
| [33] | - | CDIP | vf-TLP | 750 V | 5.8 kΩ |
| [34] | 130 nm | Flip-chip | - | 500 V | 1.5 Ω |
| [35] | 90 nm | BGA | - | 600 V | 600 Ω |
| **This paper** | 40 nm | LQFP100 | FICDM | 1 kV | 1.3 kΩ |

***Table 4.3*** *Performance analysis with similar studies for Cross Power Domain module.*

| Other studies | Technology node | Protection device | Stress Voltage | Stress Method |
|---|---|---|---|---|
| [19] | - | ggnMOS | 750V CDM | vf-TLP |
| [26] | 180 nm | Stacking MOS | 500V CDM | vf-TLP |
| [27] | 90 nm | GCT-nMOS | 500V MM | TLP |
| [28] | 130 nm | GCT-nMOS | 400V MM | TLP |
| [29] | 40 nm | RC-Clamp | 500V CDM | TLP |
| [31] | 180 nm | Decoupling capacitors | 500V CDM | FICDM |
| [30] | 45 nm | Internally distributed protection | 500V CDM | vf-TLP |
| **This paper** | 40 nm | ggnMOS | 2000V CDM | FICDM |

# Chapter 5

# Transient-Based Assessment of CDM-ESD Protection Methods

This chapter advances the ESD evaluation framework by shifting focus to the 28 nm technology node, where finer geometries and thinner gate oxides introduce new challenges for CDM-ESD protection. Building on the 40 nm study that utilized fixed-layout structures and pass/fail FICDM testing, this chapter introduces a transient-based characterization methodology using vf-TLP, which offers high-resolution insights into voltage and current behavior during fast CDM-like events. A generalized and flexible test structure is proposed to accommodate various stress configurations, with particular emphasis on long metal interconnections—known contributors to ESD vulnerability due to parasitic resistance and voltage peaking. This work is grounded in the peer-reviewed study by Dobre et al. [36], which introduced the methodology and was presented at an international conference, affirming its technical relevance. The 28 nm node, while offering enhanced performance and power efficiency, presents increased susceptibility to ESD due to reduced junction depths, narrower interconnect spacing, and thinner gate oxides [37] [38], making traditional protection schemes less effective. Moreover, CDM-specific issues such as transient overshoots [39] modeling limitations [40], and packaging-related parasitics [41] further complicate protection strategies. As highlighted by recent industry recommendations [37] [42] [43], updated standards and co-design methodologies are necessary to ensure system-level robustness.

As CMOS technologies scale to 28 nm and beyond, traditional CDM-ESD protection strategies struggle to address increased risks from thinner gate oxides and long interconnect parasitics. This chapter responds to those challenges by introducing a

transient-based validation methodology using vf-TLP, enabling detailed analysis of voltage and current behavior during CDM-like events. A generalized test structure is proposed to emulate long-routing stress scenarios, and various protection devices—such as trio-diodes, duo diodes and ggnMOS—are evaluated on silicon. Building on the peer-reviewed 2022 study by Dobre et al., this work aims to uncover critical failure mechanisms and provide actionable design insights for more robust CDM protection in advanced nodes.

## 5.1 Proposed On-Silicon Validation

This chapter introduces a versatile architecture for validating CDM-ESD protections in 28 nm technology, specifically under scenarios involving long metal interconnections between driver and receiver. The proposed structure allows for controlled application of CDM stress across various discharge paths using four accessible pads, emulating real-world CDM events with high configurability. The validation method includes three protection types—no protection, diode-based (double and trio), and grounded-gate nMOS (ggnMOS)—with ggnMOS variations implemented across different geometries for comprehensive analysis.

A key novelty lies in the structure's ability to replicate all potential CDM scenarios via configurable discharge paths, monitored through key voltage nodes (V12, V34, Vs) and series resistors that mimic parasitic effects. The testing leverages vf-TLP rather than FICDM, providing finer granularity into transient behavior, clamping performance, and stress localization—filling a gap left by pass/fail methods used in Chapter 4. Figure 5.1 highlights oxide stress voltage conditions under various pad-to-pad stress directions, with precise voltage drops calculated to identify real stress scenarios. The test plan ensures all combinations of protection structures are evaluated under realistic CDM conditions. This approach offers an accurate, silicon-based validation technique essential for guiding protection strategies in advanced CMOS nodes.

| CDM stress [10Amps] | | V12 [V] | V34 [V] | Vs [V] |
|---|---|---|---|---|
| (+) | (-) | | | |
| **1** | **2** | 4.9 | 0.6 | 4 |
| **1** | **3** | 2 | 2 | 4 |
| **1** | **4** | **2.5** | **2.5** | **7.5** |
| **2** | **4** | 3 | 2 | 6 |
| **3** | **1** | 2 | 2 | 4 |
| **4** | **1** | 2.5 | 2.5 | 7.5 |
| **4** | **2** | 3 | 2 | 6 |

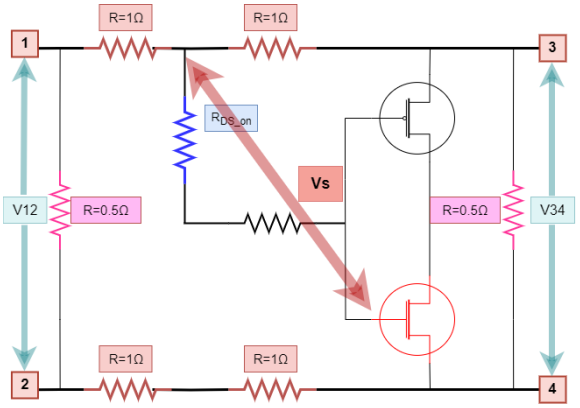



***Figure 5.1*** *Driver-receiver pair when the driver is connected to ground: nMOS oxide of the receiver is affected by the CDM stress depicted in the table.*

After layout and silicon implementation, all CDM-ESD protection structures were characterized using vf-TLP, which offers detailed transient I-V behavior. The vf-TLP setup applies fast-rising pulses (e.g., 10 ns pulse width, 100 ps rise time), enabling analysis of peak current, voltage, and failure thresholds. Measurements average

waveform responses to derive accurate I-V curves and detect failures via abrupt leakage increases.

Results showed linear resistive behavior up to a distinct inflexion point—beyond which devices exhibited open-circuit traits, indicating failure. Notably, Figure 5.2 compares structures with and without ggnMOS protection, showing improved current tolerance for certain stress paths. These insights reveal not only the limited influence of CDM protection devices in specific routing configurations but also suggest potential backend metallization issues as failure origins, underscoring vf-TLP's value in identifying subtle failure mechanisms in nanometric technologies.

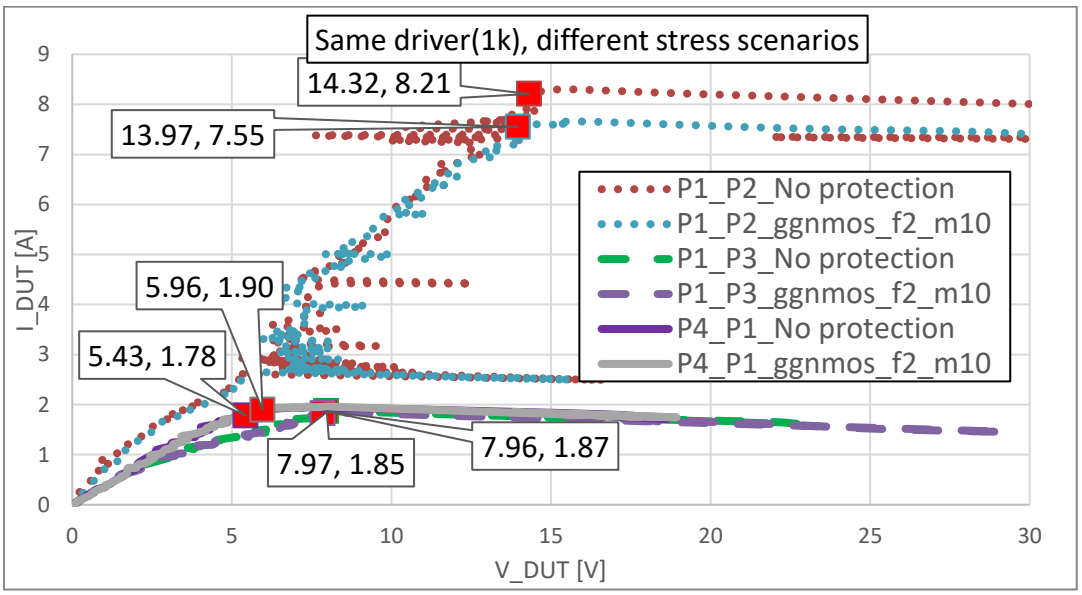



***Figure 5.2*** *Current-Voltage waveform characteristics after vf-TLP.*

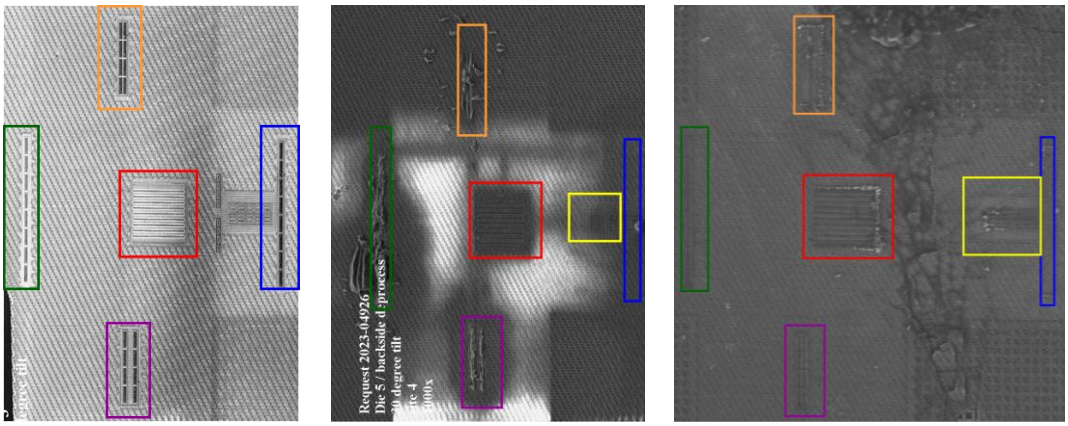
## 5.2 Failure analysis

The failure analysis following vf-TLP stress involved two main cases—(A) P1 to P2 (no receiver damage expected) and (B) P1 to P3 (receiver pMOS oxide stress expected)—each examined under two stress levels: (a) limited to 1.5A and (b) up to the current inflexion point (~7.5A or ~1.8A). Table 5.1 summarizes observed failures after 1.5A stress. Figure 5.3 presents SEM (Scanning Electron Microscopy) images revealing localized damage primarily in the 2Ω resistors, indicating routing vulnerability rather than protection device limitations. Structure 4, with dual diode protection and driver tied to power, showed no damage—unlike others, where failures were inconsistent and not strongly correlated to the type of protection. However, stress up to the inflexion point resulted in catastrophic failure across all elements confirming the initial assumption that metallization, not protection device type, dominated failure behavior. In Case B (P1 to P3), Figure 5.3 (b) shows extensive damage in the unprotected structure with driver connected to power. The results for this: Structure 5 (unprotected, driver to power) suffered the most severe damage (four elements failed), while Structures 1 and 3 (grounded drivers with no or dual diode protection) were least affected. As stress exceeded 1.8A, all structures experienced thermal runaway and complete failure. These

observations confirm that certain components—especially the receiver, 2Ω top resistor, and 1kΩ driver resistor—are particularly susceptible to CDM-ESD stress. While trio diode and ggnMOS protections offer moderate resilience, they do not fully prevent damage, reinforcing the need for optimized design and material selection in future nanoscale ESD protection schemes.

***Table 5.1*** *Pass/Fail results after stress from P1 to P2 up to 1.5A and FA*

| No. | Structure | 2Ω bottom resistor | 2Ω top resistor | 0.5Ω left resistor | 0.5Ω right resistor | 1kΩ driver resistor | Receiver |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| 1 | NM_diode | ✗ | ✗ | ✗ | ✗ | ✓ | ✓ |
| 2 | NM_ggnMOS | ✗ | ✗ | ✓ | ✓ | ✓ | ✓ |
| 3 | PM_no_protection | ✗ | ✗ | ✗ | ✓ | ✓ | ✗ |
| **4** | **PM_diode** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 5 | **PM_ggnMOS** | ✗ | ✗ | ✓ | ✓ | ✗ | ✗ |



(a) (b) (c)

***Figure 5.3*** *Damage suffered from the structure (driver connected to ground) protected with duo-diode when the stress was applied from (a)/(b) P1 to P2 (no oxide damage) up until: the current reached 1.5A/shifted; (c)P1 to P3 1.5A.*

This study highlights the need for optimized CDM-ESD protection and improved routing to prevent failure, especially in vulnerable metal paths. It reveals that standard 2 µm metal widths are insufficient under CDM stress and should be increased. Additionally, introducing a fifth bonding pad would enable more accurate leakage monitoring during vf-TLP, helping to detect oxide damage thresholds without requiring failure analysis, thus streamlining protection evaluation in advanced nodes.

## 5.3 Deriving Insights from vf-TLP Data

This section explores deeper insights from vf-TLP waveform data to better understand CDM-ESD protection behavior in advanced nanometric technologies. While no clear "best" protection device emerged from standard pass/fail testing, vf-TLP waveform analysis—including I-V curves, voltage/current transients, and energy dissipation—reveals critical failure dynamics and highlights the influence of averaging windows and

stress directionality. Figure 5.4 shows that adjusting the averaging window significantly affects extracted I-V characteristics, especially in the early transient phase where current is still rising. Figure 5.5 compares decoupling capacitance values under different stress directionalities, showing consistently higher capacitance for P1-P2 stress, which correlates with better robustness and higher I/V thresholds before failure. Although protection type alone does not determine decoupling behavior, the stress path plays a major role in shaping waveform and energy responses. Overall, this analysis confirms that decoupling capacitance and transient waveform behavior—rather than static protection type alone—are key indicators of CDM-ESD robustness. Time-domain waveform data enables detection of subtle differences in protection efficiency and failure onset, supporting a more precise and predictive co-design strategy for CDM resilience in 28 nm CMOS technologies.

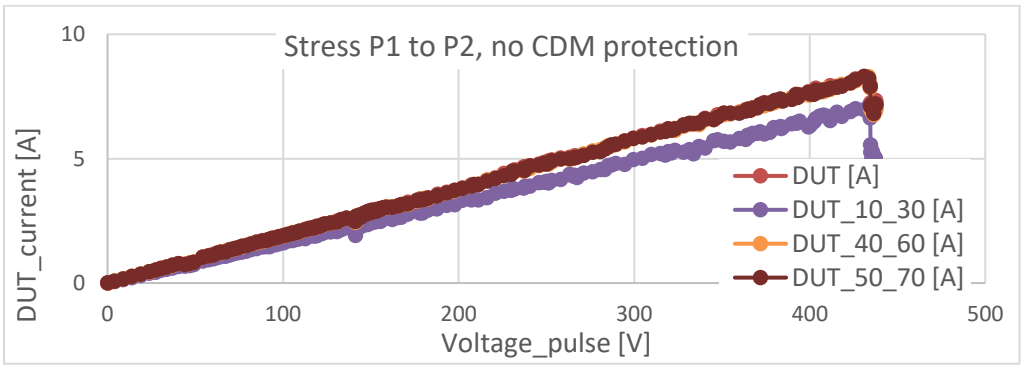



***Figure 5.4*** *Various average windows considered dependent of the voltage pulse.*

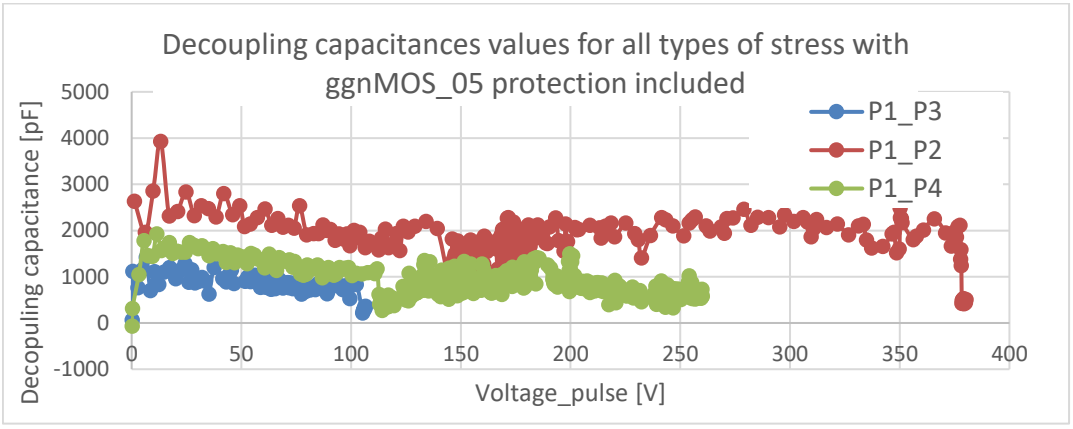



***Figure 5.5*** *Decoupling capacitance values.*

This chapter introduced a novel transient-based methodology using vf-TLP to assess CDM-ESD protection schemes in 28 nm technology, offering a significant advancement over traditional pass/fail FI-CDM testing. By enabling detailed waveform analysis and emulating multiple stress scenarios within a single layout, especially those involving long metal interconnects—this study uncovered critical insights into failure mechanisms, energy accumulation, and the role of decoupling capacitance. The methodology forms a foundation for improved ESD co-design practices, with ongoing work set to enhance test structures, refine routing, and explore additional protection devices for even greater reliability in nanometric nodes.

# Chapter 6

# Conclusion

## 6.1 Objectives, Results and Original Contribbutions

The core objective of this thesis is to develop and validate robust protection methodologies for two major reliability concerns in advanced CMOS technologies: Electrostatic Discharge (ESD)—with a focus on Charged Device Model (CDM)—and latch-up phenomena. As CMOS nodes scale to 55 nm, 40 nm, and 28 nm, traditional protection schemes become less effective due to smaller geometries and higher current densities, demanding new architectures and validation strategies. Driven by both industrial needs and research gaps, this work proposes optimized, scalable protection solutions supported by silicon validation and targeted test structures. The methodology combines analytical modeling, layout optimization, and experimental evaluation to ensure reliability with minimal design overhead. This involved:

- Establishing methodologies for compact guard ring design to mitigate latch-up while reducing I/O cell area.
- Characterizing grounded gate nMOS (ggnMOS) devices under varying geometries and CDM stress conditions to define reliable design rules in 40 nm technology.
- Quantifying the impact of ground-bus resistance on CDM protection efficiency, culminating in layout-aware design guidelines.
- Investigating oxide failures in 28 nm technologies under CDM stress, especially in long-wire interconnect scenarios, and evaluating diode-based versus ggnMOS protection topologies.
- Utilizing statistical frameworks like Design of Experiment (DOE) to intelligently sample and optimize large parameter spaces, thereby accelerating the convergence toward robust design solutions.

By bridging the gap between design rule constraints, device physics, and system-level integration, this research contributes significantly to the field of ESD and latch-up reliability. The insights provided are directly applicable to IC designers working in the 55 nm to 28 nm range, and the methodologies can be extended to future nodes, with appropriate adjustments. This thesis thus provides both immediate solutions and a strategic foundation for ongoing innovation in semiconductor reliability

The core original contributions of the thesis are concentrated in Chapters 3 through 5, each addressing critical limitations in modern CMOS reliability and culminating in experimentally validated protection strategies. The findings have been documented and published in a series of original papers, listed as references [1] to [7] in Subchapter 6.3, and attributed to the respective contributions below.

**A Methodology for Latch-up Rule Definition** [1-3]

Chapter 3 introduced a structured approach to optimize latch-up protection in I/O cells by applying Design of Experiment (DOE) techniques to analyze and refine guard ring configurations. The methodology allowed systematic variation of foundry-defined guard ring parameters—such as implant widths and spacing—resulting in a set of compact layout rules that maintained JEDEC-compliant latch-up immunity while significantly reducing the silicon area. Beyond its immediate benefits for area efficiency, the method establishes a scalable and repeatable flow that can be adapted across different submicron nodes. These contributions are particularly valuable as latch-up protection consumes a growing proportion of layout area in modern high-density I/O designs [1-3].

**Experimental Structures for CDM-ESD Robustness in Cross-Power Domains [5]**

To address the increased sensitivity of nanometric circuits to CDM events—particularly at domain boundaries [4] —this work introduced (in Chapter 4) specialized test structures for evaluating grounded-gate nMOS (ggnMOS) protection devices in cross-power domain scenarios. A systematic study was conducted across multiple geometries (55 different structures) and CDM stress levels (from 500V up to 2000V) in 40 nm CMOS, leading to quantitative design recommendations, such as increasing the ggnMOS channel length by ~50% over the minimum (≥60 nm) for reliable operation (up to 500V CDM). The results demonstrated that even minimal device adjustments can significantly enhance protection at domain crossings. The findings were validated using Field-Induced CDM (FICDM) testing, ensuring both the functional relevance and robustness of the proposed protection methodology [1] [2] [4] [5].

**Investigation of CDM Robustness in Extended Metal Routing [6]**

A second major contribution in Chapter 4 involved the design and testing of experimental structures aimed at assessing CDM susceptibility along extended on-chip interconnects [6]. By varying ground track lengths and resistances, the study revealed a clear correlation between CDM failure thresholds and ground resistance, identifying critical resistance values above which CDM-induced failures consistently occurred. To reliably sustain CDM levels up to 1 kV, ground resistance should be kept below ~1.3 kΩ, and for 2 kV, below ~0.7 kΩ. This insight led to concrete layout and routing guidelines to minimize ground impedance in large or distributed circuits. The use of FICDM provided precise stress control and repeatability, confirming the importance of maintaining ground resistance below defined thresholds to ensure reliable CDM immunity in 40 nm ICs [2] [6].

**Transient-Based Assessment of CDM-ESD Protection Methods** [7]

Chapter 5 focused on thin-oxide vulnerabilities in 28 nm CMOS technologies, where traditional ESD protection methods become insufficient. A novel validation technique was developed for evaluating CDM stress in long metal interconnect scenarios—a critical issue in high-performance ICs with extended driver-receiver connections [7]. Through both simulation and silicon implementation, the study defined the failure thresholds associated with increasing ground path resistance, effectively linking layout-induced parasitics to oxide reliability. Experimental results demonstrated how failures correlate with ground wire resistance, leading to practical guidelines for safe wire routing and layout practices in advanced nodes. Additionally, protection topologies using diode-based

and ggnMOS configurations were directly compared, providing insights into the trade-offs between protection strength, leakage behavior, and physical implementation [1] [2] [7].

These contributions advance latch-up and CDM-ESD protection by providing scalable, area-efficient solutions aligned with modern IC design needs. Validated through simulation and silicon implementation, the proposed methods are both practical and adopted in real designs at 55 nm, 40 nm, and 28 nm nodes. Published in peer-reviewed venues, they now support robust IC development and serve as design frameworks for future semiconductor technologies.

## 6.2 List of Original Publications

The findings presented in this thesis are based on the following publications:

[1] **M. -D. Dobre** and G. Brezeanu, "Pad cells performances in submicron technologies," in Proceedings of the 39th International Semiconductor Conference (CAS), Sinaia, Romania, 2016, pp. 205-208, doi: 10.1109/SMICND.2016.7783087. ISBN 978-1-5090-1207-7. ISSN 1545-827X. (Indexed in Web of Science, WOS: 000391323300042).

[2] **M. -D. Dobre**, P. Coll and G. Brezeanu, "I/O library comparison methodology for 40nm CMOS technology," in Proceedings of the 40th International Semiconductor Conference (CAS), Sinaia, Romania, 2017, pp. 183-186, doi: 10.1109/SMICND.2017.8101194. ISBN 978-1-5090-3985-2. ISSN 1545-827X. (Indexed in Web of Science, WOS: 000425844500038).

[3] **M. -D. Dobre**, P. Coll and G. Brezeanu, "I/O Cells Latchup Immunity: Methodology for Compact Layout Rules in an Advanced CMOS Technology," in Proceedings of the 43rd International Semiconductor Conference (CAS), Sinaia, Romania, 2020, pp. 115-118, doi: 10.1109/CAS50358.2020.9268033. ISBN 978-1-7281-1073-8. ISSN 1545-827X (Indexed in Web of Science, WOS: 0006372646000262).

[4] R. -V. Petrica, **M. -D. Dobre**, P. Coll, F. Draghici and G. Brezeanu, "Comparison of Level Shifter Architectures: Application to I/O Cell," in Proceedings of the 41st International Semiconductor Conference (CAS), Sinaia, Romania, 2018, pp. 209-212, doi: 10.1109/SMICND.2018.8539796. ISBN 978-1-5386-4482-9. (Indexed in Web of Science, WOS: 000514386700041).

[5] **M. -D. Dobre**, P. Coll and G. Brezeanu, "A Study on ESD-CDM Cross-Power Domain Failures," in Proceedings of the 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Villasimius, SU, Italy, 2022, pp. 21-24, doi: 10.1109/PRIME55000.2022.9816786. ISBN 978-1-6654-6700-1 (Indexed in Web of Science, WOS:000945853500032).

[6] **M.-D. Dobre**, P. Coll, and G. Brezeanu, “CDM protection test structure for I/O cells in a submicronic technology”, in Electronics Journal, vol. 10, no. 4, art. no. 443, Feb. 2021. doi: 10.3390/electronics10040443. ISSN 2079-9292. (Indexed in Web of Science, WOS:00062338340000, Q2 Journal).

[7] **M. -D. Dobre**, P. Coll and G. Brezeanu, "Validation Technique for Thin Oxide CDM Protections," in Proceedings of the 45th International Semiconductor Conference

(CAS), Poiana Brasov, Romania, 2022, pp. 131-134, doi: 10.1109/CAS56377.2022.9934740. ISBN 978-1-6654-5256-4. ISSN 1545-827X. (Indexed in IEEE Xplore Digital Library).

[8] **M. -D. Dobre**, C.-Y. Chang, C.-K. Chen, P. Coll and G. Brezeanu, "On-Silicon Characterization of CDM-Like Stress in Long Interconnects Using vf-TLP in Nanometric ICs " – accepted to be published in IEEE Transactions on Device and Materials Reliability (Q2 Journal).

Papers [1]–[3] laid the foundation for the direction and relevance of this thesis, addressing latch-up and ESD phenomena within I/O cells. Papers [1] and [2] established a baseline through simulation and characterization of full I/O libraries in submicron technologies, while Paper [3] focused on level shifter design—key to interfacing different voltage domains and central to the CDM-ESD strategies discussed in Chapter 4. Chapter 3 is supported by Paper [4], where the latch-up protection methodology was first validated. Journal Publication [5] introduced the silicon testing framework used to assess long interconnects under CDM-ESD stress in 40 nm, while Paper [6] extended this by fully characterizing Module 1. Papers [7] and [8] addressed CDM-ESD evaluation at 28 nm, proposing a modular test architecture for analyzing protection schemes against interconnect-related vulnerabilities. Collectively, these papers—cited seven times in IC robustness literature—demonstrate the thesis's contribution to ESD and reliability research.

## 6.3 Future Work

Although the methodologies and architectures proposed in this thesis have addressed key reliability issues in scaled CMOS technologies, ongoing challenges and potential research directions remain:

- Re-iteration of 28 nm CDM-ESD Protection Testing: Future work will include a new iteration of CDM-ESD protection testing in 28 nm technology, as no definitive correlation has yet been established between the type of protection device (diode or ggnMOS) and its geometry with respect to CDM robustness. This next phase will build upon the key findings of the current study, specifically by implementing improved routing strategies to eliminate CDM-induced damage paths and integrating an additional bonding pad dedicated to accurate leakage current monitoring.
- Process Scaling Adaptation: As the industry transitions towards 7 nm and beyond, additional parasitic and variability effects are expected. Extension of the latch-up immunity and CDM protection methodologies to FinFET and GAA-based technologies will be necessary.
- Full-Chip CDM Modeling: Future work should involve the integration of CDM protection analysis into full-chip ESD simulations. Advanced modeling platforms capable of accounting for layout-dependent effects and parasitic ground distribution will enhance prediction accuracy.

- Automated Design Tools: The implementation of the developed DOE-based latch-up immunity flow into EDA tools would greatly benefit IC layout designers by providing real-time feedback on protection rule compliance.
- Adaptive Protection Devices: Research into adaptive or smart protection circuits that can dynamically adjust to environmental or operational changes (temperature, voltage fluctuations) could further enhance robustness without incurring area or power penalties.

In conclusion, this thesis provides a foundation for robust ESD and latch-up protection in nanometric CMOS nodes, offering both theoretical frameworks and validated implementation strategies. The methodologies and architectures introduced herein contribute directly to enhancing IC reliability in advanced semiconductor manufacturing.

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