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Doctoral School of Electronics, Telecommunications and Information Technology

Ph.D. THESIS SUMMARY

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PRECISION CIRCUITS FOR CURRENT MEASUREMENT AND CONTROL

CIRCUITE DE PRECIZIE PENTRU MĂSURAREA ȘI CONTROLUL CURENTULUI

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Table of Contents

Chapter 1

Introduction

1.1. General Context of the Thesis

The title of the thesis, *"Precision Analog Circuits for Current Measurement and Control"*, directly reflects the structure and content of the work. The current measurement component is addressed through the design and characterization of current sense amplifiers (CSA). Current control is treated along two complementary paths: on one hand, in gate driver (GD) circuits, where maintaining a constant output current despite supply variations is essential [1]; on the other hand, in temperature sensors based on Schottky diodes on SiC, where precise control of the diode's bias current is required to ensure accurate temperature sensing [2]. Thus, the thesis integrates, in a unified framework, circuits that handle both signal acquisition, as well as active control functions, across diverse and critical application contexts.

1.2. Motivation of the Thesis

The results presented in this thesis are the outcome of several years of research and development activity, reflecting the professional path of a design engineer committed to both scientific rigor and the concrete demands of the semiconductor industry. The work combines the author's inclination toward critical thinking and analytical depth with the pragmatism required in real-world industrial projects, where quick problem-solving and adaptability are essential.

This fusion between fundamental research and practical implementation validates both the scientific relevance and the technological impact of the results, justifying the multidirectional approach adopted in this doctoral research.

1.3. Structure of the Thesis

The thesis is organized into six chapters. In addition to the introductory and final chapters, which provide context and general conclusions, the work includes four substantial chapters that reflect both the theoretical foundations and the author's original contributions.

Chapter 2

Theory and Principles of Current Measurement and Control

2.1. Introduction

Precision analog circuits play a critical role in a wide range of industrial applications, particularly in scenarios requiring the measurement or control of small signals under harsh environmental conditions. The architecture shown in Figure 2.1 illustrates a typical electric motor control system [3].

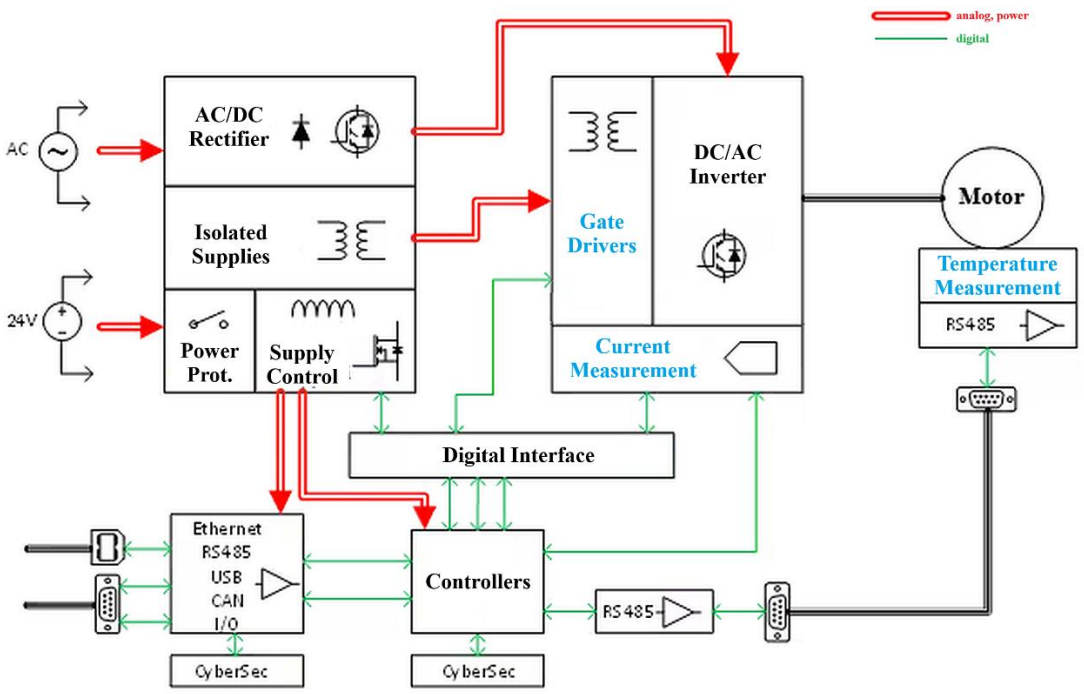

Figure 2.1. *Architecture of a typical electric motor control system [3]*

In addition to the standard power conversion and switching blocks, three key technological directions – highlighted in blue in Figure 2.1 – are essential for the system's performance, safety, and efficiency [4]:

- **Current measurement**, crucial for real-time motor control, overcurrent protection, and energy efficiency;
- **Gate driver circuits (GD)**, responsible for controlling the power transistors;
- **Temperature sensing**, integrated near the motor, critical for overheating detection and thermal compensation algorithms.

2.2. Principles and Topologies for Electric Current Measurement

This subsection provides a progressive structure of the content, starting with a general overview of the main current measurement techniques found in the literature, followed by a detailed rationale for selecting the shunt resistor method (R_{SENSE} technique, using a current sense amplifier) as the most suitable for the analyzed applications. After justifying this choice, the discussion moves to the theoretical aspects specific to this method, including the design requirements for current sense amplifiers and the key parameters relevant for precision, stability, and compatibility with automotive applications. This structure offers the conceptual framework needed to introduce, in the following chapter, a concrete CSA architecture based on the R_{SENSE} technique and optimized for high-precision automotive use.

2.3. Gate Drivers for Power Switches

Gate drivers (GD), are specialized functional blocks that manage the switching of power transistors by ensuring proper charging and discharging of the gate capacitance. These circuits are essential for fast, efficient, and safe switching of MOS or IGBT devices in static power conversion, motor drives, and energy control applications [5]–[8], as also illustrated in Figure 2.1. This paragraph focuses on CGD implementations for controlling n-MOS transistors and presents the main gate driver types: hard-switching gate drivers (HS-GD) and current source gate drivers (CS-GD). Additionally, the superior electromagnetic compatibility (EMC) performance of current source gate drivers is highlighted, which justifies the exclusive focus on this family of drivers in Chapter 4.

2.4. Bias Current Control in Semiconductor-Based Sensors

Precise control of electric current is a key requirement in both measurement and actuation circuits, and applications involving semiconductor sensors are no exception [2], [9]–[11]. Within the context of this thesis – focused on the design of precision analog circuits for current measurement and control – the biasing of sensors, meaning the application of a stable and well-controlled current, becomes a central topic. This subsection naturally fits within the theoretical chapter, as it explores in detail how the bias current directly influences the accuracy and reproducibility of the sensor's output.

Chapter 3

Precision Current Sense Amplifier with Disable Function and Resistive Network Trimming (CSA-DF-RNT)

3.1. Introduction

The structure of this chapter is as follows: in the first part, the functional requirements and target performance metrics for such a circuit will be defined, followed by the proposal of a general block diagram that is common to both architectures presented later. Based on this block diagram, two implementations of the CSA are developed, both relying on the same operating principles, but differing significantly in the way the shutdown function and the fine adjustment of the resistive network are implemented..

3.2. Specifications. Block Diagram

The specifications presented in Table 3.1 have been established for the CSA's typical operating conditions.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Common Mode Rejection Ratio	CMRR	Câștig (G) = 50V/V	-2		2	µV/V
			-4		**4**	
Offset Voltage Referred to Input	V_{OS}	G = 50V/V	-15		15	µV
Power Supply Rejection Ratio	PSRR	G = 50V/V		±0.1	±10	µV/V
Input Bias Current in Active Mode	I_{IB}			35	40	µA
Input Bias Current in Shutdown	I_{IBSD}				**500**	nA
Gain Error	GE			±0.2	**±0.3**	%
Quiescent Current	I_Q			45		µA
					50	
Quiescent Current in Shutdown	I_{QSD}			0.2	0.3	µA

Table 3.1. *Main specifications of the CSA-DF-RNT* [12]

In order to fulfill the specifications listed in Table 3.1, the general architecture illustrated in Figure 3.1 [13] was adopted.

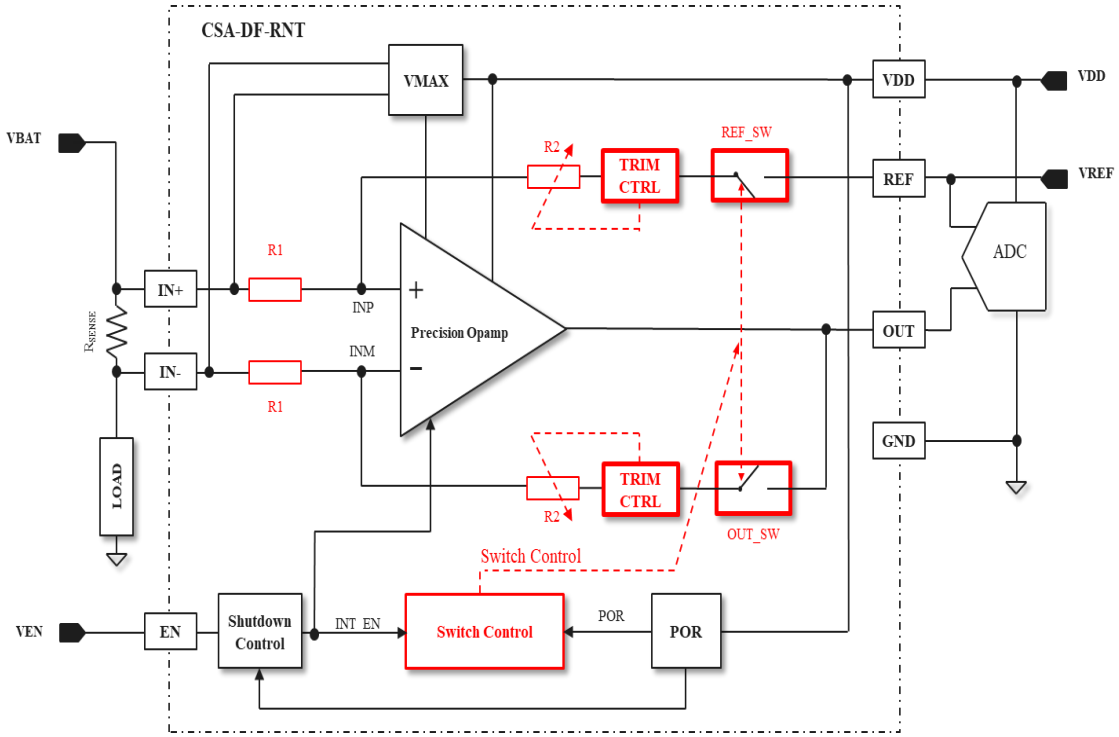

Figure 3.1. *Block diagram of CSA-DF-RNT* [13]

3.3. Implementation with Transfer Gate-Based Disable Function and Standard Resistive Trimming Procedure (CSA-DF-RNT-1)

The first of the two implementations of the current-sense amplifier with shutdown function and fine resistive network adjustment is detailed in the following. This architecture, referred to as CSA-DF-RNT-1, was initially proposed and validated in a previous work [14], being implemented in 0.25 µm CMOS technology and tested through both simulations and experimental measurements.

3.3.3. Experimental Results on CSA-DF-RNT-1

The architecture based on the general block diagram from Figure 3.1, which integrates both the shutdown circuit described in Subsection 3.3.1 and the fine resistive network trimming mechanism presented in 3.3.2, was physically implemented in 0.25 µm BCD CMOS technology and fabricated through a complete industrial flow. After the trimming of the resistive network and packaging of the chip, extensive measurements were performed on a batch of 22,000 circuits, with the results shown in Figure 3.5. Accuracy parameters such as offset and common-mode rejection ratio (CMRR) do not meet the specified requirements, indicating a degradation in

measurement performance. Since the operational amplifier used is well-characterized and exhibits excellent offset and CMRR performance, the results suggest that the resistive network trimming is suboptimal, and mismatch within the passive structure contributes significantly to these deviations.

In addition, the switches used to implement the shutdown function introduce further errors due to their high R_{ON} resistance at low supply voltages, as well as resistance mismatch between the two branches. Packaging effects also play a role, potentially altering the absolute value of the resistors and introducing additional offsets.

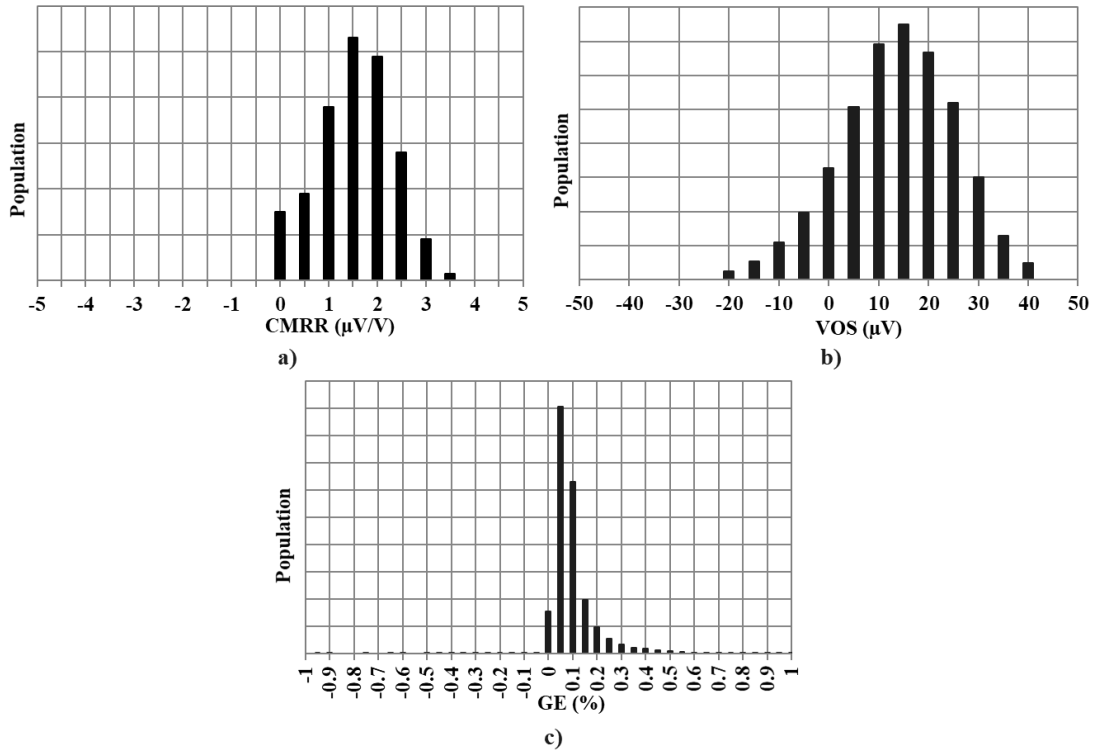

Figure 3.5. *Histograms of the main parameters of CSA-DF-RNT-1 – measured data*

3.4. Advanced Implementation with Digital Trimming and Optimized Disable Function (CSA-DF-RNT-2)

To overcome the limitations identified in the previous architecture, this section presents an advanced implementation that integrates a digital trimming mechanism for the resistive network and an optimized shutdown function, capable of ensuring stable performance across the entire supply voltage range.

3.4.1. Working Principle of the Disable Function

Unlike the previous implementation, where the shutdown function was realized using transfer gates (n-MOS + p-MOS), the advanced architecture proposed in this subsection employs pass-transistor switches based exclusively on n-MOS transistors

[13]. The architecture of the switches and their control circuit is shown in the simplified diagram in Figure 3.6.

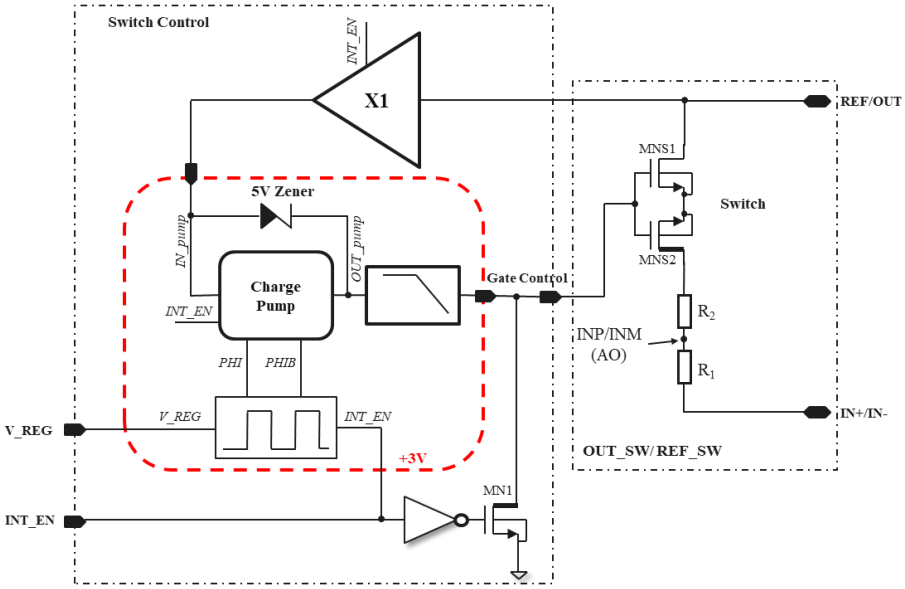

Figure 3.6. *Optimized schematic of the disable function from CSA-DF-RNT-2* [13]

3.4.2. Working Principle of the Digital Trimming Technique

One of the main drawbacks identified in the first architecture (CSA-DF-RNT-1) was the error introduced by the resistive network, which led to systematic offsets and gain inaccuracies. To overcome these limitations, the CSA-DF-RNT-2 architecture incorporates a digitally programmable resistive network (Figure 3.8), allowing fine calibration of the resistances on both branches after the packaging process.

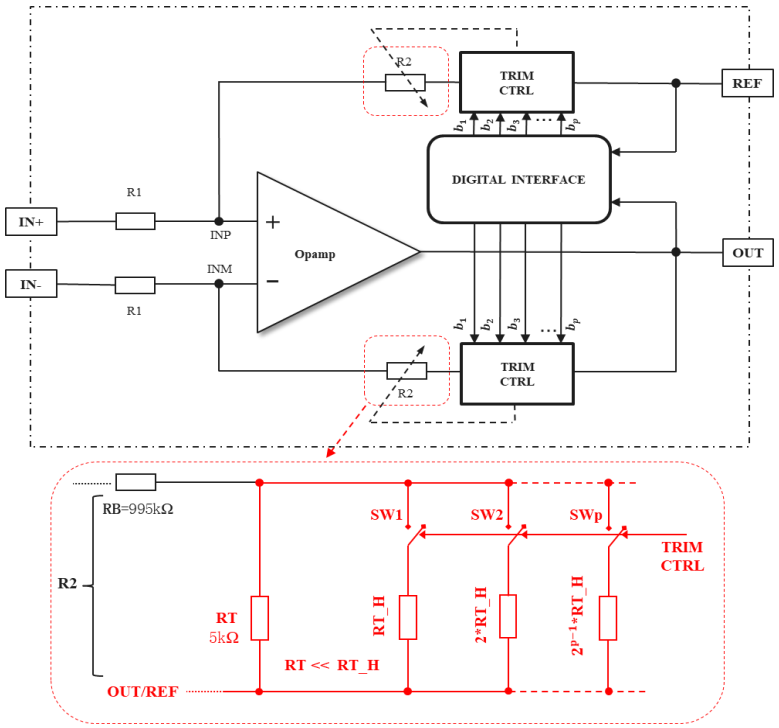

Figure 3.9. *Schematic Diagram of the Trimming Technique from CSA-DF-RNT-2*

Offset voltages can be compensated by activating a specific combination of switches. If the control bit b_k controls the activation of switch k, then the offset that can be corrected by a binary sequence, $b_1, b_2, \ldots, b_p$, such as the one shown in Figure 3.9, is given by the following expression:

$$V_{OS\_\eta} = -(V_{CM} - V_{REF}) \frac{{R_T}^2}{G \cdot R_{T\_H} \cdot (R_1 + R_2)} \sum_{k=1}^{p} \frac{b_k}{2^{k-1}} \tag{3.5}$$

Furthermore, based on these determinations, a look-up table can be implemented to associate offset voltage intervals with the switches that need to be activated in order to correct the corresponding offset.

3.4.3. Experimental Results on CSA-DF-RNT-2

The architecture referred to as CSA-DF-RNT-2, which integrates the optimized shutdown circuit and the digital fine-trimming technique described in Subchapter 3.4, was implemented in the same 0.25 μm BCD technology and under conditions similar to those of the first architecture. The experimental data shown in Figure 3.10 were obtained as part of a complete industrial qualification process carried out on tens of thousands of circuits. Based on these results, the product datasheet was also developed [13], confirming the relevance and validity of the proposed solutions in a real-world application context.

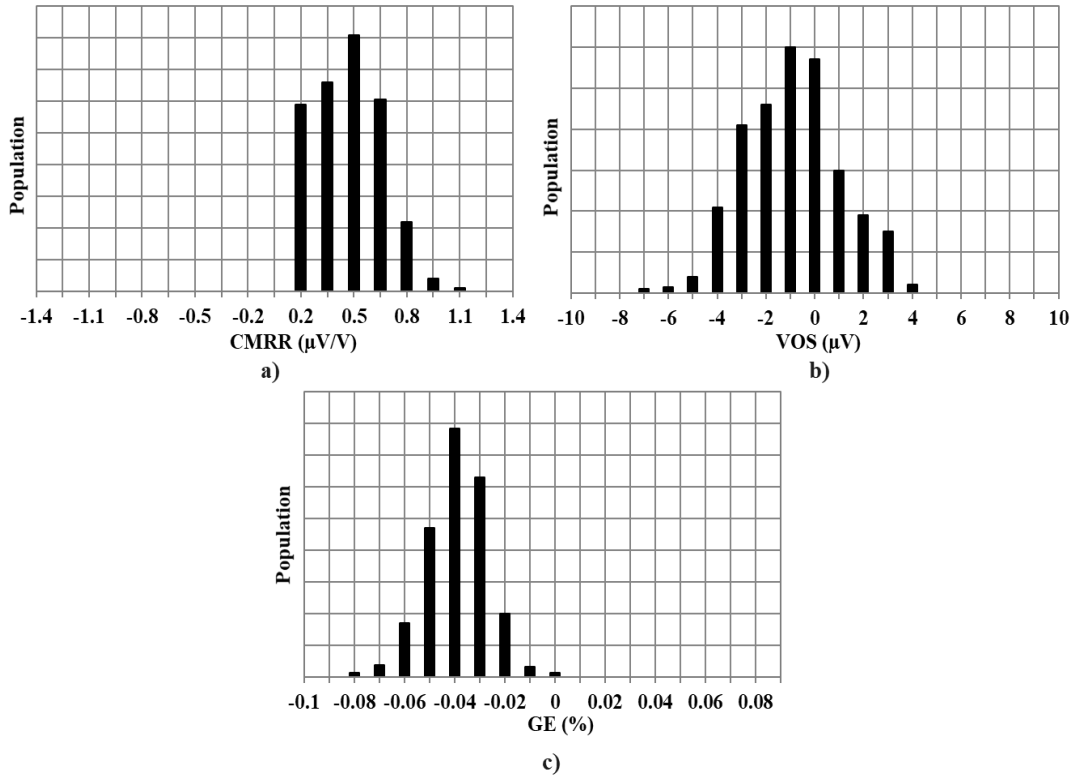

Figure 3.10. *Histograms of the main parameters of CSA-DF-RNT-2 – measured data*

It can be observed that the post-packaging digital fine-trimming technique performs excellently, having a significant impact on reducing parameter variation.

Compared to the results corresponding to an architecture without fine resistive network trimming (Figure 3.2), the offset voltage is now clearly reduced, with extreme values on the order of ±6 μV—representing a major improvement over the wide-spread distribution observed in the first implementation.

Param.	Specification		Measured Data				Unit
			AMC-FD-RFRR-1		AMC-FD-RFRR-2		
	Min.	Max.	Min.	Max.	Min.	Max.	
CMRR	2		4		1		μV/V
V_{OS}	-15	15	-50	50	-4	4	μV
GE	-0.4	0.4	-0.4	0.4	-0.1	0.1	%
I_{IB}		40		64		29	μA
I_{IBSD}		100		0.1		140	nA
I_Q		45		45		45	μA
I_{QSD}		0.2		0.25		0.2	μA

Table 3.3. *Comparison between specification and measured data on CSA-DF-RNT-1 and CSA-DF-RNT-2*

The clear advantages in terms of precision – particularly the reduction of offset, the improvement in CMRR, and gain error – fully justify the use of the optimized architecture, CSA-DF-RNT-2, especially in critical applications where metrological performance is essential.

3.5. Conclusions. Impact of the Proposed Methods on Current Measurement

Chapter 3 presented two original architectures of current sense amplifiers, referred to as CSA-DF-RNT-1 and CSA-DF-RNT-2. Both share the same block diagram (Figure 3.1) and integrate disable functions along with fine resistive network trimming mechanisms. The author's contributions focused on the development of these essential functionalities, as well as on the simulation of both architectures.

Based on a detailed theoretical analysis of the impact of the resistive network on offset and gain error, an original fine-trimming method was proposed and implemented in the CSA-DF-RNT-2 architecture. This solution significantly improves precision compared to the previous version, CSA-DF-RNT-1.

The CSA-DF-RNT-2 architecture, which integrates both contributions – the optimized disable function and the digital trimming technique – was implemented in a commercial product. The latter is characterized by low V_{OS} (±4 μV), CMRR > 120 dB, and gain error below 0.1%. These figures demonstrate a substantial performance improvement over CSA-DF-RNT-1 (V_{OS}= ±50 μV, CMRR > 108 dB, GE = ±0.4%).

In conclusion, this chapter provides relevant contributions to the field of precision current sense amplifiers.

Chapter 4

Methods for Output Current Compensation of Floating Gate Driver

4.1. Introduction

In this chapter, gate drivers (GDs) are analyzed in a specific application context – BLDC (brushless DC) motor control. The classical current-source GD architecture and its inherent limitations are presented. These limitations are examined as the main motivation for the proposed improvements: two patented techniques for compensating output current variations in high-voltage floating GDs [15]. These techniques significantly reduce the sensitivity of the output current to supply voltage variations.

The developed solutions have led to a substantial performance improvement, reducing the output current deviation from 25% in the uncompensated case to below 2% across the entire operating range (1 mA – 150 mA). Experimental results confirm the accuracy of the simulations, validating the effectiveness of the proposed approaches [15], [16], [17].

Therefore, this chapter not only highlights the importance of precise current control in critical applications, but also proposes scalable, robust, and industrially validated solutions that can be easily integrated into existing GD architectures for electric drive applications

4.2. Current Sources in Gate Drivers. Applications in BLDC Motor Control

In motor control applications, gate drivers play a critical role in managing the switching behavior of power devices such as MOSFETs or IGBTs, which are responsible for controlling the current through the motor windings [18], [19]. These devices can be integrated on-chip or implemented as external discrete transistors, depending on the system architecture and application requirements [20]–[24].

Many modern applications require gate drivers capable of delivering a constant current for charging or discharging the gate (I_{CHG}/I_{DCHG}), the so-called current-source gate drivers (CS-GD). Unlike traditional gate drivers (with external resistance), current-source gate drivers (CS-GD) allow precise programming and control of the output current value, both during the charging and discharging phases. This approach enables

independent control of dV/dt and dI/dt during switching, reduction of switching losses, and improved electromagnetic compatibility. In the absence of such an architecture, the gate current can vary significantly with the supply voltage, leading to variations in switching times and unpredictable behavior in critical applications [25]–[27].

The primary function of a CS-GD is to charge or discharge the gate capacitance of the power switch by delivering a controlled source or sink current, ensuring well-defined voltage transitions between the ON and OFF states [26].

One of the most important parameters of a current-source gate driver is, naturally, the accuracy of the output current, as it directly impacts key performance factors such as switching speed, rise and fall times, and overall power losses.

4.3. Standard Current-Source Gate Driver (CS-GD) Architecture. Operating Principles

After the previous section analyzed the role of CS-GDs in motor control applications, this paragraph presents a standard architecture used for generating the output current in such drivers. This solution has been practically implemented in several industrial projects and validated through both simulations and silicon testing, demonstrating robust operation under real-world conditions.

4.3.2. Simplified Architecture of a Current-Source Gate Driver with V_{GS} Reference

A typical gate control architecture for an active power branch (High-Side Gate Driver – HSx or Low-Side Gate Driver – LSx) is illustrated in Figure 4.5. It consists of three main blocks: the output stage, which includes the gate charge and discharge devices (M_{chg} and M_{dschg}); the V_{GS} reference circuit (including the reference transistors, M_{ref}); and the current digital-to-analog converter (iDAC). For simplicity and clarity, the explanations below will refer exclusively to the high-side branch.

As shown in Figure 4.5, the simplified architecture employs two VGS-REF structuresone for defining the maximum output current and the other for defining the minimum output current. These structures are used to convert the reference currents $I_{ref,min}$ and $I_{ref,max}$ into $I_{vgs,min}$ and $I_{vgs,max}$. The resulting currents serve as inputs to the current digital-to-analog converter (iDAC). The output of this block is a current referred to as I_{vgs}, more specifically $I_{vgs,chg}$, since it generates the control voltage for the output charge transistor, M_{chg}. Its value is given by the following relation:

$$I_{vgs,chg} = I_{vgs,min} + \frac{n}{2^m}\left(I_{vgs,max} - I_{vgs,min}\right) \tag{4.9}$$

where $I_{vgs,min}$ and $I_{vgs,max}$ have the previously discussed meanings, *m* is the resolution of the converter in bits, and *n* is the input word to the converter, represented on m bits. As shown by equation (4.9), the output current of the iDAC, which generates the control voltage for the output transistor, is a linear combination of the two I_{vgs}. Therefore, the

architecture benefits from first-order thermal compensation resulting from the cancellation of the threshold voltage variation with temperature.

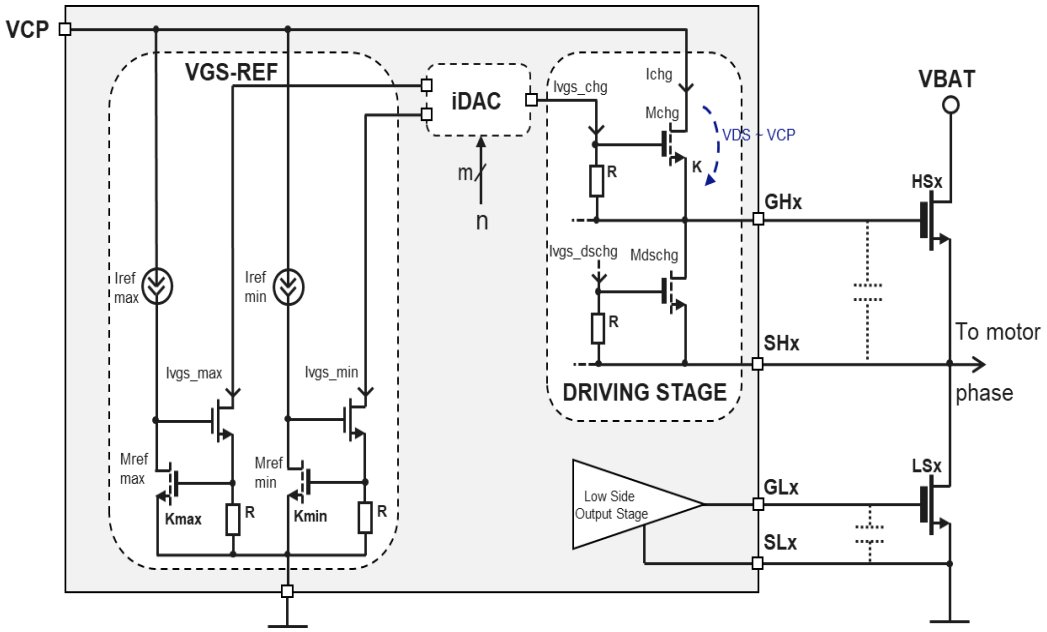

Figure 4.5. *Architecture of a current-source gate driver with V_{GS} reference*

The simplified schematic in Figure 4.5 is completed by the output stage of the floating gate driver. Within this output stage, two key transistors can be identified: the current-control transistor for gate charging (M_{chg}), and the corresponding one for gate discharging (M_{dschg}). For the subsequent analysis, we will focus exclusively on the charging transistor (M_{chg}), as all conclusions derived can be extended without loss of generality to the discharging path. The gate to source voltage (V_{GS}) of M_{chg} is given by the output current of the iDAC, which flows through a resistor connected between the gate and source terminals of this transistor.

Thus, a simplified current-source gate driver architecture with V_{GS} reference, has been presented, highlighting its main functional blocks and the significance of the key parameters involved in the circuit operation.

4.4. Standard Architecture's Limitations. Prior Art

To facilitate a clear analysis of the limitations inherent to the standard architecture, Figure 4.6 introduces a simplified version of the gate driver depicted in Figure 4.5. This version excludes the iDAC block and employs a single V_{GS} reference, instead of the dual-reference schematic implemented in the full design.

Such simplification allows for an intuitive understanding of the gate current generation and propagation mechanism, while preserving the generality of the conclusions. The analytical derivations and design considerations presented in the following sections can be directly extended to the complete case, which features two reference levels and digital switching between current settings.

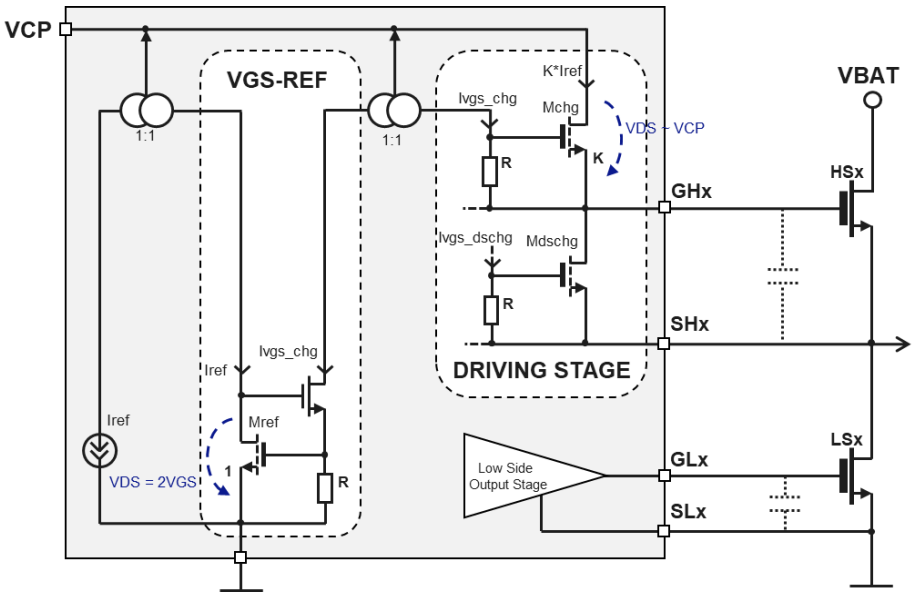

Figure 4.6. *Simplified architecture of a current-source gate driver*

A source of mismatch between the reference (M_{ref}) and the output stage transistor (M_{chg}) is highlighted in the schematic from Figure 4.6, namely the significant difference in their drain–source voltages, V_{DS}. While the reference transistor operates with a V_{DS} of approximately two gate–source voltages (around 4–5 V), the charging transistor sees a V_{DS} equal to the full supply voltage V_{CP} at the start of the charging phase. The charge pump output voltage, V_{CP}, typically reaches several tens of volts. Figure 4.7 illustrates the dependence of the charge current (I_{chg}) on the charge pump voltage (V_{CP}), under the maximum current setting condition of 150 mA.

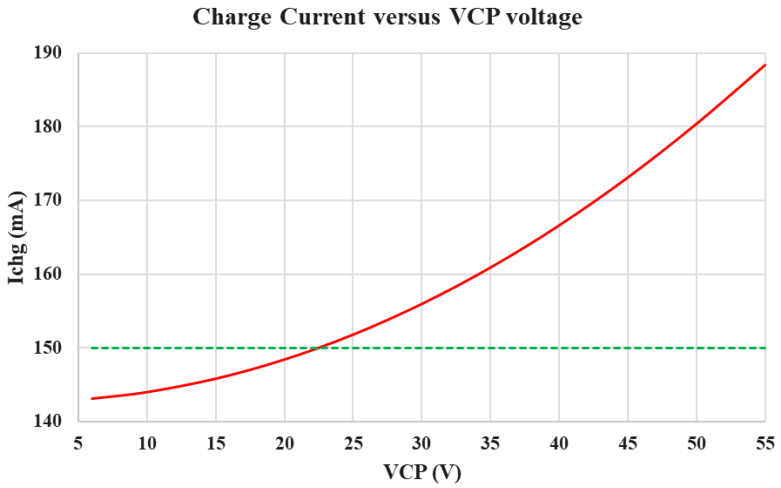

Figure 4.7. *Dependence of the charge current I_{chg} on the charge pump voltage V_{CP}*

The graph highlights the behavior of the charging current across the entire operating range of V_{CP}, thereby revealing a critical performance limitation.From the typical charge pump voltage of approximately 25 V up to its maximum value of 55 V, the observed variation in the charging current exceeds 20% – increasing from the expected nominal value of 150 mA to 185 mA.

The first method to address this issue involves increasing the channel length of the transistor [17], [25], which results in a quadratic increase in the area of the six-channel charging transistors.This approach is inefficient in terms of both cost and silicon area integration.

The second approach is illustrated in the conceptual diagram shown in Figure 4.8 and involves the use of a cascode configuration, M_{CASC}, for the charge transistor [50]. The cascode limits the V_{DS} of the charge transistor to the output voltage of the floating bias circuit (SH + 15 V) minus the V_{GS} of the cascode transistor. As a result, the V_{DS} is clamped to a value around 10 V [25].

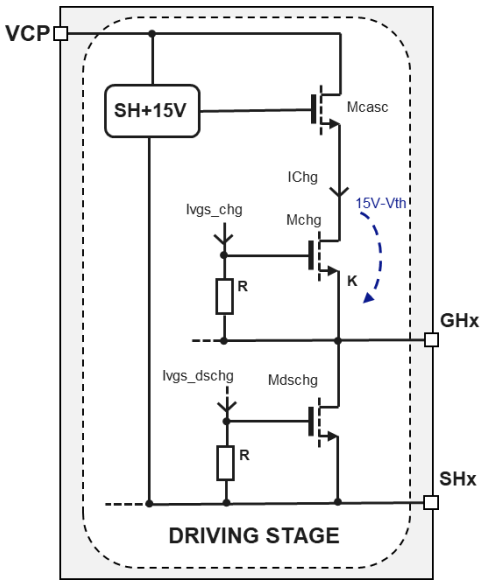

Figure 4.8. *Driving stage with cascoded charge transistor*

Ultimately, both approaches result in a significant increase in silicon area, emphasizing the need for a compensation technique capable of ensuring the required output current accuracy without compromising efficiency or cost. The following sections present two original compensation methods, developed with the goal of improving output current precision while maintaining low power consumption and minimal impact on silicon area.

4.5. Compensation Methods for Channel-Length Modulation in Current Sources Used in Gate Drivers. Operating Principle

As a consequence of the limitations identified in the previous subsection, two compensation methods were developed to address the channel-length modulation effect in current-source gate drivers (CS-GD). Both methods are based on the same underlying operating principle, illustrated in the diagram shown in Figure 4.9. The two proposed architectures are referred to as the I_{ref} method and the I_{vgs} method.

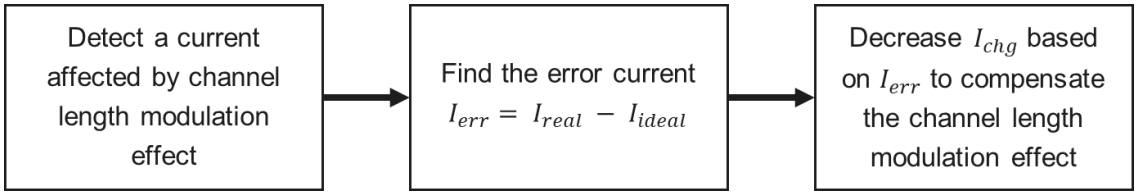

Figure 4.9. *Functional diagram of the proposed methods*

4.6. Proposed Architecture with I_{ref} compensation

The first proposed solution, referred to as the I_{ref}-compensated architecture (Figure 4.11), aims to correct reference current variations and is applied exclusively within the V_{GS} reference generation circuit.

This method introduces an additional branch that includes a sensing transistor, M_{sns}, identical to the reference transistor, M_{ref}, nd biased with the same gate-source voltage, V_{GS}. However, the drain-source voltage of M_{sns} is set to a level close to V_{CP}. Under these conditions, the drain current of the sensing transistor is affected by channel length modulation in the same way as the output stage transistor, becoming slightly higher than the reference current.

$$I_{sns} = I_{ref}(1 + \lambda V_{CP}) = I_{ref}(1 + \alpha) \tag{4.15}$$

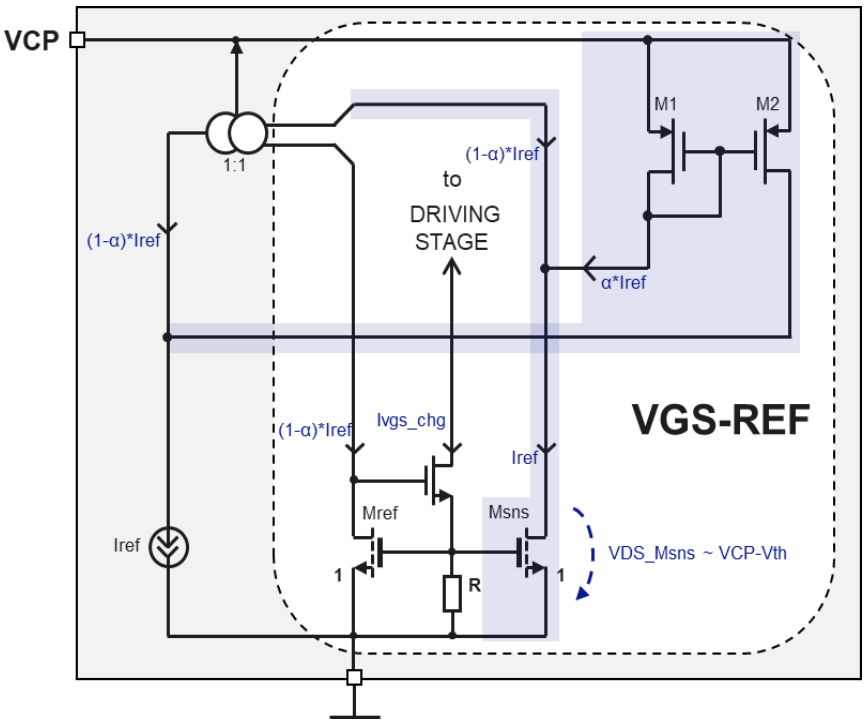

Figure 4.11. *Proposed arhitecture with I_{ref} compensation*

The M_1-M_2 current mirror is used to sense the error current. By applying Kirchhoff's first law at the drain node of transistor, M_1, the following expression is obtained:

$$I_{M1} = I_{ref}(1 + \alpha) - I_{ref} = \alpha I_{ref} = I_{err} \tag{4.16}$$

As can be observed, the reference transistor, M_{ref}, is deliberately biased at a lower current, $I_{ref}(1-\alpha)$, in order to compensate the channel length modulation effect in the charge transistor from the output stage. By substituting the compensated value of the reference current into equation (4.13), the following expression is obtained:

$$I_{chg,real} = K \cdot I_{ref}(1-\alpha)(1+\alpha) = K \cdot I_{ref}(1-\alpha^2) \quad (4.17)$$

Assuming that $\alpha << 1$, it is a reasonable approximation to consider $1-\alpha^2 \cong 1$. In this case, it can be observed that the actual load current is effectively compensated, with the error being significantly reduced by the proposed architecture.

In comparison with the standard configuration presented in Figure 4.6, the proposed architecture introduces only a limited number of additional devices.

4.7. Proposed Architecture with I_{vgs} Compensation

The second proposed method, referred to as I_{vgs} compensation (figure 4.12), is applied exclusively within the driving stage. Similar to the first method, a sensing transistor (M_{chg_sns}) is also used in this case.

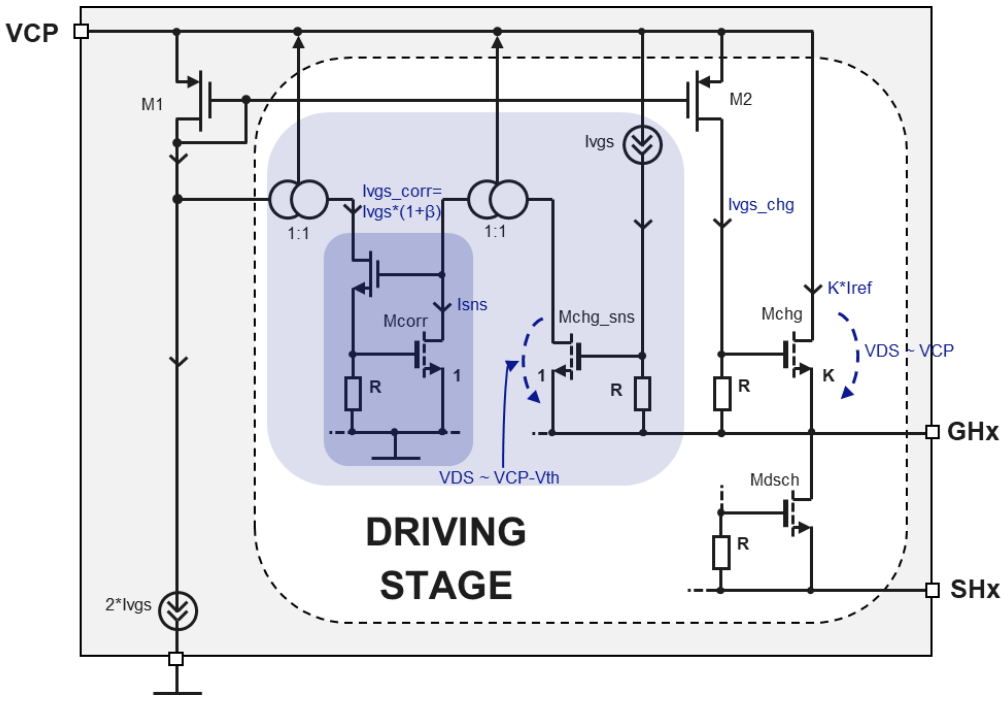

Figure 4.12. *Proposed architecture with I_{vgs} compensation*

Next, a VGS-REF-type structure (comprising M_{corr} and R_S), is used to convert this supply-dependent current into a I_{vgs} curent, named I_{vgs_corr}. Its value is obtained by substituting the drain current of the sensing transistor given by equation (4.15) into equation (4.3).

$$I_{vgs\_corr} = \frac{V_T + \sqrt{\frac{2LI_{ref}}{CW}(1+\alpha)}}{R} \quad (4.18)$$

Assuming that $\alpha << 1$, it is a valid approximation to consider that $\sqrt{1+\alpha} \cong 1 + \frac{\alpha}{2} = 1 + \beta$. Equation (4.18) is then expanded using this approximation, obtaining:

$$I_{vgs\_corr} = I_{vgs}\,(1+\beta) \tag{4.19}$$

At this stage, a I_{vgs} current affected by the channel length modulation effect has been obtained. In order to achieve a compensated current, $I_{vgs}\,(1-\beta)$ is targeted. This can be easily achieved by subtracting the previously obtained correction current, I_{vgs_corr}, from $2I_{vgs}$. By applying Kirchhoff's first law at the drain of transistor M_1 in the circuit shown in Figure 4.12, the following expression is obtained:

$$I_{vgs\_chg} = I_{vgs}\,(1-\beta) \tag{4.20}$$

As a result, in this compensation method, the charge transistor, M_{chg} is deliberately biased with a lower control voltage, imposed by the compensation applied to the I_{vgs_chg} current. In this way, the channel length modulation effect is minimized through the correction of the I_{vgs}. Similar to the previously presented method, this method introduces only a small number of additional devices, which are highlighted in Figure 4.12. These devices do not significantly increase the overall chip area.

4.8. Results. Simulations and Measurements

The two compensation architectures designed to mitigate the channel length modulation effect in the load transistor were validated through simulations and measurements, which will be presented in this section. Additionally, the I_{ref} compensation architecture was implemented in a commercial product.

Figure 4.13 shows a graph illustrating the load current error as a function of the charge pump voltage, for the extreme output current values—1 mA (minimum) and 150 mA (maximum). Simulation results indicate that, in the absence of compensation, the load current deviation can reach up to 25%. Once either of the compensation methods is implemented, the deviation drops below 2% in all cases. Bench measurements (green dots) confirm the effectiveness of this solution, with errors remaining below 2%, thus demonstrating the robustness and practical applicability of the proposed method.

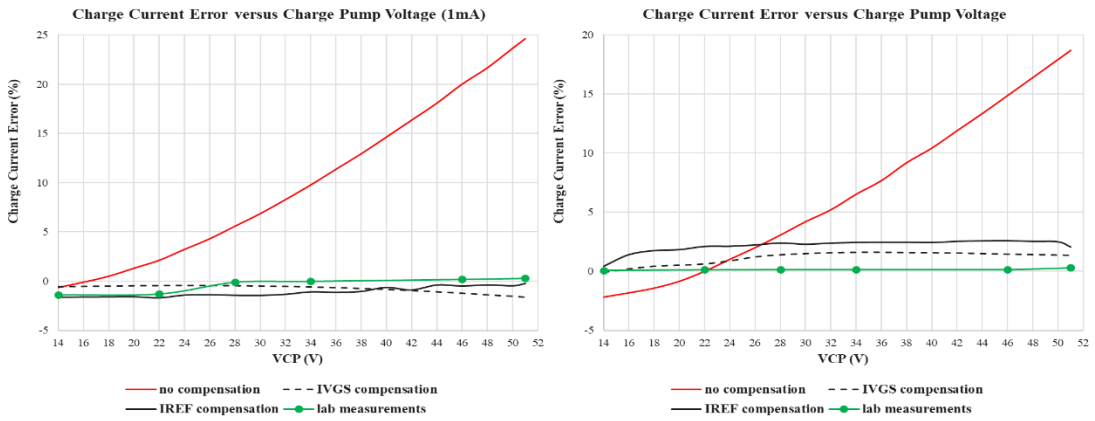

Figure 4.13. *Charge current error versus V_{CP} voltage*

To assess the robustness and consistency of the proposed circuit, a statistical analysis was performed on a batch of 345 fabricated chips. The experimental results are presented in Figure 4.15. The parameter under investigation is the output load current, evaluated at the minimum and maximum current settings. Measurements were conducted at room temperature, with the charge pump voltage set to its maximum value (51 V), under identical test conditions, in order to ensure the reliability and repeatability of the results.

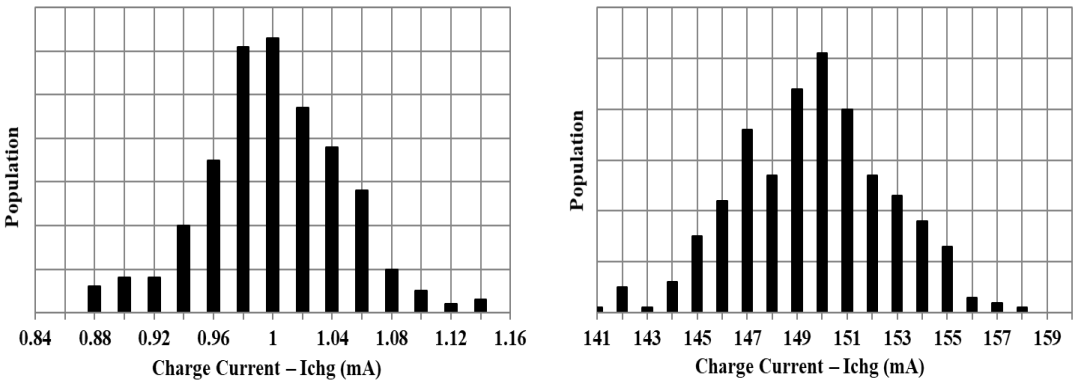

Figure 4.15. *Measured charge current distributions*
a) minimum setting – 1mA b) maximum setting – 150mA

4.9. Conclusions. Impact of the Proposed Methods on Current Control

In conclusion, this chapter addresses the significant impact of the voltage drop across the output stage on the gate driver output current. A typical gate driver control architecture was presented, highlighting its inherent limitations and the need to compensate the V_{DS} variation in order to ensure performance that meets the stringent requirements of the automotive domain..

To overcome this limitation, two original compensation techniques were developed: the I_{ref} method and the I_{vgs} method. Based on these techniques, two new circuit architectures were designed, without incurring a significant increase in silicon area. One of these architectures, based on I_{ref} compensation, was implemented in silicon, and the measurement results show strong agreement with simulations, confirming the high performance of the proposed solution. Both methods were included in a patent application [15]. It is worth noting that the I_{ref} compensation solution was used in a commercial product.

The developed solutions effectively reduce the charge current error from 25% to 2%, highlighting their potential to improve the accuracy and reliability of gate drivers in real-world applications. Owing to their demonstrated efficiency in minimizing current errors, these methods represent strong candidates for integration into future high-performance gate driver products.

Chapter 5

Temperature Sensor Based on SiC Schottky Diodes Biased with Constant Current

5.1. Introduction

In industrial applications involving high temperatures and harsh operating conditions, accurate temperature monitoring is critical for ensuring equipment reliability and performance. In this context, the silicon carbide (SiC) Schottky diode emerges as a promising alternative due to its thermal stability and high sensitivity to temperature variations [28], [29].

This chapter presents a comparative analysis of two essential temperature sensing methods based on SiC Schottky diodes: the standard method and the differential method [30]. Based on the differential method, identified as the optimal solution, an original patented architecture [31] is proposed, whose key component is a digitally programmable current source. This source ensures the stable and accurate generation of the bias currents required by the sensing diode. The diode-conditioning circuit assembly was initially tested under laboratory conditions and subsequently integrated into an industrial-grade probe, resulting in an intelligent temperature sensor whose operation was validated through detailed experimental measurements.

5.2. Sensor Architecture Considerations and Industrial Application Requirements

5.2.1. Schottky Diode used as Temperature Sensor: Working Principles

As demonstrated in [28], [32], the voltage across a Schottky diode (V_{SD}) biased at a constant current (I_{SD}) exhibits a quasi-linear dependence on temperature, as expressed by the following relation:

$$V_{SD}(T) = n\Phi_{Bn,eff} - \left[n\Phi_{Bn,eff} + 2mV_{th0}\ln\left(\frac{T}{T_0}\right) - V_{SD}(T_0)\right]\frac{T}{T_0} \quad (5.1)$$

Equation (5.1) describes a quasi-linear, decreasing characteristic with a slope of approximately –2 mV/°C. The temperature sensing method based on equation (5.1) involves simple, direct processing of the voltage across the device terminals.

The Schottky diode can also be used as a temperature sensor if a differential processing method is employed, as described by the following relation:

$$\Delta V_{SD}(T) = m\frac{KT}{q}\ln(n) = C_1 T \quad (5.3)$$

If the input quantity to the conversion system is the voltage difference between two identical diodes biased with different currents, as previously considered, then equation (5.3) shows that this quantity is directly proportional to temperature, with a sensitivity that is logarithmically dependent on the ratio of the two bias currents, ln(n). As shown in [32], an identical relation to equation (5.3) can be obtained if two diodes are biased with the same current and placed in the same environment, but with a junction area ratio equal to n.

5.2.2. Comparison between Methods. Calibration. Error Analysis

The data presented in this paragraph highlight the significantly superior performance of the differential method, particularly when two-point calibration is applied, where the advantages in terms of linearity and error reduction become even more pronounced. Based on this observation, a dedicated signal processing circuit is proposed, which uses the differential method.

5.3. Intelligent Temperature Sensor (D1C)

5.3.1. Design Requirements

The specifications of the intelligent temperature sensor are presented in Table 5.1.

Parameter	Symbol	Specification	Comments
Eroarea maximă de măsurare	ERR = $\Delta T = T_{meas} - T$	<8º	2% Error related to the Entire temperature range Valid for any temperature from the 0 – 400ºC range;
Supply Voltage	V_{DD}	Tipic 24V	Assymetric supply voltage, specified by the industrial application;
Output Current	I_{OUT} (T)	4-20mA	I_{OUT} (0°C)=4mA; I_{OUT} (400ºC)=20mA;
Transmission via digital protocol	-	-	Transmission via RS485 to enable compatibility with a PROFIBUS-type network [4]
Ambient Temperature Range	T_{amb}	-40 < T_{amb} < 125ºC	Corresponds to the industrial application;
Current Comsuption	I_Q	<1mA	Valid at any T_{amb}; Total current consumption minus the output current, I_{OUT} (T);

Table 5.1. *Design requirements for the intelligent temperature sensor*

Among the most important requirements are the sensor's accuracy – defined by a maximum error of 8°C over the temperature range of interest (0–400°C) – and the asymmetric supply voltage of 24 V. Data transmission is performed using the industrial standard for sensors: a 4–20 mA current output. The operating temperature range of the components used must comply with industrial specifications (–40 to 125°C), and the supply current of the entire system must not exceed 1 mA.

5.3.4. Design of the Intelligent Temperature Sensor

The architecture of the developed sensor is shown in Figure 5.9. This represents an original contribution and is the subject of a patent, registered under number RO137926A2 [31]. It is based on the differential method, using a single diode that is sequentially biased with different currents.

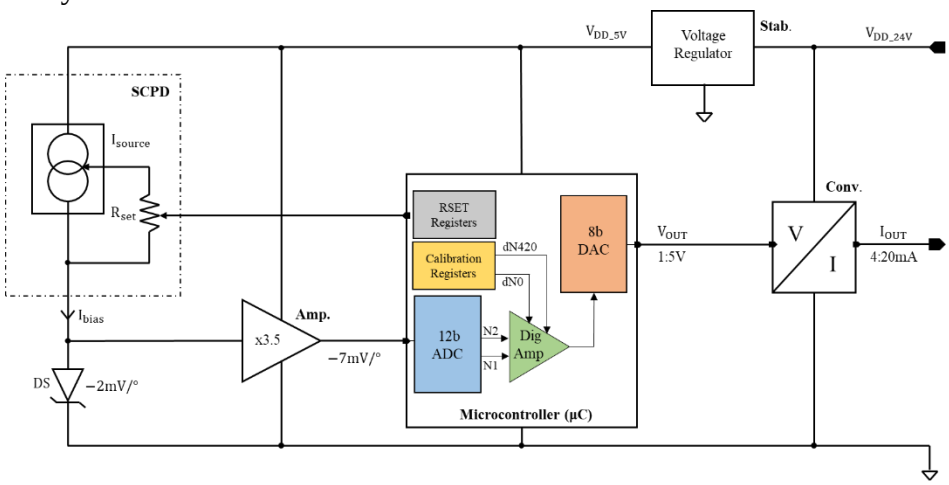

***Figure 5.9**. Proposed architecture for the D1C intelligent temperature sensor*

The originality of the architecture lies both in its functional simplicity and in its robustness to external variations, thus enabling the integration of the sensor in applications with high reliability and precision requirements. The intelligent sensor schematic consists of a digitally programmable current source (DPCS), a fixed-gain voltage amplifier (Amp.), a microcontroller (µC), a voltage regulator (Stab.), and a voltage-to-current converter (Conv.).

The entire signal processing chain, from the voltage across the sensing diode to the output current $I_{out}(T)$ is illustrated in Figure 5.10.

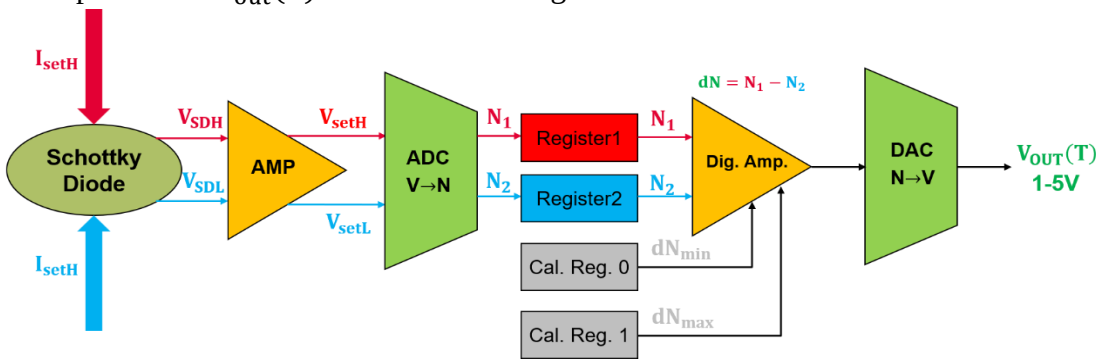

***Figure 5.10.** Signal processing chain of the Schottky diode voltage*

5.4. Practical Implementation of the Intelligent Sensor: PCB Design and Microcontroller Programming

After defining the architecture and analyzing the theoretical performance, the practical implementation of the sensor involved the development of a compact printed circuit board, as well as the programming of the microcontroller responsible for control, signal acquisition, and processing.

5.4.1. Schematic of the Intelligent Temperature Sensor

The selection of appropriate components for the signal conditioning circuit connected to the diode was followed by the design of the system's electrical schematic, shown in Figure 5.11. The schematic was created using the OrCAD Capture environment, with the goal of subsequently developing the PCB layout in the Allegro PCB Editor platform.

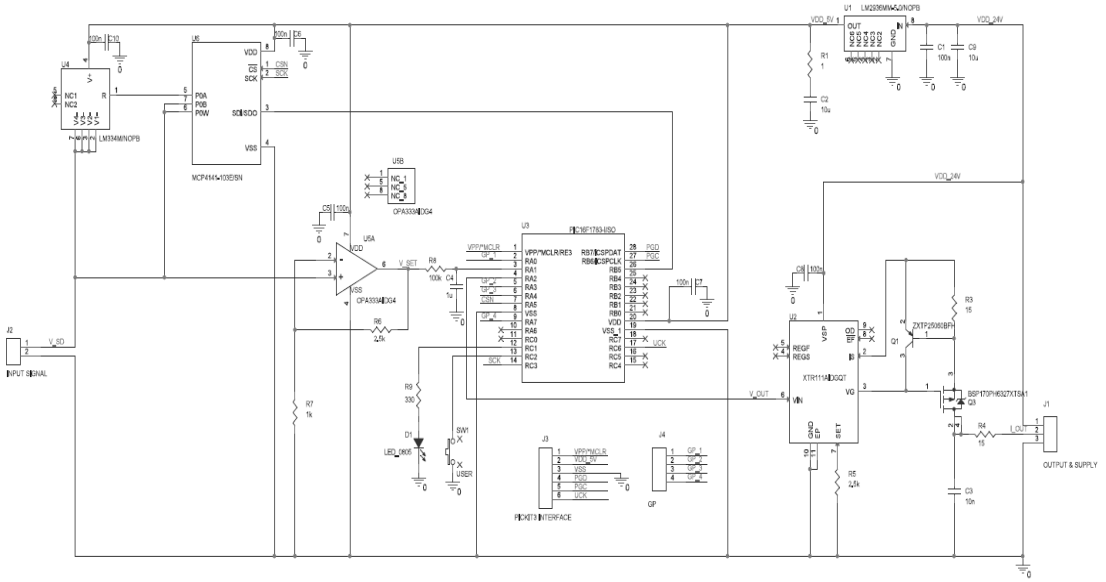

Figure 5.11. *Schematic of the intelligent temperature sensor*

The designed schematic includes the following components: a programmable current source based on the LM134 and the digital potentiometer MCP4141 (U4, U6), a precision operational amplifier (OPA333 – U5) configured as a non-inverting amplifier and accompanied by the feedback resistors R6 and R7, the PIC16F1783 microcontroller (U3), and the voltage-to-current converter XTR111 (U2), together with transistors Q1–Q3. Power is supplied from a 24 V industrial source and locally regulated through a linear voltage regulator (U1). In addition to these main blocks, the schematic contains auxiliary elements such as the ICSP programming interface (J3), a status LED (D1), a calibration button (SW1), and decoupling and protection filters to ensure stability and electromagnetic compatibility.

5.4.2. Design and Fabrication of the Printed Circuit Board

The printed circuit board integrating the intelligent temperature sensor based on a SiC Schottky diode was designed with consideration for the physical constraints imposed by the industrial probe enclosure in which it will be mounted. Figure 5.15 shows the final layout of the PCB and how it fits within the developed industrial probe.

Figure 5.15. *Placement of the circuit inside the sheath of a temperature probe used in a cement factory*

5.5. Lab Measurements

After the complete implementation of the hardware architecture and the associated firmware, the intelligent temperature sensor was subjected to a series of experimental tests in the laboratory at UPB. The results, summarized in Table 5.8, show that the calibration was successfully performed and that the probe is ready to be deployed in the industrial environment. The analysis was carried out over a temperature range from 0°C to 400°C, and the results demonstrate very good accuracy, with a maximum temperature deviation of approximately 2°C.

Temp. [°C]	I_{OUT} measured [mA]	I_{OUT} ideal [mA]	Temp. measured [°C]	ε_T [°C]
0.00	4	4.00	0.00	0.00
27.80	5.11	5.11	27.98	0.18
101.80	8.02	8.05	101.07	-0.73
150.50	10.06	10.02	151.4	0.90
202.30	12.15	12.06	204.65	2.35
251.00	14.09	14.04	252.22	1.22
299.80	16.02	15.99	300.47	0.67
350.30	18.02	18.01	350.61	0.31
400.00	20	20.00	400.00	0.00

Table 5.8. *Test results of the calibrated intelligent temperature probe in the 0 – 400°C temperature range*

5.6. Sensor Testing in Industrial Environment

To evaluate the real-world performance and reliability of the intelligent temperature sensor based on the SiC Schottky diode, testing was conducted under harsh industrial conditions at the Heidelberg Cement Romania S.A. plant in Fieni. Figure 5.23 shows the placement of the intelligent temperature probe within the industrial application.

Figure 5.23. *Installation place of the intelligent temperature sensor at the cement factory*

To evaluate the performance of the proposed intelligent temperature sensor, it was compared under industrial conditions with a conventional probe equipped with a thermocouple. The 20-hour time evolution of the temperature measured by the prototype probe, alongside the reference probe readings, is shown in Figure 5.24.

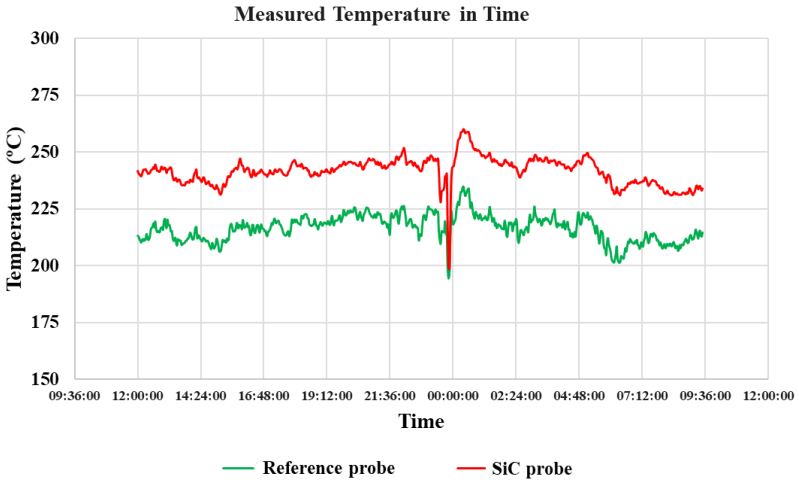

Figure 5.24. *Time Evolution of the Temperature Measured by the Intelligent Temperature Probe in an Industrial Environment (Cement Plant)*

The results presented in Figure 5.24 highlight a similar response dynamic for the two probes, confirming consistent behavior under real operating conditions. The measured temperature falls within the 200°C – 260°C range, and the shape of the curves indicates good correlation between the signals of the two measurement systems. The difference of approximately 30–40°C in the absolute values reported by the two probes is attributed to the ~3-meter distance between their mounting points.

5.7. Conclusions

Chapter 5 presented an original, patented D1C-type architecture for a high-precision temperature sensor, successfully tested up to 400 °C in harsh industrial environments. The solution employs a single SiC Schottky diode sequentially biased with two digitally programmed currents, achieving a maximum error below 8 °C, a standard 4–20 mA output, and 24 V supply. Testing in a cement plant confirmed the sensor's robustness, stability, and industrial applicability, validating both the differential method and the central role of the programmable current source in the system's performance.

Chapter 6

Conclusions

6.1. Summary of the Obtained Results

This thesis addressed, in an integrated and application-oriented manner, the problem of current measurement and control in precision analog circuits, with applications in industrial fields such as automotive, motor control, intelligent sensors, and power equipment. The work was structured around three complementary research directions: the design of current-sense amplifiers with shutdown function and fine resistive network trimming, the development of original methods for output current compensation in floating gate drivers, and the implementation of an intelligent temperature sensor based on a SiC Schottky diode biased with controlled current.

All proposed solutions are original and were supported by rigorous theoretical analyses, simulations, and experimental validations either on silicon or at system level. The contributions presented in Chapters 3 and 4 have been industrially implemented, integrated into commercial products, and fully characterized, confirming the practical applicability of the results. Additionally, the contributions described in Chapters 4 and 5 have been protected through patent applications, further consolidating the original and innovative nature of the work.

Chapter 2 provided the unifying theoretical framework for the three major research directions developed in the thesis: current-sense amplifiers (CSA), current-source gate drivers (CS-GD), and semiconductor-based temperature sensors. It offered a detailed analysis of current measurement techniques, the shutdown function and the need for fine trimming in CSAs, the fundamentals of GDs and EMC requirements, as well as the importance of controlled bias current for sensor accuracy. This chapter highlighted the thematic coherence of the work and the conceptual connection between the three domains in the context of industrial applications.

Chapter 3 presented two novel architectures of precision current-sense amplifiers (CSA) with shutdown function and fine resistive trimming: CSA-DF-RNT-1 and CSA-DF-RNT-2. The first architecture achieved a shutdown current below 0.25 μA and input bias current under 0.1 nA, but exhibited an offset of 50 μV and CMRR below 108 dB. The second, optimized architecture achieved an offset below 10 μV, CMRR above 120 dB, and gain error under 0.1%, thanks to a digitally controlled resistive network and a novel switch implementation. CSA-DF-RNT-2 was validated on thousands of units and integrated into an industrial product.

Chapter 4 Chapter 4 presented two novel, patented architectures for output current compensation in floating current-source gate drivers (CS-GDs) used in motor control applications. Both solutions – one based on I_{ref}, the other on I_{vgs}– reduced the output current error from 25% to below 2% across the entire current range (1–150 mA),

and were validated through simulations and large-volume measurements. Industrial implementation confirmed their performance across the full temperature range (–40 °C to +175 °C) and supply voltage range (4–40 V), demonstrating the robustness and practical feasibility of the proposed methods.

Chapter 5 presented a novel, patented architecture for a high-precision temperature sensor based on a single SiC Schottky diode, capable of operating up to 400 °C. The differential method employed achieves a maximum error below 8 °C across the entire temperature range, with a standard 4–20 mA output and 24 V supply. A digitally programmable current source precisely controls the bias ratio, ensuring stable and accurate measurement even in harsh industrial environments such as cement plants.

6.2. Original Contributions

This doctoral thesis includes a series of original contributions developed by the author and disseminated during the course of the research through patent applications and scientific communications in the field. The main contributions can be summarized as follows:

1) Synthesis of the literature and in-depth analysis regarding:
- Methods and architectures for current measurement;
- Error sources affecting current measurement applications using CSAs;
- Gate driver circuits for power switches, with emphasis on precision and electromagnetic compatibility in automotive applications;
- Semiconductor-based temperature sensors, biasing methods, and signal conditioning techniques, with a focus on the advantages offered by Schottky diodes fabricated in silicon carbide (SiC).

2) Contributions regarding current-sense amplifier (CSA) architectures:
- Contributions to the development of a precision CSA architecture integrating a shutdown function and a fine resistive network trimming mechanism, referred to as CSA-DF-RNT-1 [1], [12];
- Validation of the architecture through detailed measurements and simulations, enabling analysis of the impact of each block on overall performance [1], [12];
- Design and simulation of a novel circuit for implementing the shutdown function, based on a pass-transistor structure [12];
- Implementation and simulation of a digitally controlled fine-trimming solution, allowing post-packaging calibration of the resistive network [12];
- Contributions to the development of an improved precision CSA architecture, integrating an optimized shutdown function and an advanced trimming mechanism, referred to as CSA-DF-RNT-2 [12];
- Validation of the complete CSA-DF-RNT-2 system through simulations and experimental measurements [12].

3) Contributions regarding current-source gate driver (CS-GD) circuits:

- Identification of the main limitation in the classical CS-GD architecture in meeting application-level precision requirements, namely the variation of the output current caused by the channel length modulation effect (CLME) [1], [4], [6], [11], [12];
- Development, based on theoretical analysis, of a patented compensation technique for CLME using a sensing transistor that replicates the V_{DS} conditions of the output transistor [6];
- Development of CLME compensation architectures through adjustment of either the reference current or the control voltage (V_{GS}) of the output transistor, with a focus on area efficiency; both architectures are the subject of a patent [1], [4], [6], [11], [12];
- Conceptual validation of both architectures through simulations and measurements over an extended output current range (1–150 mA), demonstrating a reduction in error from 25% to 2% [1], [4], [6], [11], [12];
- Industrial implementation of the CS-GD architecture based on reference current adjustment within a commercial product.

4) Contributions regarding temperature sensors development:

- Comparative analysis, based on experimental data, of the standard and differential temperature sensing methods [3], [10];
- Development, based on the conclusions of this analysis, of an original implementation concept for the differential technique, including the design of a digitally programmable current source that sequentially biases the SiC Schottky diode at different currents [3], [5], [8], [10];
- Integration of the diode and signal conditioning circuit into an intelligent temperature sensor designed for industrial applications [3], [5], [8], [10];
- Experimental validation of the proposed solution and laboratory testing [3], [8], [11];
- Confirmation of the robustness of the proposed architecture through testing in a cement factory, under conditions of vibration, mechanical shock, and high temperature, as well as validation of compliance with industrial standards (4–20 mA output, 24 V supply);
- Contributions to the patenting of the proposed D1C architecture [5], [3], [10];

6.3. List of Original Publications

The following section presents the publications related to the research topics of this doctoral thesis, in which the original contributions described in the previous section are included. These publications have been cited throughout the chapters of the thesis

in the order in which the corresponding content appears, but they are listed below using a renumbered format.

[1] **V. Moise**, R. Pușcașu, G. Brezeanu, *Circuit Techniques for Enhancing Output Current Accuracy in Floating Gate Drivers*, in **Romanian Journal of Information Science and Technology**, 28(2), pp. 150-160, 2025, **ISI Q1 (2025), DOI: 10.59277/ROMJIST.2025.2.03**.

[2] **V. Moise**, R. Pușcașu, G. Brezeanu, *A Precision Current Sense Amplifier With Disable Function*, in **Proceedings of the 2020 International Semiconductor Conference (CAS)**, Sinaia, România, 8–10 October 2020, **ISI**, **WOS:000637264600013**, **DOI: 10.1109/CAS50358.2020.9268040.**

[3] **V. Moise**, F. Draghici, G. Pristavu, R. Pascu, D.-T. Oneata, G. Brezeanu, *Intelligent Temperature Sensor with SiC Schottky Diode*, in **Proceedings of the 2022 International Semiconductor Conference (CAS)**, Poiana Brașov, Romania, 12–14 Octombrie 2022, **ISI**, **DOI: 10.1109/CAS56377.2022.9934369.**

[4] **V. Moise**, R. Pușcașu, G. Brezeanu, *Methods for Output Current Compensation of Floating Gate Drivers*, in **Proceedings of the 2024 International Semiconductor Conference (CAS)**, Sinaia, Romania, 9–11 October 2024, **ISI**, **WOS: 001361909500029**, **DOI: 10.1109/CAS62834.2024.10736828.**

[5] F. Drăghici, G. Brezeanu, **V.-G. Moise**, R. Pascu, G. Pristavu, F. Mitu, *Sondă de măsurare a temperaturii în instalațiile industriale bazată pe diodă senzor pe carbură de siliciu*, Brevet **RO137926A2**, 30 January 2024.

[6] R. Pușcașu, **V. Moise**, *Controlling a power switching element using a sense switching element*, Patent Application USA, **Docket No.: 1186-623US01 / 2023P23191US**, 2023.

[7] **V. Moise**, A. Bădescu, *An Amplifier Design for Cosmic Particles Radio Detectors*, in **Proceedings of the 2018 Mediterranean Microwave Symposium (MMS)**, Istanbul, Turkey, 31 October – 2 November 2018, **ISI**, **WOS: 000458427500098**, **DOI: 10.1109/MMS.2018.8611799.**

[8] **V. Moise**, F. Drăghici, G. Pristavu, R. Pascu, F. Mitu, G. Brezeanu, *Wide Range Temperature Sensor with SiC Schottky Diode – Error Source Analysis*, poster presentation at **The 19th International Conference on Silicon Carbide and Related Materials (ICSCRM)**, 11–16 september 2022, Davos, Switzerland.

In addition to these, four scientific research reports have been completed, as detailed below:

[9] **V. Moise** – *Differential signal conditioning circuit for a sensor*, Scientific Report No. 1/2022, Doctoral School of Electronics, Telecommunications and Information Technology, University Politehnica of Bucharest, 2022.

[10] **V. Moise** – *Implementation and testing of the intelligent temperature sensor*, Scientific Report No. 1/2022, Doctoral School of Electronics, Telecommunications and Information Technology, University Politehnica of Bucharest, 2022.

[11] **V. Moise** – *Methods for output current compensation of floating gate drivers*, Scientific Report No. 1/2022, Doctoral School of Electronics, Telecommunications and Information Technology, University Politehnica of Bucharest, 2022.

[12] **V. Moise** – *Precision circuits for current measurement and control*, Scientific Report No. 1/2022, Doctoral School of Electronics, Telecommunications and Information Technology, University Politehnica of Bucharest, 2022.

Part of the publications included in this thesis were developed within a research project, in which the author contributed as a doctoral research member:

• **PN-III-P2-2.1-PED-2019-275PED/2020** – *High-temperature PTAT sensors with SiC Schottky diodes for monitoring and safety in harsh industrial environments* [3], [5], [8];

6.4. Perspectives for further development

With regard to current-sense amplifiers, the present work focused on improving the resistive feedback network by introducing innovative fine-trimming solutions and a reliable shutdown function. However, the core of the circuit—the operational amplifier—was not extensively analyzed. This opens a future research direction toward the exploration of advanced differential amplifier architectures with reduced offset, improved PSRR, and optimized power consumption, tailored for precision industrial applications.

As for gate drivers, the solutions proposed in this thesis were primarily adapted to conventional automotive systems powered at 12 V. However, current trends indicate a clear transition toward electric and hybrid vehicles, where the supply voltage often reaches 48 V or higher. Under these conditions, power dissipation becomes a major constraint, and the proposed current control solutions are no longer optimal in terms of energy efficiency. Therefore, new gate driver architectures are needed, featuring advanced current control mechanisms, reduced dynamic power consumption, and enhanced protection against voltage and temperature variations.

Finally, the further development of the temperature sensor presented in Chapter 5 could include the integration of an industrial digital interface (e.g., ProfiBUS, RS-485), as well as the implementation of self-calibration, diagnostics, and bidirectional communication mechanisms to enable full integration into intelligent industrial ecosystems.

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