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AND TECHNOLOGY POLITEHNICA
BUCHAREST**



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and Information Technology**

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Ph.D. THESIS SUMMARY

Cristian STANCU

**AMPLIFICATOARE OPERAȚIONALE CU
PERFORMANȚE ÎMBUNĂȚĂȚITE**

**OPERATIONAL AMPLIFIERS WITH IMPROVED
PERFORMANCE**

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Chapter 1

Introduction

1.1 Presentation of the field of the doctoral thesis

Electronics and microelectronics are key enablers of modern technology. Continuous miniaturization has made it possible to integrate a very large number of components on a single silicon chip, leading to faster and more compact systems, with reduced power consumption and improved reliability. In System-on-Chip (SoC) architectures, analog blocks remain indispensable because real-world signals are inherently analog; their conversion and conditioning rely on circuits such as operational amplifiers (op-amps), analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), oscillators, and voltage/current references. The operational amplifier, introduced in the 1940s-1950s and widely adopted once monolithic integration became available in the 1960s, has evolved significantly: performance levels once considered excellent (open-loop gain around 40 dB, common-mode rejection ratio (CMRR) around 50 dB, and offset voltage V_{OS} in the tens of millivolts) are no longer sufficient. Modern applications require gains above 80-100 dB, high power supply rejection ratio (PSRR)/CMRR, μV - level V_{OS} , low noise, and an extended unity-gain bandwidth (UGBW). In today's systems, the entire analog signal path performances depend directly on op-amp parameters (precision, linearity, stability, distortion), which imposes a difficult trade-off among gain, offset, noise, power, full input/output swing, transient response, and robustness to temperature and supply variations - a challenge that motivates current research in the field.

1.2 Scope of the doctoral thesis

Improving op-amps performance has a major scientific and technological impact, given their pervasive use in modern analog systems. This thesis topic - "Operational amplifiers with improved performance" - is motivated by the need to overcome current architectures limitations and to meet increasingly stringent requirements in precision applications. Op-amps design inherently involves trade-offs: reducing V_{OS} and increasing CMRR may come at the expense of bandwidth and stability, while increasing gain through larger device dimensions and bias currents introduces parasitic capacitances that can reduce phase margin.

Moreover, in two-stage CMOS folded-cascode amplifiers, lowering V_{OS} by increasing transistor area reduces mismatch, but it also increases gate-to-source capacitances and can degrade stability. In this context, the thesis investigates alternative solutions, such as source degeneration, to reduce sensitivity to variations in threshold voltage (V_{TH}) and transconductance (g_m).

An additional motivation is the CMRR, because in a folded-cascode op-amps, common-mode input variations can alter the input-stage transistors biasing (through V_{DS} variations and channel-length modulation), which leads to unequal currents and, consequently, to a common-mode-dependent offset voltage. In precision applications, it is essential that V_{OS} remains as constant as possible over the entire input range. At the same time, achieving full input swing at ever lower supply voltages remains a critical direction: complementary input pairs introduce extra parasitic and discontinuities in the transition region, whereas a charge pump can artificially extend the available voltage for the input stage. This thesis analyzes the latter approach by integrating an internal charge pump that raises the input-stage supply above V_{DD} , enabling a single differential input stage and full input-signal swing.

1.3 Content of the doctoral thesis

This thesis provides a set of original contributions in the operational amplifiers field, including the proposal, implementation, and evaluation of innovative solutions aimed at improving performance. The main contributions include: a current source that enables an approximately constant input differential stage transconductance; a temperature- and supply-compensated CMOS ring oscillator; an enhanced charge-pump architecture with feedback; a method for reducing offset voltage in folded-cascode amplifiers based on source degeneration; a circuit that improves the step response; and the integration of these elements into a family of operational-amplifiers with improved performance, demonstrating that the proposed innovations can coexist within a unified design.

The thesis is organized into seven chapters. Chapter 2 presents the proposed solution for stabilizing the input differential stage transconductance, describing the current-source architecture and the obtained results. Chapter 3 focuses on offset-voltage reduction in two-stage folded-cascode op-amps using source degeneration and high-precision resistors, with validation through simulations. Chapter 4 addresses the internal oscillator design required by the charge pump, including temperature and supply compensation. Chapter 5 details the charge pump developed to extend the input common-mode range, as well as a circuit that selects the maximum available voltage. Chapter 6 consolidates the contributions into a final schematic, highlighting the integration aspects and the achieved performance. Chapter 7 summarizes the overall conclusions, original contributions, and future research directions.

Chapter 2

Optimized Current-Source based on Brokaw Architecture for Constant Input Transistors Transconductance

Chapter 2 presents the design and validation of an optimized current source that provides a bias current with a controlled temperature dependence so that the input differential stage transconductance (g_m) remains approximately constant over a wide temperature range. The motivation is directly related to frequency stability: the bandwidth depends on g_m , and in weak inversion (often used to reduce V_{OS} and noise) g_m decreases with temperature if I_D is kept constant (2.1). Therefore, the differential pair is biased with a proportional to absolute temperature (PTAT) current so that the I_D increase with temperature compensates the g_m thermal dependence and, at the same time, helps reduce V_{OS} variation and its temperature coefficient.

$$UGBW = \frac{g_{mdiff}}{2^{(n-1)} \pi C_C} \quad (2.1)$$

2.1 Comparative Analysis of the Studied Architectures and Design Premises

Section 2.1 reviews representative literature solutions used as a starting point: the Widlar source, which is simple and efficient for small currents but temperature sensitive in weak inversion, and the Brokaw architecture, which generates a PTAT component (via ΔV_{BE}) and allows adding a complementary to absolute temperature (CTAT) component through resistors to tune the current temperature coefficient. However, although these solutions provide control over thermal dependence, they do not inherently guarantee an optimal g_m compensation for the input stage; therefore, the chapter develops the optimized solution proposed in this thesis.

2.2 Proposed current-source architecture

The complete implementation in Figure 2.3 includes: (i) an internal operational amplifier built with M_3 - M_4 and M_5 - M_8 , stabilized by capacitor C_1 ; (ii) current mirrors M_9 - M_{14} and M_{28} to replicate the current to the output branches; (iii) mirror cascodes (M_{15} - M_{20} and M_{29}), biased through M_{21} , to increase output resistance and improve immunity to supply variations; (iv) a start-up network that prevents the circuit from locking in the $I=0$ state; (v) a reference block based on a bandgap core and a voltage-to-current converter. The bias current temperature dependence is compared for three solutions (Widlar, Brokaw, and the proposed one), all sized to approximately $1\ \mu\text{A}$ at room temperature.

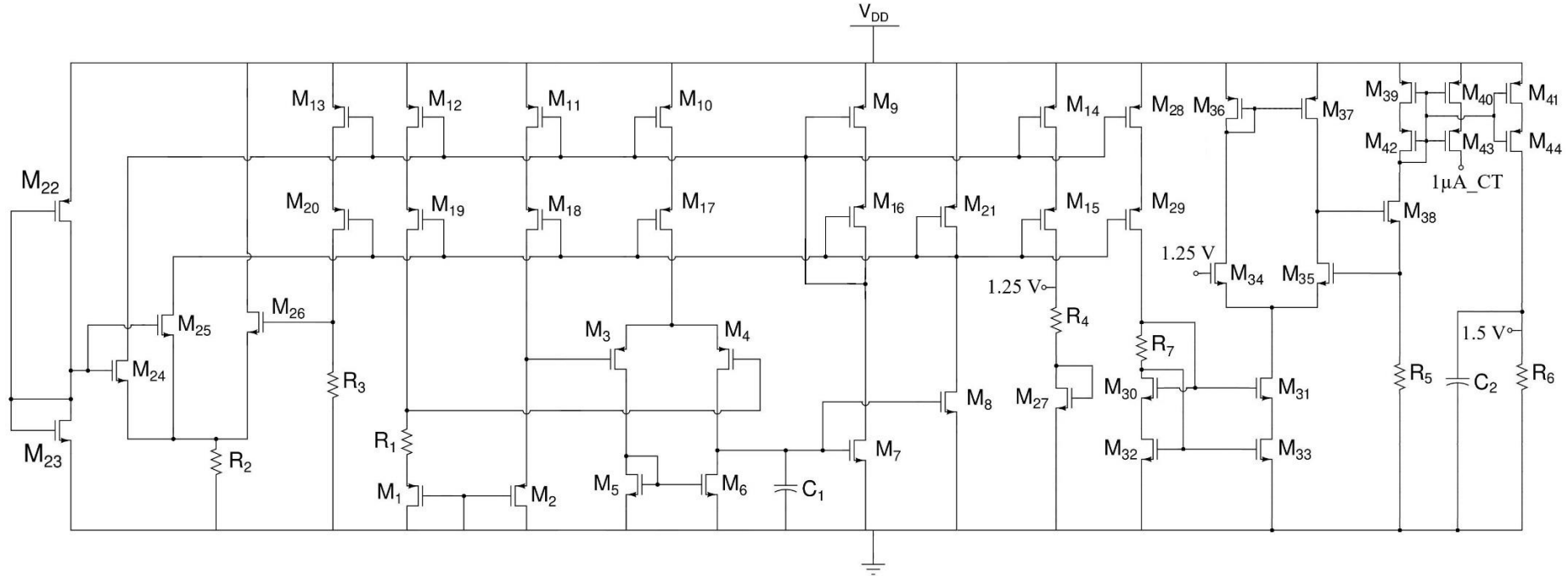


Figure 2.3 Optimized current source for achieving a constant transconductance of the input transistors.

2.3 Simulation results and analysis

The proposed architecture is evaluated through schematic-level simulations performed in Cadence Virtuoso using a 0.25 μm CMOS technology, at $V_{DD} = 5\text{ V}$ and temperature ranging from -40 to $150\text{ }^\circ\text{C}$. Comparative results are provided against the Widlar and Brokaw current sources, focusing on the generated bias current temperature variation, as well as the ability to stabilize the input-stage transconductance.

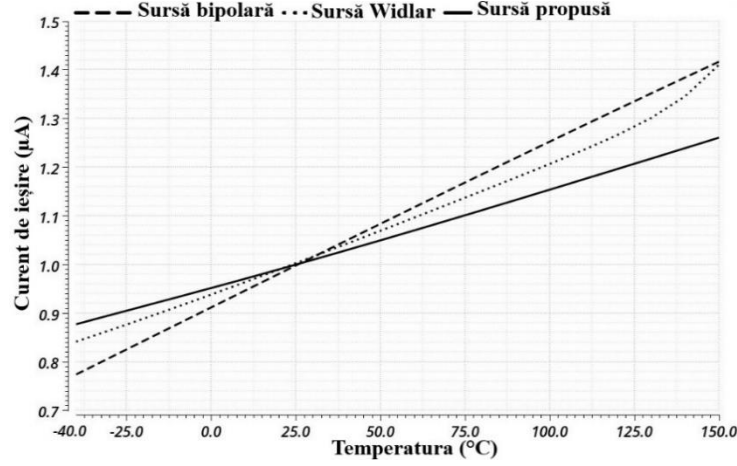


Figure 2.1 Bias current variation versus temperature for three current-source architectures: Widlar, Brokaw, and the proposed solution.

To highlight the impact on transconductance, the current delivered by each source biases a pMOS test differential pair (DUT), designed such that it has the same current density as device M_1 . The results in Figure 2.11 show the proposed source's direct benefit: for $g_m \approx 380\text{ }\mu\text{S}$ at room temperature, the total g_m variation over $(-40\text{ to }150)\text{ }^\circ\text{C}$ is only about $7\text{ }\mu\text{S}$ (below $\pm 2\%$).

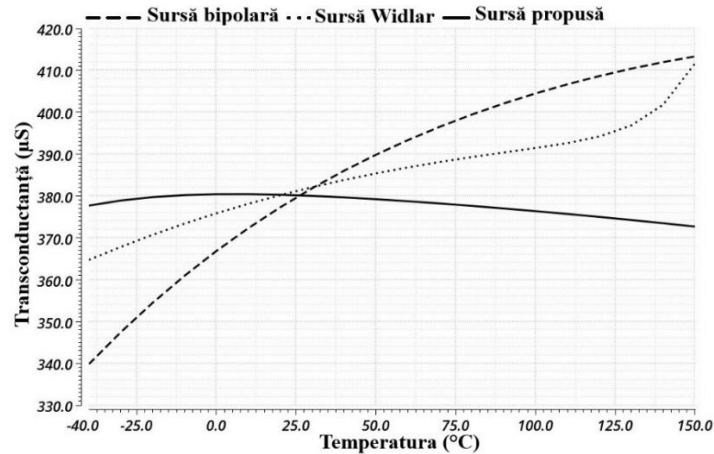


Figure 2.2 Input differential-stage transconductance variation versus temperature.

Robustness to process variations is evaluated in process corners (SS, FF, Sn-Fp, Fn-Sp). As expected, the absolute current value shifts across corners, while the PTAT slope remains very similar. In addition, Monte Carlo simulations (500 samples at $25\text{ }^\circ\text{C}$) yield a distribution centered around $\approx 1\text{ }\mu\text{A}$, with a standard deviation of $\approx 33.46\text{ nA}$.

2.4 The circuit layout

To validate physical integration, the current source layout is implemented (Figure 2.14) in a 0.25 μm CMOS technology, without the adjacent blocks (bandgap reference, voltage-to-current converter, 1.5 V reference). The occupied area is approximately 0.1495 mm² (excluding the auxiliary blocks).

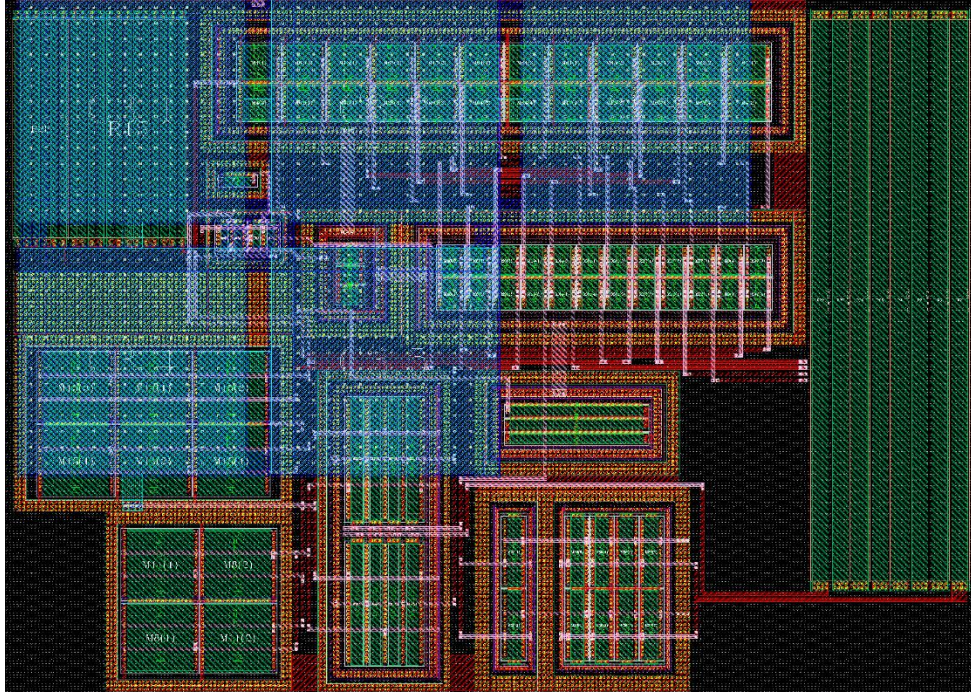


Figure 2.3 Designed current source layout.

2.5 Final conclusions

This chapter presented an optimized current source derived from the Brokaw principle and implemented in 0.25 μm CMOS, intended to stabilize the input-stage transconductance through a PTAT current, with direct impact on UGBW and on the amplifier thermal behavior. Simulations confirmed a reduced current variation of approximately (0.877 - 1.26) μA and a minimal g_m variation with temperature ($\approx 7 \mu\text{S}$), outperforming Widlar and Brokaw solutions. Corner and Monte Carlo analyses supported robustness to process spread, while the circuit layout demonstrated a compact integration ($\approx 0.1495 \text{ mm}^2$) verified by DRC/LVS.

Chapter 3

Offset voltage reduction in two-stage folded-cascode operational amplifiers using precision resistors

3.1 Two-stage folded-cascode op-amps architecture and offset-voltage derivation

The analysis is performed on a classic two-stage CMOS topology (Figure 3.2).

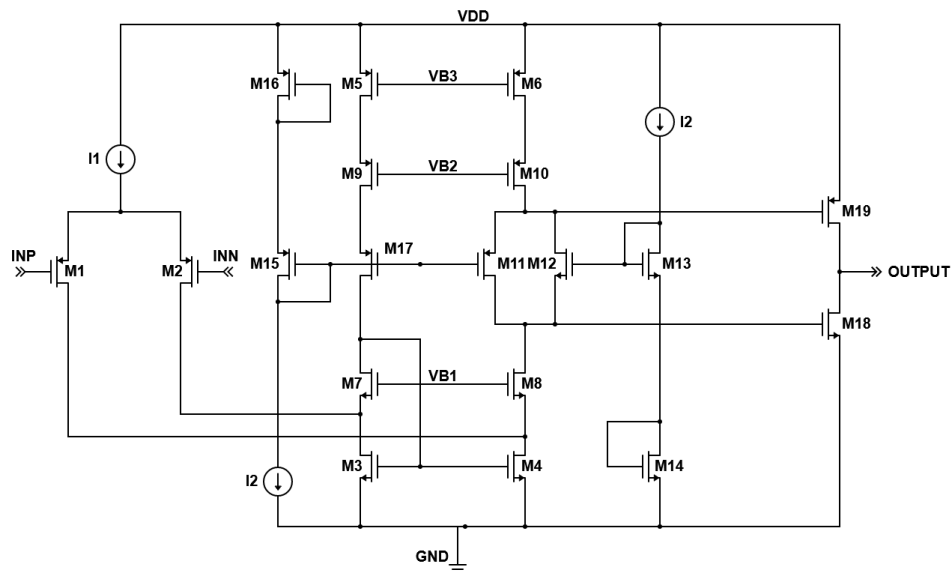


Figure 3.1 Two-stage folded-cascode operational amplifier.

3.2 Offset-voltage reduction using source degeneration

Source-degeneration resistors in the current-mirror sources reduce the effective g_m and the sensitivity to mismatches, the resulting V_{OS} is given in (3.17).

$$V_{OS} = - \left(\Delta V_{T1,2} + \frac{\Delta V_{T3,4}}{g_{m1,2} R_{S3,4}} + \frac{\Delta V_{T5,6}}{g_{m1,2} R_{S5,6}} \right) - \frac{I_D}{g_{m1,2}} \left(\frac{3 \cdot \Delta R_{S3,4}}{R_{S3,4}} + \frac{2 \cdot \Delta R_{S5,6}}{R_{S5,6}} - \frac{\Delta \beta_{1,2}}{\beta_{1,2}} \right) \quad (3.17)$$

3.3 High-precision (SiCr) resistors implementation to mitigate mismatch

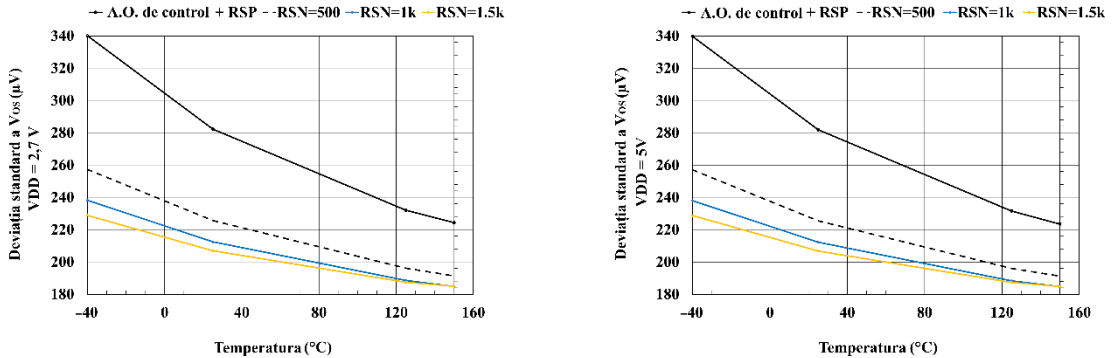
Because mismatch between adjacent resistors (ΔR_S) can introduce an additional component in V_{OS} , the use of high-precision resistors is essential.

3.4 Simulations and results

To assess the source degeneration impact on the ap-amp performance, both schematic-level and post-layout simulations with PEX, including parasitic elements, were carried out.

3.4.1 Schematic-level simulations

The simulations were performed in Cadence Virtuoso (0.25- μm CMOS), sweeping source degeneration in both the pMOS and nMOS current mirrors for $R_S=500\ \Omega$, 1 k Ω , and 1.5 k Ω . The V_{OS} variability was assessed via Monte Carlo analysis (1000 samples), showing a reduction in $\sigma(V_{OS})$ with increasing degeneration and a clear temperature dependence (Figure 3.11). This behavior is attributed to partial mismatch compensation at the nMOS mirror nodes, where currents from the differential pair and the folded-cascode branch are summed.



(a)

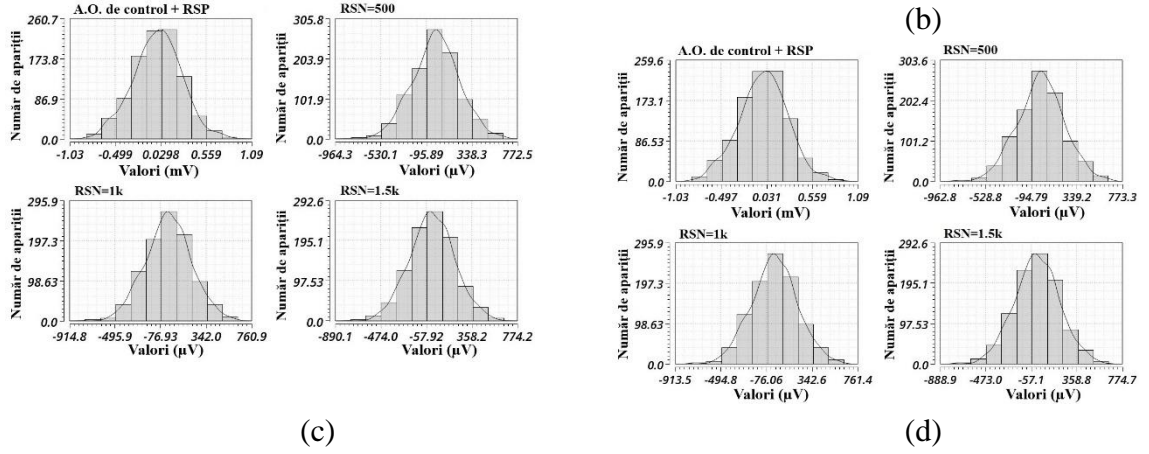


Figure 3.2 $\sigma(V_{os})$ with temperature, pMOS source degeneration = 1 k Ω and nMOS source degeneration included. (a) $VDD = 2.7 V$; (b) $VDD = 5 V$; (c) Monte Carlo histograms, room temperature and $VDD = 2.7 V$; (d) Monte Carlo histograms, room temperature and $VDD = 5 V$.

3.4.2 Post-layout simulations

Post-layout PEX (R_C_CC) simulations include parasitic elements; the schematic-versus-PEX comparison for $\sigma(V_{OS})$ and CMRR is shown in Figure 3.17. The differences are minor; at 27 °C, $\sigma(V_{OS}) \approx 209 \mu V$, remaining nearly constant vs. schematic results.

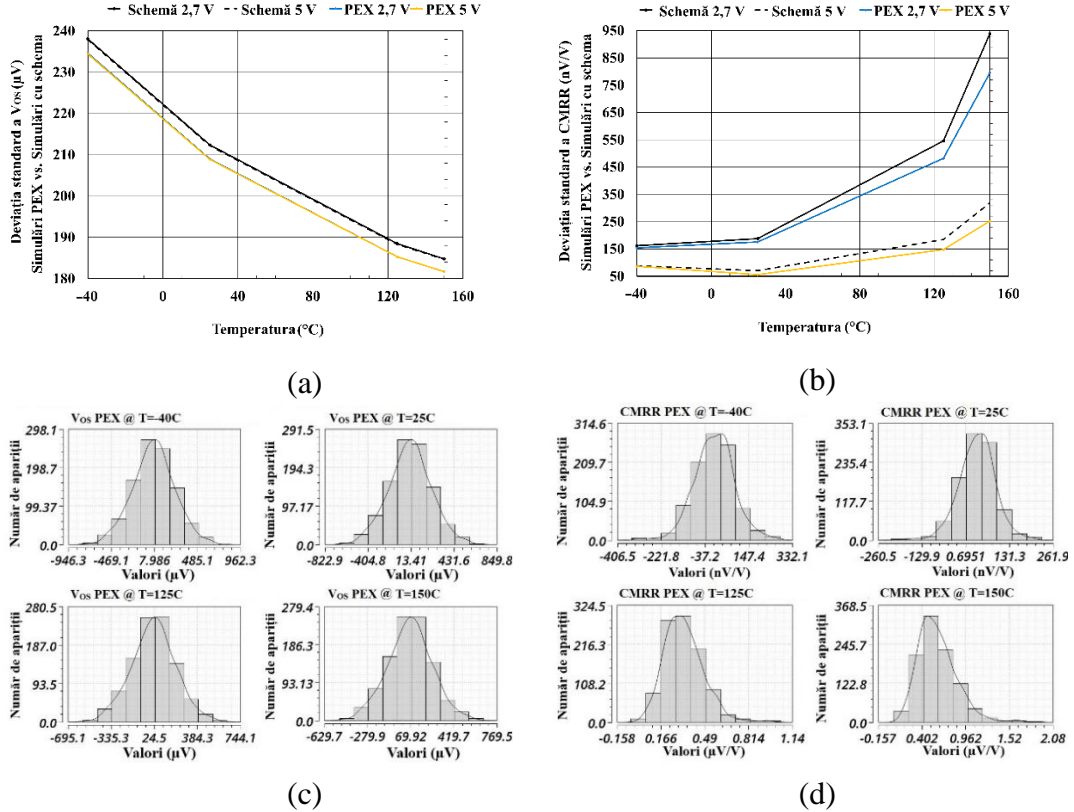


Figure 3.3 Results obtained after PEX. (a) $\sigma(V_{os})$; (b) Comparison - $\sigma(CMRR)$; (c) V_{os} histograms, $VDD = 5 V$; (d) CMRR histograms, $VDD = 5 V$.

3.5 The circuit layout

The layout implementation (Figure 3.22) aims to avoid introducing a systematic offset component through interconnects: the the metal routes geometry that connect the degeneration resistors to the nMOS mirror nodes is treated as a critical element, and the interconnects must be symmetric and equivalent from a resistance standpoint.

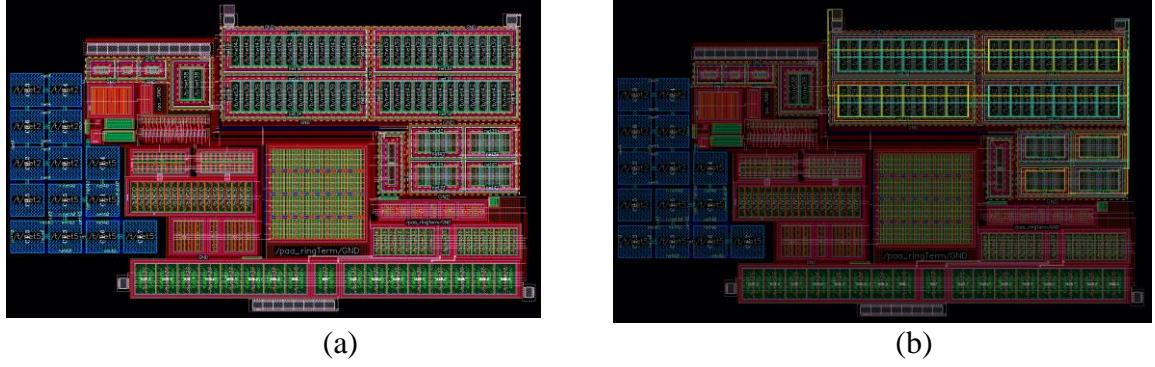


Figure 3.4 Proposed circuit layout implementation, $R_{SP} = 1.5 \text{ k}\Omega$, and $R_{SN} = 1 \text{ k}\Omega$. (a) Top-level view; (b) Detailed view of the metal routing that connects the degeneration resistors.

3.6 Final conclusions

Table 3.1 Comparison of obtained results, $V_{DD}=5\text{V}$, room temperature.

Parameter	Unit	Proposed Op-amp (PEX)	Control Op-amp	Improvement (%)
Gain	dB	116.4	114.3	1.83
UGBW	MHz	3	3.1	-4.2
PM	°	48.9	43.6	12.1
THD, $V_{CM}=2.5 \text{ V}$	%	$2 \cdot 10^{-3}$	$1.7 \cdot 10^{-3}$	-14.8
Spectral Noise 1 kHz	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	25.6	32	20.2
Spectral Noise 10 kHz		17.8	19	6.2
V_{OS} Deviation	μV	208.9	281.8	25.9
CMRR Deviation	nV/V	56.1	110.5	49.2
PSRR	$\mu\text{V/V}$	126.5	124	2
I_O	mA	0.42		0

Chapter 4

Temperature and Power Supply Compensated CMOS Clock Circuit Based on Ring Oscillator

The chapter presents a ~ 50 MHz clock circuit for the charge pump that supplies the op-amps input stage. The solution employs a current-controlled ring oscillator with an internally supply, providing robustness against temperature, V_{DD} , and process variations.

4.1 Proposed architecture design and implementation

4.1.1 Current-starved ring oscillator

The starting point is a classic current-starved ring-oscillator architecture, and the reasons why a direct implementation leads to undesirable frequency variations are highlighted: the relevant transistor V_{DS}/V_{GS} voltages become dependent on V_{DD} and temperature, which affects the charge/discharge times and, consequently, the oscillation frequency.

4.1.2 Proposed ring-oscillator architecture

The proposed architecture (Figure 4.3) reduces supply and temperature sensitivity by using cascoded current mirrors and by controlling the switching current with references derived from blocks developed in previous chapters. To mitigate dependencies introduced by V_{DD} variations at critical nodes, a 2 V low drop-out voltage is implemented. The design targets ≈ 50 MHz frequency at room temperature with a duty cycle close to 50% to ensure efficient switching in the charge pump.

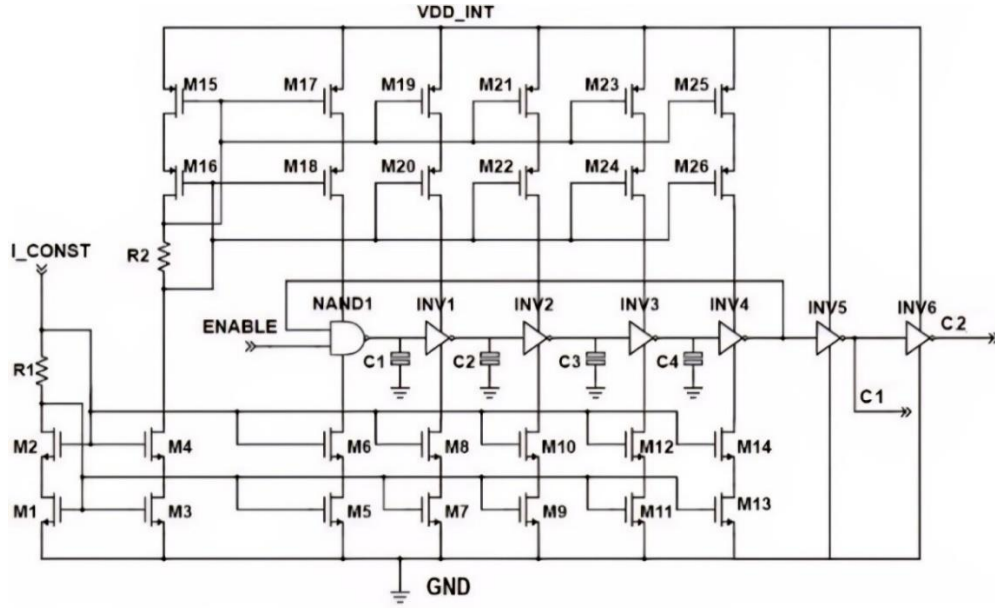


Figure 4.1 Proposed ring-oscillator architecture that is compensated with temperature and supply voltage.

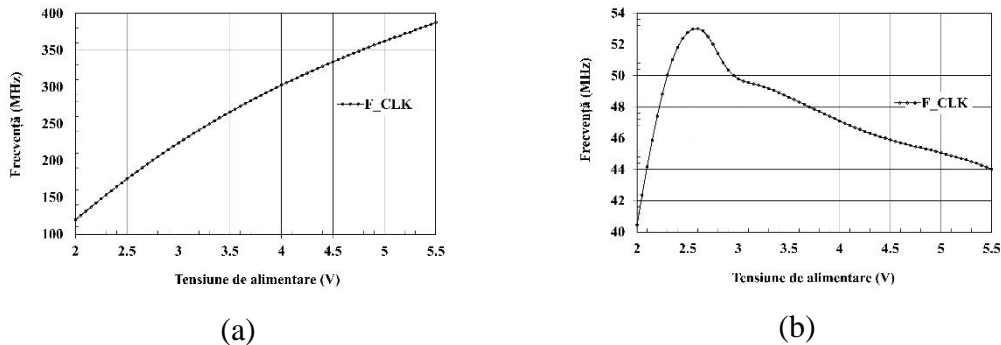
4.1.3 Low drop-out voltage (LDO) concept

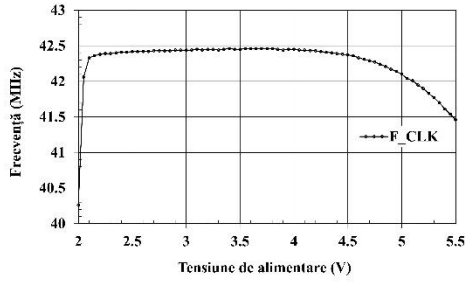
A two-stage op-amp-based LDO with a resistive feedback divider is used to generate V_{DD_INT} from $V_{REF} \approx 1.25$ V, while an output capacitor attenuates disturbances.

4.2 Simulations and results

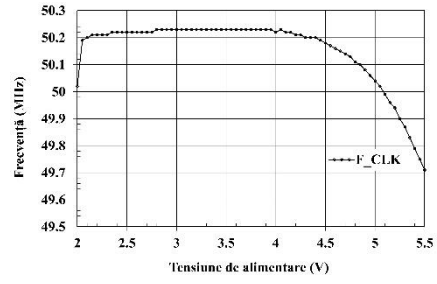
4.2.1 Schematic-level simulations

Figure 4.6 compares the oscillation-frequency dependence on V_{DD} across successive architecture refinements, highlighting the current limiting and the internally supply effect. At least, the frequency variation over V_{DD} range is reduced to ≈ 0.53 MHz.





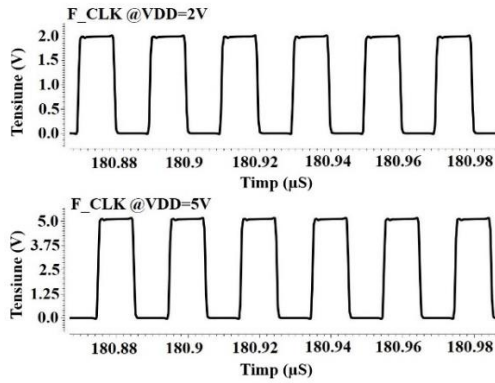
(c)



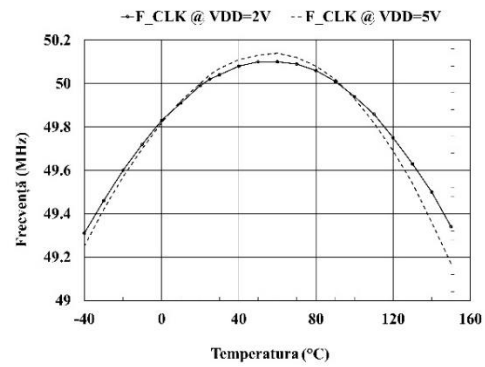
(d)

Figure 4.2 Clock frequency dependence on supply voltage for the ring oscillator. (a) Initial architecture; (b) Current-starved architecture; (c) Architecture that includes the stabilized internal supply; (d) Proposed architecture.

Figure 4.7 indicates $f \approx 50$ MHz and a duty cycle $\approx 50\%$, with $\epsilon_{osc} \approx 1,6\%$.



(a)

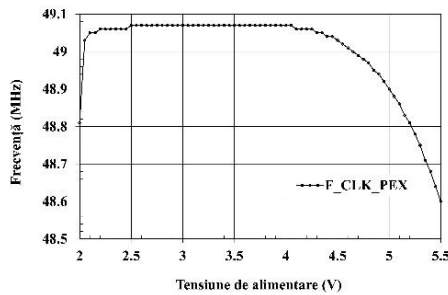


(b)

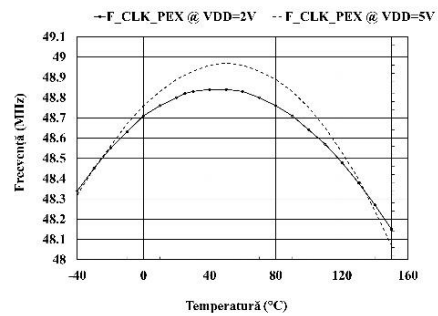
Figure 4.3 Typical simulation for clock signal. (a) Time-domain response; (b) Frequency dependence on supply voltage and temperature.

4.2.2 Post-layout simulations

Post-layout simulations confirm that the compensation is preserved in the parasitic element's presence (Figure 4.11). Table 4.5 benchmarks the results against literature.



(a)



(b)

Figure 4.4 Clock-frequency characterization after PEX simulations: (a) versus supply voltage; (b) versus temperature.

Table 4.1 Comparison with other works from literature.

Parameter	Unit	Proposed oscillator	[69]	[79]	[80]	[81]
Technology	nm	250	250	180	130	250
V_{DD}	V	2	2.2	1.8	3.3	3
Power @ f_0	mW	0.124	1.5	0.43	19.8	N/A
Frequency	MHz	48.9	7	100	1250	1
$\Delta f/f_0$ vs. T	%	1.7	0.84	4.5	4.8	3.33
Temperature	°C	(-40–150)	(-40–125)	(-40–125)	(-40–120)	(-40–125)

4.3 The circuit layout

The layout implementation (Figure 4.12) aims to minimize clock-path parasitic through compact placement, routing, and the upper metal layers use.

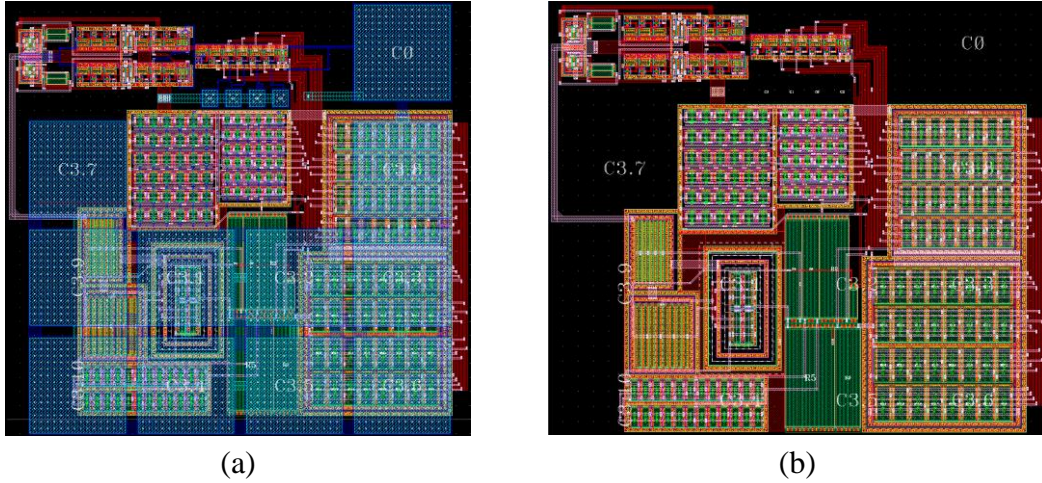


Figure 4.5 The circuit layout implementation. (a) with M_3 and M_4 metal masks included; (b) without the MIM capacitors.

4.4 Final conclusions

The chapter presented a CMOS clock circuit with reduced sensitivity to V_{DD} and temperature. Schematic simulations confirm $f \approx 50$ MHz (Figures 4.6–4.7) and indicate robust operation with low power consumption. Post-layout (PEX) simulations further confirm that the compensation is preserved in the presence of parasitic elements.

Chapter 5

Enhanced Charge Pump Architecture with Feedback Supply Selector for Optimized Switching Performance

5.1 Design and implementation

5.1.1 Charge-pump operating principle

A charge pump transfers charge by controlled charging/discharging of capacitors and is fundamentally limited by $\tau = R \cdot C$ (R includes the switch R_{SW} and interconnect resistances).

5.1.2 Proposed switched-capacitor charge pump

The charge-pump generates $V_{CP} \approx V_{DD} + V_{IN}$ in two phases: during phase 1, C_1 is charged to V_{IN} ; in phase 2, V_{IN} is added on top of V_{DD} to charge the load capacitor (Figure 5.5).

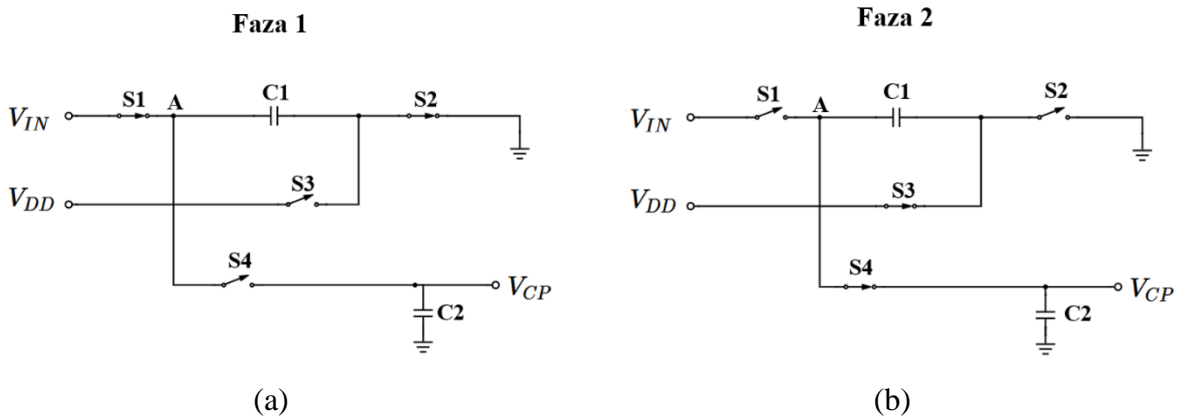


Figure 5.1 Proposed charge-pump architecture: (a) Phase 1; (b) Phase 2.

5.1.3 Low dropout regulator's relevance

Switch losses and load-current variation (50–400 μA) reduce the available voltage margin; therefore, an LDO is used to regulate $V_{\text{IN}} \approx 2 \text{ V}$ and provide the required current.

5.1.4 Innovative maximum supply voltage selector circuit

The proposed circuit dynamically selects the maximum between V_{DD} and V_{CP} to drive the switches, ensuring full switching operation and reducing losses.

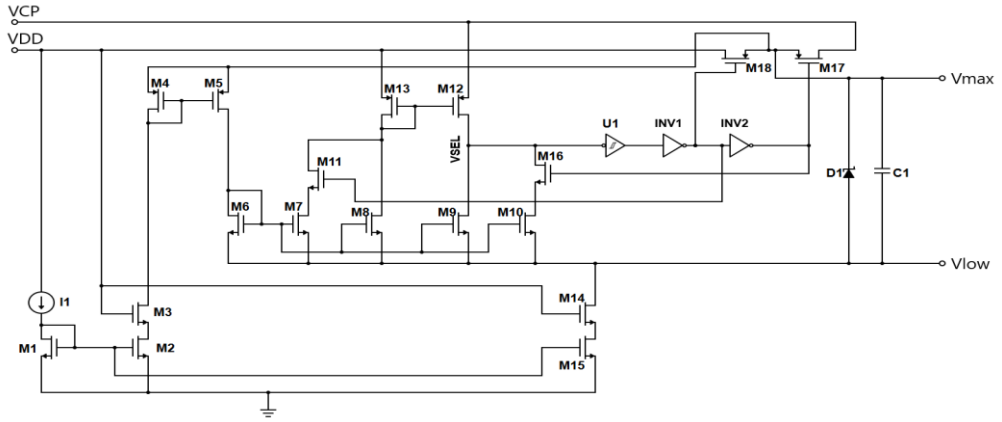


Figure 5.2 Implementation for the maximum supply voltage selector circuit.

5.1.5 Final schematic design for the proposed charge-pump

The architecture implemented is shown in Figure 5.7 and includes the switched-capacitor charge-pump, the LDO ($V_{\text{IN}} \approx 2 \text{ V}$), the maximum supply voltage selector, and auxiliary clock/level-shifting circuits, with C_1 as the flying capacitor and C_2 as the load capacitor.

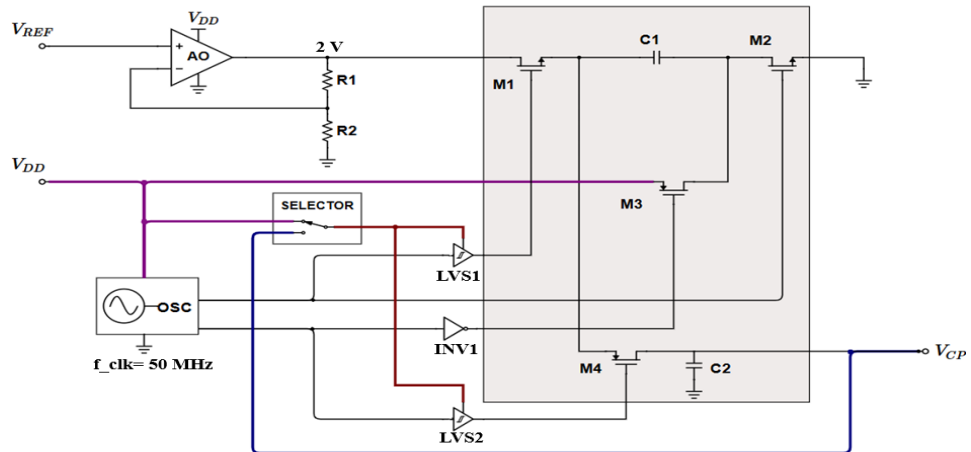


Figure 5.3 Proposed charge pump architecture.

5.2 Simulations and results

5.2.1 Schematic-level simulations

The maximum-voltage selection block benefit is demonstrated by the with/without comparison in Figure 5.11: at $V_{DD} = 2$ V the output increases by approximately 960 mV. V_{CP} is further characterized over $I_{LOAD} = (50\text{--}400)$ μA (Figure 5.12).

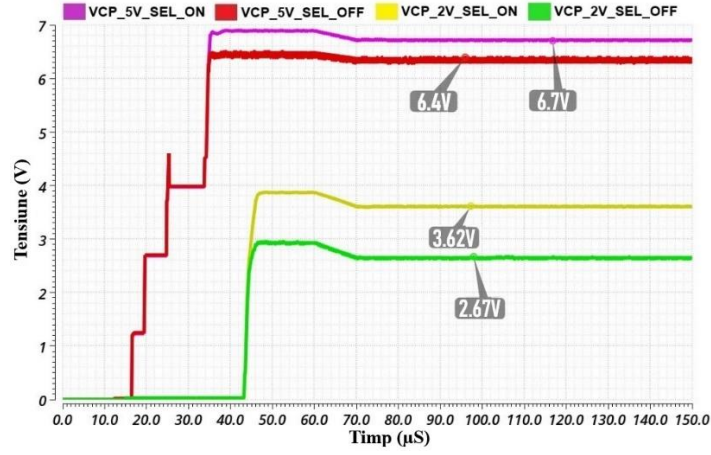


Figure 5.4 Charge-pump efficiency with and without the supply selector.

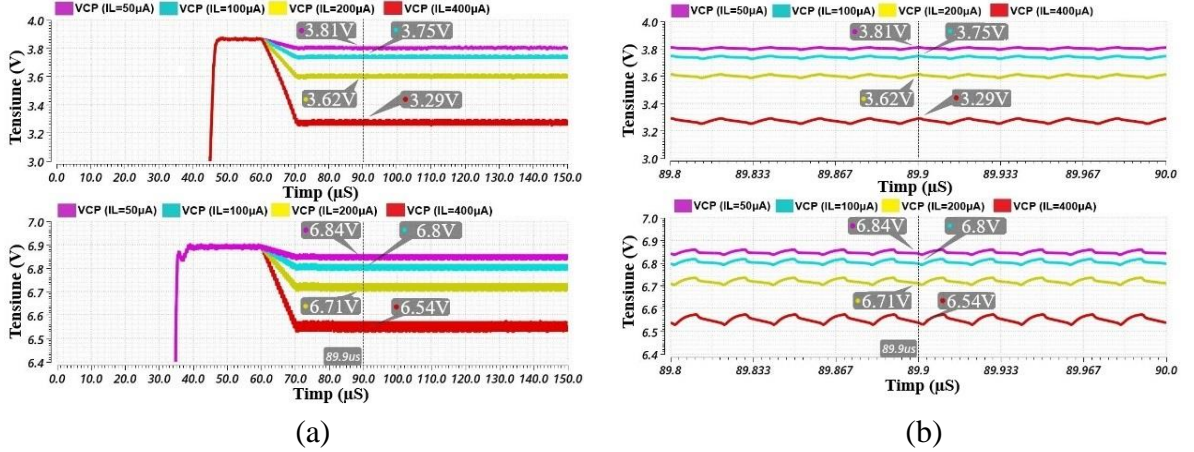


Figure 5.5 Charge-pump response for different load currents: (a) Overall view; (b) Detailed view.

5.2.2 Post-layout simulations

Post-layout simulations with PEX (R_C_CC) show a V_{CP} voltage reduction compared to schematic simulations (routing resistance + R_{ON}) and a slightly reduced effective frequency (≈ 48.13 MHz); the results are presented in Figures 5.16.

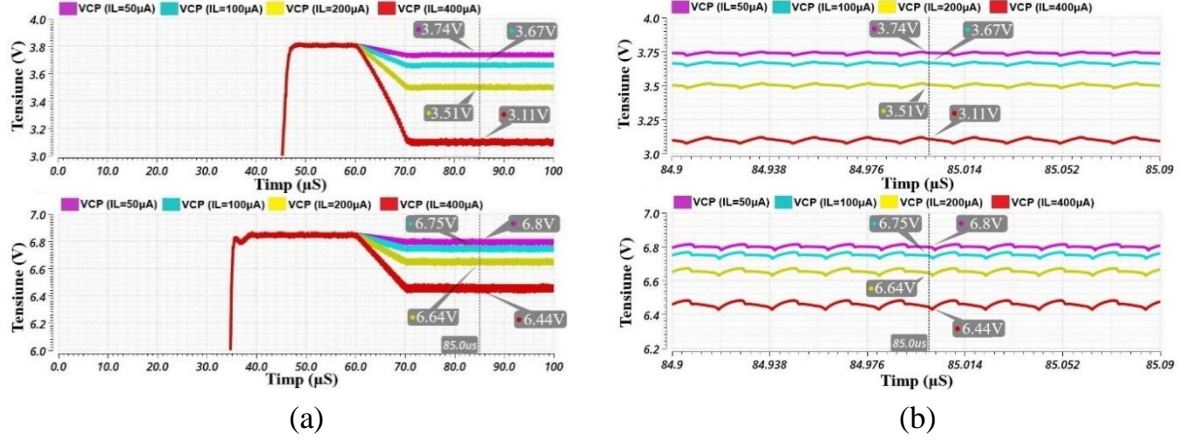


Figure 5.6 PEX results for different load currents: (a) overall view; (b) detailed view.

5.3 The circuit layout

The circuit layout implementation is shown in Figure 5.20. The area is 0.354 mm².

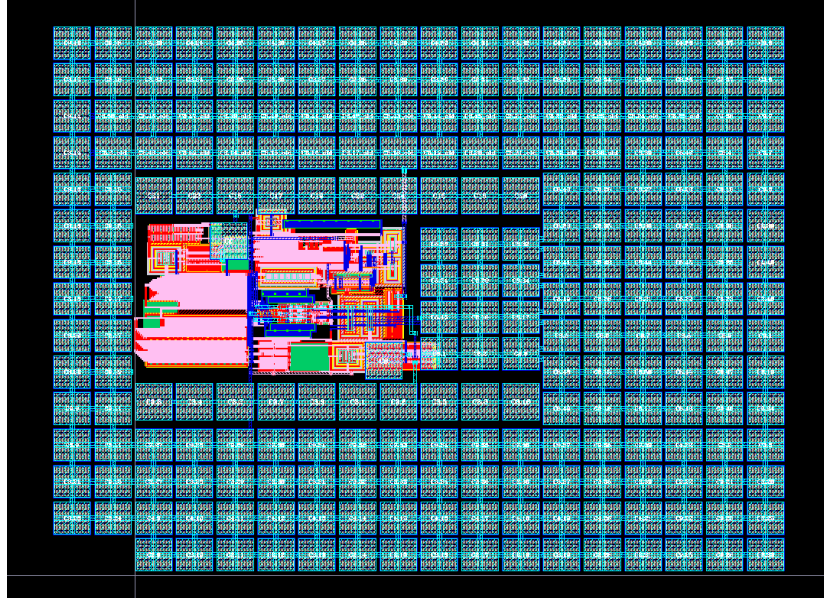


Figure 5.7 Charge-pump layout implementation including the load capacitance.

5.4 Final conclusions

The chapter presented a charge pump that enables the rail-to-rail input swing using only one differential input pair, with dynamic maximum-voltage selection as the key mechanism for optimal switching. Schematic and post-layout simulations validate the architecture, including under the impact of parasitic elements.

Chapter 6

Final Architecture of the Improved-Performance Operational Amplifiers Family

Chapter 6 starts with the op-amps architecture in Chapter 3, implemented predominantly with symmetric low-voltage devices in a 250 nm CMOS technology, for which drain-to-source and gate-to-source voltages are limited to 5.5 V. This choice is motivated by device symmetry, reduced area, and smaller parameter spread (V_{TH} , β).

However, integrating the charge pump (to achieve rail-to-rail input voltage swing with a single differential stage) leads to two limiting cases at high supplies (Figure 6.1), visible at low common-mode ($V_{CM} = V_{SS} - 0.1$ V) and high common-mode ($V_{CM} = V_{DD} + 0.1$ V), which affect both the current mirror that biases the differential pair and the input stage itself. For $V_{CM} = V_{SS} - 0.1$ V, under worst-case conditions ($T = -40$ °C and $V_{CP} \approx 6.8$ V - value obtained in 5.2.2 for $I_{LOAD} \approx 50$ μ A), the voltage exceeds the 5.5 V limit.

For the high- V_{CM} case, a similar analysis leads to approximately 5.79 V, again above the low-voltage device limit. Exceeding these values directly impacts transistor parameters. The practical consequence is confirmed through the g_m variation: at $V_{DD} = 2$ V; g_m remains stable, whereas at $V_{DD} = 5$ V a drop appears once V_{CM} exceeds ≈ 4.5 V.

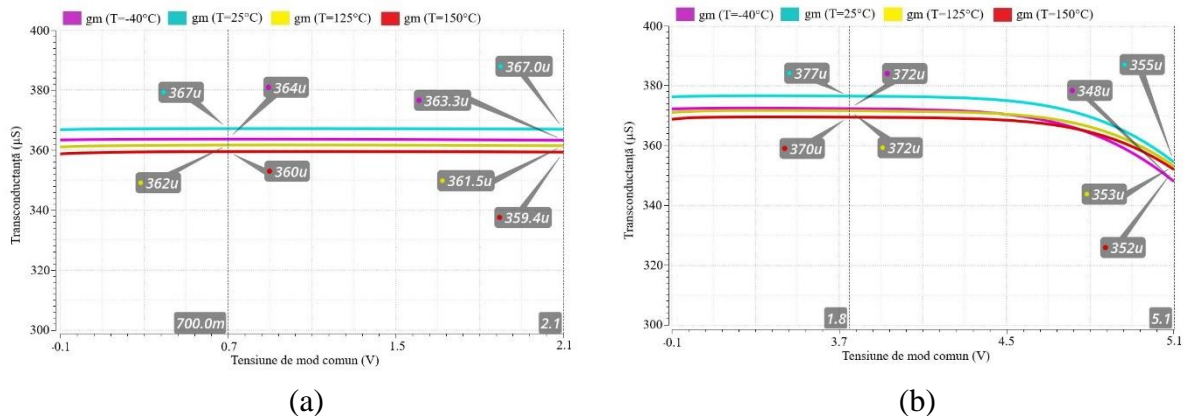


Figure 6.1 Input differential-stage transconductance fluctuation versus common-mode:
(a) $V_{DD} = 2$ V; (b) $V_{DD} = 5$ V.

6.1 Final Operational Amplifiers with improved performance architecture

The final architecture is proposed in Figure 6.2 and removes the limitations caused by voltages exceeding the allowed limit (5.5 V), while preserving the symmetric low-voltage devices advantages in the differential stage. The op-amp design parameters are summarized in Table 6.1.

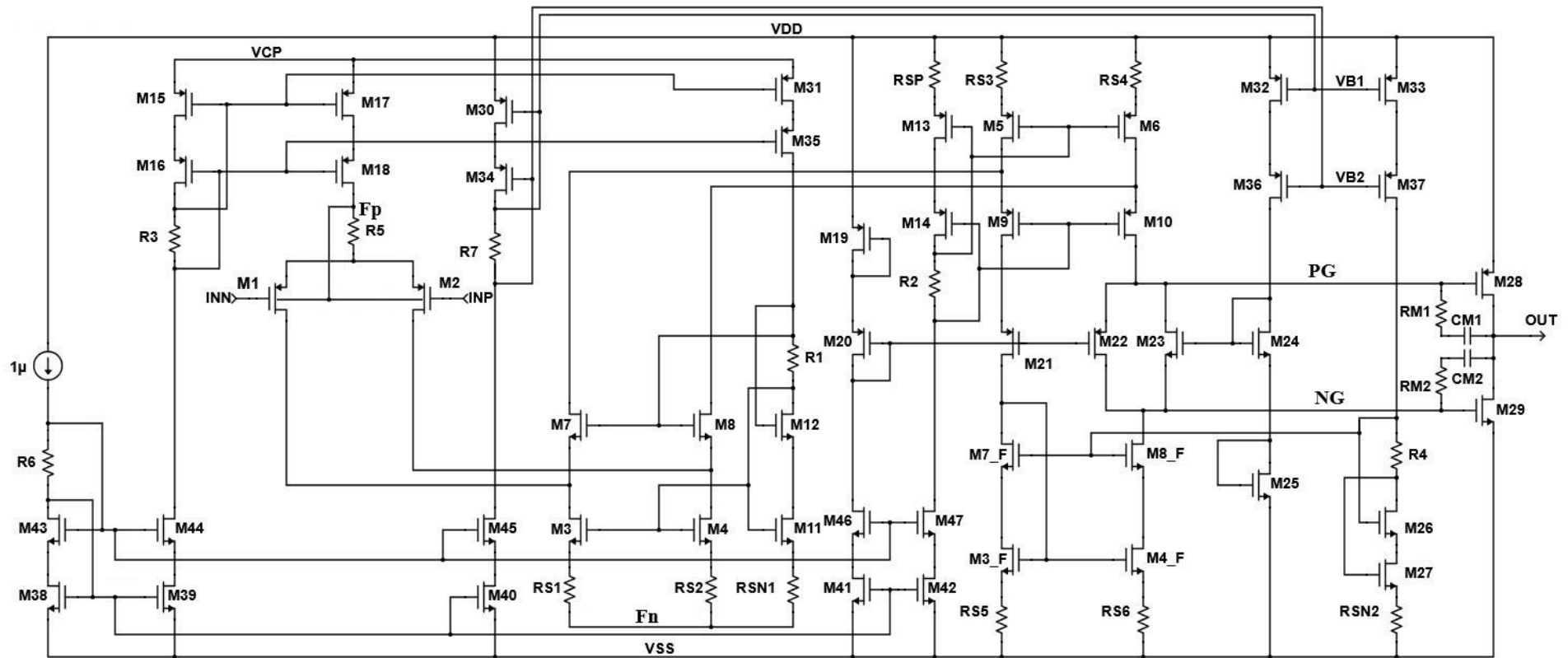


Figure 6.2 Final Architecture of the Family of Operational Amplifiers with Improved Performance.

Table 6.1 Design parameters for the operational amplifier with improved performance.

Category	Elements / group	Value	Unit
MOS Dimensions	M1–M2: W/L	1360/2	μm/μm
MOS Dimensions	M3–M4, M11: W/L	960/5; 120/5	μm/μm
MOS Dimensions	M5–M6, M13: W/L	480/10; 60/10	μm/μm
MOS Dimensions	M7–M8, M12: W/L	160/0.7; 40/0.7	μm/μm
MOS Dimensions	M9–M10, M14: W/L	240/1; 60/1	μm/μm
MOS Dimensions	M3_F–M4_F, M27: W/L	240/10; 60/10	μm/μm
MOS Dimensions	M7_F–M8_F, M26: W/L	160/1; 40/1	μm/μm
MOS Dimensions	M15, M17, M31: W/L	60/3; 480/3; 60/3	μm/μm
MOS Dimensions	M16, M18, M35: W/L	30/0.6; 240/0.6; 30/0.6	μm/μm
MOS Dimensions	M19–M22: W/L	12,6/0.5; 18/1.2; 72/1.2; 36/1.2	μm/μm
MOS Dimensions	M23–M25: W/L	12/1.2; 6/1.2; 4.2/0.5	μm/μm
MOS Dimensions	M28–M29: W/L	468/0.5; 156/0.5	μm/μm
MOS Dimensions	M30–M32–M33: W/L	90/3	μm/μm
MOS Dimensions	M34–M36–M37: W/L	90/3	μm/μm
MOS Dimensions	M38; M39–M40–M41– M42: W/L	4/2; 20/2	μm/μm
MOS Dimensions	M43; M44–M45–M46– M47: W/L	4/2; 20/2	μm/μm
Resistors	R1–R7	15.8; 50.2; 75.3; 28.4; 3; 281; 62.2	kΩ
Source Degeneration	RS1–RS2, RSN1	2.5; 20	—
Source Degeneration	RS3–RS4, RSP	1; 8	—
Source Degeneration	RS5–RS6, RSN2	3; 12	—
Compensation	RM1–RM2	6.9	—
Compensation	CM1–CM2	5.75	pF
Load	Load capacitance	100	pF
Bias	II (T ≈ 25 °C)	1	μA

6.2 Slew Rate Enhancement Circuit for Improved Transient Response

A dedicated circuit is introduced to improve the transient step response (SR), based on (6.6) and illustrated in Figure 6.3.

$$SR = \frac{I_{TAIL}}{C_C} \quad (6.6)$$

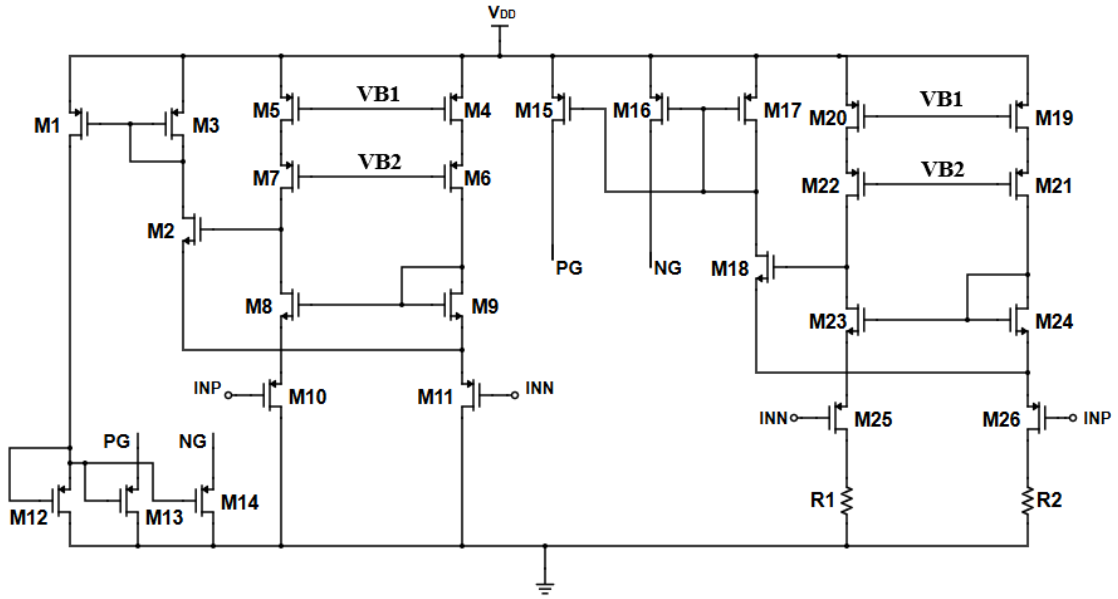


Figure 6.3 Slew Rate Enhancement Circuit for Improved Transient Response.

6.3 Op-amp architecture - top-level view and constituent blocks description

Figure 6.4 summarizes the main blocks integration, namely the current reference/source (Chapter 2, including V_{REF}), the charge pump, the final op-amp (Section 6.1), and the block that constrains the voltage difference between the critical nodes F_P and F_N below the 5.5 V threshold; this top-level view is used as a reference for interpreting the results discussed in Section 6.4. The SR enhancement circuit is integrated within the operational amplifier internal structure shown in Figure 6.2.

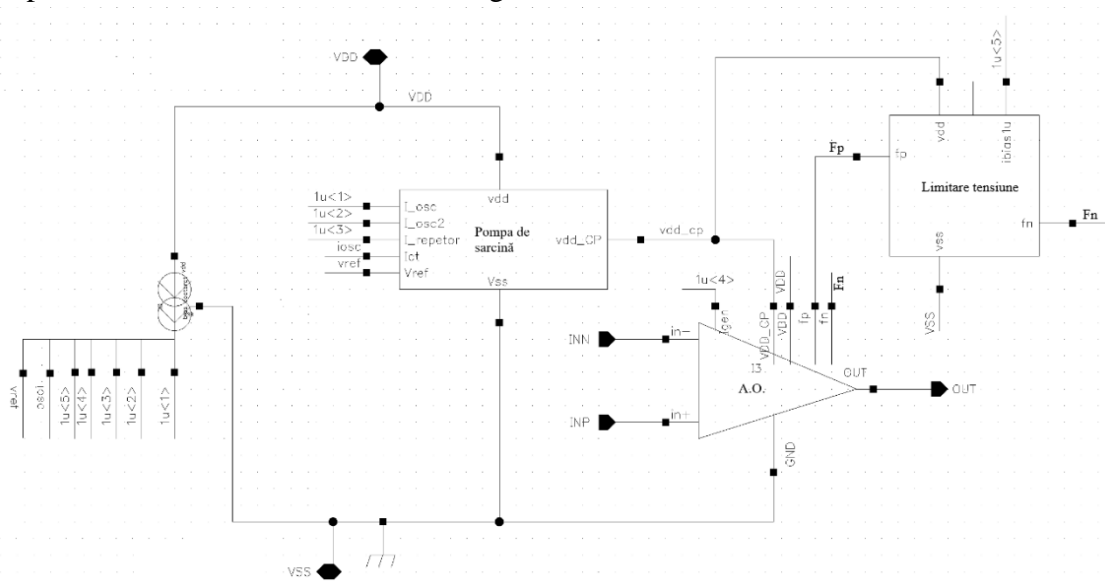


Figure 6.4 Top-level view for the blocks composing the op-amp architecture with improved performance.

6.4 Simulations and results

Schematic simulations include the step response validation with and without the additional circuit (Figure 6.5) for $V_{DD} = 2\text{ V}$ and $V_{DD} = 5\text{ V}$, at $T = 25\text{ }^{\circ}\text{C}$.

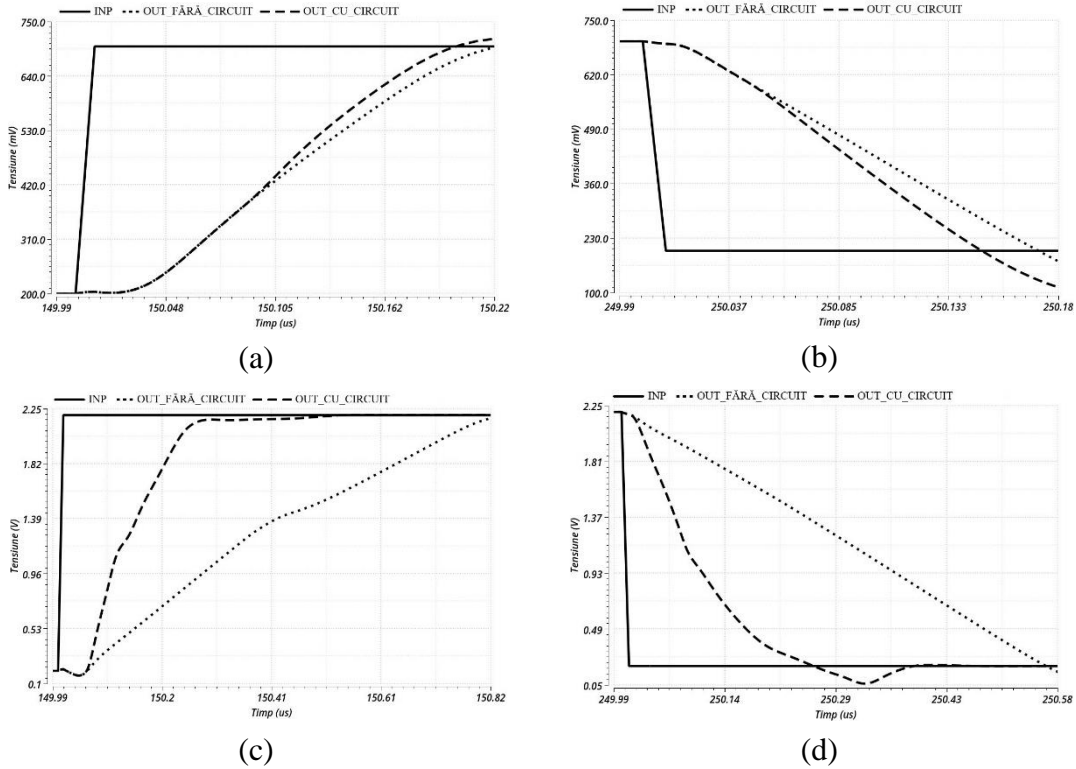


Figure 6.5 Op-amp with improved performance transient response with and without the additional circuit: (a) $V_{DD} = 2\text{ V}$ - rising edge; (b) $V_{DD} = 2\text{ V}$ - falling edge; (c) $V_{DD} = 5\text{ V}$ - rising edge; (d) $V_{DD} = 5\text{ V}$ - falling edge.

The ripple propagation from the differential input-stage to the output is analyzed and PSRR versus frequency is evaluated (Figure 6.7).

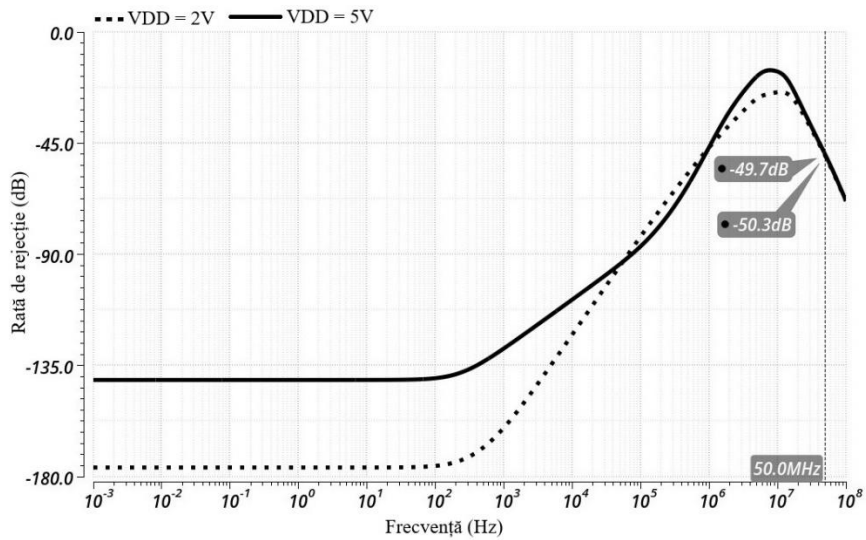


Figure 6.6 Frequency-domain PSRR for the two supply voltages.

At the reference clock frequency (50 MHz), PSRR is 50.3 dB ($V_{DD} = 2$ V) and 49.7 dB ($V_{DD} = 5$ V), corresponding to a $316\times$ attenuation. It is shown that increasing the frequency to 75 MHz can improve rejection to ≈ 60 dB (about $1000\times$ attenuation) and reduce the output ripple from the μV range to the nV range (Figure 6.8); however, the thesis keeps 50 MHz for result consistency. The final results (AC/noise/PSRR/power) are summarized in Table 6.5.

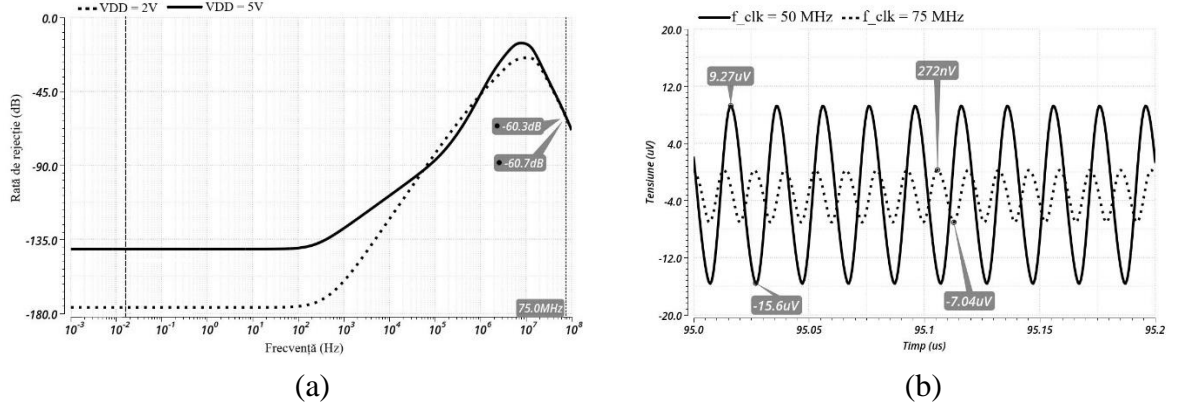


Figure 6.7 PSRR obtained with increased oscillator frequency: (a) waveforms; (b) Output waveform comparison.

Table 6.2 Results summary, $T = 25$ °C.

Parameter	Unit	$V_{DD} = 5$ V	$V_{DD} = 2$ V
UGBW	MHz	4.36	4
PM	°	58.4	51.7
AVOL	dB	116.4	112.4
GM		13.78	16.62
Spectral Noise, 1 kHz	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	23.68	24
Spectral Noise, 10 kHz		17.09	17.33
V_{OS} Deviation	μV	216	218
CMRR Deviation	nV/V	195	410
PSRR @ 50 MHz	dB	49.7	50.3
I_Q	μA	1000	740

6.5 Final conclusions

Chapter 6 establishes the final op-amps family architecture with improved performances. The key limitation is associated with exceeding the 5.5 V limit of low-voltage devices, which translates into g_m degradation. The proposed solution enables continued use of symmetric low-voltage devices in the differential stage, preserving their advantages, while validation through simulations (including frequency-domain PSRR and the synthesis in Table 6.5) confirms the overall system feasibility and robustness.

Chapter 7

Conclusions

7.1 Obtained results

This thesis completion led to the design, optimization, and simulation-based validation of a modern CMOS operational-amplifiers family architecture targeting precision applications characterized by wide temperature variations and stringent stability requirements. The work followed a modular approach, in which each chapter addressed a critical aspect: Chapter 2 proposed a Brokaw-core-based current source intended to stabilize the input-stage transconductance; Chapter 3 reduced offset voltage through current mirrors' source degeneration using precision resistors; Chapter 4 implemented a temperature and supply-compensated ring oscillator to generate a robust clock; Chapter 5 developed a switched-capacitor charge pump with dynamic maximum supply voltage selection to extend the input range; and Chapter 6 integrated these solutions into a final schematic, with architectural modifications that enable low-voltage devices implementation in the differential stage while preserving the advantages in precision and area. Overall, the results confirm the thesis objectives achievement: a high-precision CMOS op-amps family with improved parameter stability over temperature and supply, and rail-to-rail input voltage swing achieved with a single differential stage, without the discontinuities that appears in conventional complementary-input solutions.

7.2 Original contributions of the author

Based on the research carried out in this doctoral thesis, the following original contributions of the author were obtained in the high-precision CMOS operational amplifiers field of design and simulation:

[O.C. 1] **A innovative current-source architecture based on the Brokaw cell principle**, adapted to maintain the input differential-stage transconductance approximately constant over the entire studied temperature range.

[O.C. 2] **Simulation and validation of the current-source architecture** that maintains an approximately constant input-stage transconductance, using multiple simulation methods (transient, process corners, Monte Carlo).

[O.C. 3] **An offset voltage reduction technique based on current mirrors source degeneration using precision resistors** - a local mismatch-compensation method was developed for the folded-cascode current mirrors, reducing sensitivity to threshold-voltage and current-factor variations.

[O.C. 4] **Theoretical and simulation-based demonstration for the source degeneration effectiveness** - it is shown that adding degeneration resistors leads to a substantial offset voltage reduction, thereby improving amplifier accuracy.

[O.C. 5] **A temperature and power supply compensated CMOS clock circuit based on ring oscillator** - the proposed oscillator minimizes frequency dependence on temperature and supply variations, enabling overall analog system robust operation.

[O.C. 6] **Design of an innovative switched-capacitor charge pump intended to extend the op-amps input range** - the proposed solution includes an original feedback mechanism that automatically adjusts the switch-gate drive level, enabling precise control and improving charge-pump efficiency.

[O.C. 7] **Rail-to-Rail input voltage swing achievement with a single differential input stage** - the designed charge pump ensures input transistors correct biasing even when the input signal approaches 0 V or V_{DD} , waiving the requirement for complementary input pairs and avoiding the compromises associated with conventional solutions.

[O.C. 8] **Slew Rate Enhancement Circuit for Improved Transient Response** - an additional circuit was implemented and integrated to enhance the amplifiers transient response to a step input. The results show a faster reaction compared to the original architecture, extending applicability to fast data-acquisition circuits and precision analog-to-digital conversion.

[O.C. 9] **Integration of all developed blocks** (current source, operational amplifier, oscillator, charge pump, step-response enhancement circuit) into a unified operational-amplifiers family architecture. The final schematic was realized and optimal co-operation conditions among subcircuits were ensured by addressing interfacing and compatibility issues.

[O.C. 10] **The proposed integrated amplifiers family validation through comprehensive simulations** - extensive analyses (DC, AC, transient, and Monte Carlo) were performed to verify performance under realistic scenarios.

[O.C. 11] **Design of a high-precision CMOS operational amplifiers family** with performance superior to that of a conventional one. The final implementation exhibits significantly reduced offset voltage, low thermal drift coefficient, improved CMRR and PSRR, and a bandwidth adequate for precision applications, achieving an overall improvement of the performance metrics.

[O.C. 12] **A design methodology establishment for precision operational amplifiers** - by addressing the problem in a multi-dimensional manner, the thesis provides a general framework for developing CMOS op-amps with improved performance. This methodology can support future research and precision analog circuits development under varying supply conditions.

7.3 List of original publications

7.3.1 Journal publications

1. **Stancu, C.**; Neacsu, A.; Profirescu, O.; Dobrescu, D.; Dobrescu, L., *Temperature and Power Supply Compensated CMOS Clock Circuit Based on Ring Oscillator*, *Electronics* **2023**, 12, (3), 507, WOS: 000929372600001, DOI: 10.3390/electronics12030507, indexed in the Web of Science Core Collection under the category Engineering, Electrical & Electronic, with an impact factor of 2.6 and Q2 quartile classification.
2. **Stancu, C.**; Neacsu, A.; Ionescu, T.; Stanescu, C.; Profirescu, O.; Dobrescu, D.; Dobrescu, L., *Offset Voltage Reduction in Two-Stage Folded-Cascode Operational Amplifier Using High-Precision Source Degeneration*, *Electronics* **2023**, 12, (21), 4534. WOS: 001100407700001, DOI: 10.3390/electronics12214534, indexed in the Web of Science Core Collection under the category Engineering, Electrical & Electronic, with an impact factor of 2.6 and Q2 quartile classification.
3. **Stancu, C.**; Mitu, A.A.; Ionescu, T.; Neacsu, A.; Dobrescu, L.; Dobrescu, D., *Enhanced Charge Pump Architecture with Feedback Supply Selector for Optimized Switching Performance*, *Electronics* **2025**, 14, (7), 1484. WOS: 001465760600001, DOI: 10.3390/electronics14071484, indexed in the Web of Science Core Collection under the category Engineering, Electrical & Electronic, with an impact factor of 2.6 and Q2 quartile classification.

7.3.2 Papers published in the proceedings of IEEE-indexed conferences

1. **Stancu, C.**; Dobrescu, D.; Dobrescu, L., *Offset Voltage Reduction Methods for a Two-Stage Folded Cascode Operational Amplifier*, 2022 14th International Conference on Electronics, Computers and Artificial Intelligence (ECAI), Ploiesti, Romania, 2022, pp. 1-4, doi: 10.1109/ECAI54874.2022.9847308
2. **Stancu, C.**; Mitu, A.A.; Neacsu, A.; Dobrescu, L.; Dobrescu, D., *Optimized Current-Source based on Brokaw Architecture for Constant Input Transistors Transconductance*, 2025 17th International Conference on Electronics, Computers and Artificial Intelligence (ECAI), Targoviste, Romania, 2025, pp. 1-4, doi: 10.1109/ECAI54874.2022.9847308

3. **Stancu, C.**; Voicu, A.; Profirescu, O.; Dobrescu, L.; Dobrescu, D., *Slew Rate Enhancement Circuit for Improved Transient Response in Folded Cascode Operational Amplifiers*, 2025 *International Semiconductor Conference (CAS)*, Sinaia, Romania, 2025, pp. 385-388, doi: 10.1109/CAS66707.2025.11222264
4. Voicu, A.; **Stancu, C.**; Dobrescu, L.; Dobrescu, D., *Current Mirror Precision in CMOS: Beyond Threshold Voltage Mismatch*, 2025 *14th International Symposium on Advanced Topics in Electrical Engineering (ATEE)*, Bucharest, Romania, 2025, pp. 1-4, doi: 10.1109/ATEE66006.2025.11299990

7.3.3 Other published works

1. L. Dobrescu, **C. Stancu**, D. Dobrescu, *Advanced MOS Structures Design for Low-Power Devices – Review and Future Challenges*, *Virtual International Conference on Science, Technology and Management in Energy*, 2021

The publications' impact produced during the doctoral program can also be quantified by their citation counts. The paper “*Offset voltage reduction in two-stage folded-cascode operational amplifier using high-precision source degeneration*” has received 6 citations in Web of Science and 11 citations in Google Scholar; the paper “*Offset Voltage Reduction Methods for a Two-Stage Folded Cascode Operational Amplifier*” has received 13 citations in Google Scholar; and the paper “*Temperature and power supply compensated CMOS clock circuit based on ring oscillator*” has received 3 citations in Web of Science and 5 citations in Google Scholar.

Overall, the Web of Science database reports a total of 9 citations for the published articles, corresponding to an h-index of 2, while the author's Google Scholar profile indicates an h-index of 3.

7.4 Perspectives for further developments

The value of this thesis lies in the proposal and validation of a coherent set of solutions that enable a precision CMOS operational amplifiers family development that are robust and energy-efficient, without a significant increase in design complexity. The work provides a design framework for precision analog circuits in submicron technologies and establishes a solid basis for further extensions. Future research directions include the silicon prototype fabrication and its experimental characterization, as well as integration into more complex systems and further refinement for the compensation techniques. Overall, the initial objectives are achieved, and the results open opportunities for continued developments in the precision operational amplifiers' field.

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